A 136-GHz Dynamic Divider in SiGe Technology

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Abstract — A dynamic divide-by-2 circuit is presented. The frequency divider operates from 74 GHz up to at least 136 GHz, limited by the available input power. A balun is included on chip to convert the single-ended input signal to differential, while maintaining input sensitivity better than 0 dBm over the entire frequency range. The divider core has a low power consumption of 72.6 mW from -3.3 V and is implemented in a 210-GHz-\textit{f\textsubscript{T}} SiGe bipolar technology.

Index Terms — Dynamic divider by 2, F-band, Low power, Miller frequency divider, On-chip balun, Transformer.

I. INTRODUCTION

Frequency division circuits are an important component in systems such as PLLs and radio transceivers. Increasing the frequency of operation of dividers allows building faster systems. Generally, dynamic dividers based on the Miller configuration \cite{1} operate faster than static dividers. State of the art dynamic dividers have achieved operation up to 150 GHz in InP technology \cite{2} and 110 GHz in SiGe technology \cite{3}. A 160-GHz divide-by-four circuit has also been demonstrated \cite{4}, but divide-by-two circuits are still necessary for many applications. Static frequency dividers have been shown to work up to 100 GHz in SiGe \cite{5} and 90 GHz in CMOS \cite{6} technologies. In this paper we present a dynamic divide-by-2 circuit in a 210-GHz-\textit{f\textsubscript{T}} SiGe technology that operates from 74 GHz up to at least 136 GHz.

II. FREQUENCY DIVIDER ARCHITECTURE

The dynamic divider chip (Fig. 1) consists of an input stage, the Miller divider core, and a 50- output buffer.

A. Dynamic Divider Core

The schematic of the dynamic divider core is shown in Fig. 2. It is composed of a mixer followed by a low-pass filter. To increase the frequency of operation of the divider, a Cherry-Hooper amplifier \cite{7, 8} is inserted into the mixer. The divider input is biased by a resistor divider. Two sets of emitter-followers act as the filter and also shift the DC component of the signal from the mixer output down to the mixer input. The dynamic divider works from a -3.3 V supply and consumes 72.6 mW.

B. Transformer

The on-chip input network consists of a transformer that converts the single-ended input signal to a differential signal, and an inductor that tunes out the pad capacitance and matches the divider input to 50 . A single-ended input signal is preferred to allow simpler testing of the divider; a single input requires less external components and is beneficial for reducing overall system cost when the divider is employed as a component in bigger systems or instrumentation. All signals inside the chip are differential.

The geometry of the input transformer is shown in Fig. 3. It is implemented in the top two metals of a 5-metal backend. Due to the large vertical spacing of the top two metals, the coupling between them is small. To increase the coupling, the transformer loop was constructed from 4 coupled lines, previously modeled in \cite{9}. The width of the coils is 15 \textmu m, the inner diameter of the transformer loop is 40 \textmu m. Metal 3 is used for the slotted ground shield.
Fig. 4 presents the simulated transformer loss and the input and output match of the entire divider chip. The transformer has less than 2 dB loss over the entire frequency range of interest. The simulated $S_21$ of the divider with the input network is -6 to -7 dB from 80 GHz to 140 GHz.

Fig. 3 Transformer geometry (not to scale).

Fig. 4 Simulated transformer $S_{21}$ and divider $S_{11}$ and $S_{22}$.

C. Output Buffer

The output buffer (Fig. 5) consists of two stages. The first stage is designed with lower current to reduce its load on the divider core. This enables the dynamic divider core to work up to a higher frequency. The second stage is designed as a 50- output driver. The output buffer is broadband and produces a signal that is large enough to drive another divider. It works up to 70 GHz in simulation and at least 68 GHz in measurements. The 2-stage output buffer requires 46.2 mW and operates from -3.3 V.

III. FABRICATION AND TEST SETUP

The dynamic divider was fabricated in the IBM SiGe8HP technology [10] with transistor $f_T$ of 210 GHz and $f_{MAX}$ of 260 GHz. The chip microphotograph is illustrated in Fig. 6 with layout details shown in Fig. 7. The transformer, divider core and the output buffer occupy an area of 380 $\mu$m $\times$ 280 $\mu$m.

The dynamic divider was characterized on-wafer, using 3 different test setups for different frequency ranges, as shown in Fig. 8. An Anritsu 68177C signal source together with $\times6$ or $\times8$ multipliers (Oleson S10MS and S08MS) were employed to produce the input signal. The output signal was observed using both an Agilent 86100B oscilloscope with 70-GHz remote sampling heads and an Agilent E4448A PSA up to 51 GHz. Above 51 GHz (the limit of the PSA) an external amplifier and an external divider were used to bring the output spectrum into the PSA range. De-embedding of the input power was done with a 75-110 GHz power sensor. Due to the unavailability of a higher frequency power sensor, all power measurements above 110 GHz are not calibrated.

Fig. 6 Microphotograph of the dynamic divider. The pad-limited die area is 1.78mm $\times$ 0.63mm, the circuit area is 380 $\mu$m $\times$ 280 $\mu$m.

Fig. 7 Layout details of the dynamic divider.
Fig. 8 Illustration of the test setups employed for characterization of the divider in different frequency ranges (synchronization of instruments and DC connections not shown).

Fig. 9 Measured input sensitivity of the dynamic divider over frequency. Above 110 GHz (shaded area), the power measurements are not calibrated.
* Division was achieved at 136 GHz with the highest output power available from the signal source. The source could not provide enough power at higher frequency.

IV. MEASUREMENT RESULTS

The divider sensitivity curve is given in Fig. 9. The dynamic divider is functional from 74 GHz up to at least 136 GHz, limited by the available signal source power. This covers almost the entire F-band (90-140 GHz). Over the entire operating frequency range, the divider requires an input power less than 0 dBm, lower than in previously published work [4] in SiGe bipolar technology. This input power level can realistically be generated by a VCO. In Fig. 9, the sensitivity curve for setup #3 is lower than the others because the divider bias was adjusted to be able to divide with the lower signal power provided by the ×8 multiplier. The measured input sensitivity above 110 GHz was performed with an uncalibrated power meter. When simulated with constant input power of -5.14 dBm, the divider was dividing properly from 80 GHz to 140 GHz.

Fig. 10 Measured single-ended accumulated output signal from the divider at 96.6 GHz (top), 124.8 GHz (middle), and 136 GHz (bottom). The signal at 124.8 GHz looks cleaner because it was captured with precision timebase.

Stable operation of the divider is demonstrated with the help of Fig. 10 at 96.6 GHz, 124.8 GHz and 136 GHz. In Fig. 10, the output signal is captured on the oscilloscope for several minutes showing that no phase-flipping occurs during that time. Fig. 10 also demonstrates that the divider output buffer produces over 100-mV swing in 50 Ω up to
68 GHz, enough to drive a second divider stage or other circuits.

Fig. 11 Measured output spectrum of the dynamic divider with 102-GHz (left) and 131.2-GHz (right) inputs, showing no harmonics at the output.

Fig. 12 Measured output spectrum of the divider with 102-GHz input. (Left) phase noise at the divider output at 51 GHz, (right) phase noise of the signal source at 17 GHz.

Fig. 13 Measured output spectrum of the divider with 131.2-GHz input. (Left) phase noise at the dynamic divider output at 32.8 GHz including the external amplifier and divider, (right) phase noise of the signal source at 16.4 GHz.

Fig. 11 shows two divider output spectra with 102-GHz and 131.2-GHz inputs. In the second case the shown spectrum is after an external amplifier and divide-by-2 (setup #3). For both inputs, there are no harmonics visible in the output signal. In Fig. 12, the phase noise at the divider output with 102-GHz input and that of the 17-GHz signal source are shown. The phase noise at the divider output is -96 dBc/Hz at 100 kHz offset from 51 GHz. The phase noise at the signal source output is -107 dBc/Hz at 100 kHz offset. The 11.3-dB difference is close to the ideal 9 dB phase noise difference resulting from the 3 times shift in the carrier frequency. The 2.3-dB phase noise difference can result from the frequency multiplier at the input, or from the divider under test. Fig. 13 shows the divider output phase noise with 131.2-GHz input, after a further division by 2 and the 16.4-GHz signal source phase noise. Again, the difference between the output phase noise (-100.2 dBc/Hz at 100 kHz offset) and the source phase noise (-107 dBc/Hz at 100 kHz offset) is less than 1 dB (after accounting for 6 dB shift in frequency), and can be attributed to measurement error, or to any of the instruments in the test setup.

V. CONCLUSION

A SiGe 74-136 GHz dynamic divide-by-2 circuit has been presented. The divider requires less than 0 dBm input power over the entire frequency range for proper division. It features a single-ended input and differential output signals. The divider core consumes 72.6 mW from -3.3 V, and the output buffer requires 46.2 mW from a -3.3 V supply.

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