A New Low-Voltage RMS Converter based on Current Conveyors in MOS Technology

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Abstract: In this paper, a new current mode true RMS-to-DC converter circuit using second generation current conveyors (CCII) is presented. The second generation current conveyor employs MOSFET transistors that are operating in strong inverted saturation region. The proposed methodology provides the following advantages: a complete current-mode circuit makes it suitable for current-mode signal processing applications; modular design of the converter is achieved by using of CCII as the basic building block; and using of CCII that is active building blocks of the converter features low voltage supply and low circuit complexity, which lead to low voltage applications. Hspice simulation results shows high performance of the converter and validate the workability of the proposed circuit.

Keywords: current-mode, converter, current conveyor, MOS.

1. Introduction

The RMS measurement device is widely used in electrical engineering for different purposes such as instrumentation devices [1-3]. The RMS value of a voltage or a current represents the effective energy that is transferred to a load by a periodic source. Different methods have been reported for the precision measurement of the RMS value of an ac current. The on-going trend towards lower supply voltages has brought the area of analog integrated circuits into limelight. In conventional circuits implementation techniques using op-amp and transconductance, the supply voltage restricts the attainable maximum dynamic range. Also, it is well known that the use of current-mode active devices has some advantages such as greater linearity, wider bandwidth, larger dynamic range, and less power consumption when compared to their voltage counterparts: operational amplifiers. The most popular current-mode active device is second generation current conveyor (CCII).

In recent years, some integrated design forms of true RMS-to-DC converter have been proposed. Some of them are designed based on bipolar transistors [4, 5]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in the MOS technology. One attempt is to employ sigma-delta converter [6], but the extra needed circuit leads to a large number of transistors and high power consumption.

In this work, a new design to overcome the above problems is presented. Using a novel synthesis, a squarer/divider circuit based on CMOS second generation current conveyor (CCII) is presented. The CCII is a very interesting, attractive building block, which can easily compete with standard operational amplifiers. (in any way ,it can be considered as an excellent alternative to standard operational amplifier). The proposed squarer/divider is modular and with low supply voltage. The time average operation is performed by a current-mode low pass filter which consists of one capacitor and one MOS transistor. The complexity of this filter is much less than those proposed before [7, 8]. The proposed converter requires very low voltage with minimum supply voltage of one $V_{gs}$ plus two $V_{ds}$ and extra current and voltage biasing are not needed.

The paper organized as follows. In section 2, the basic principle of current-mode true RMS-DC converter operation is discussed. In section 3 the proposed squarer/divider and low-pass filter as the basic building blocks of the converter are presented. In section 4 the circuit and simulation results of the RMS-DC converter that demonstrate the validity of the proposed method are presented; and finally, in section 5 concluding remarks are provided.

2. Basic Principle

The definition of the root means square value of an input signal with a period of $T$ is given by:

$$I_{out} = \frac{1}{T} \int_{0}^{T} I_{in}^2(t) dt$$  \hspace{1cm} (1)

where $I_{in}(t)$ and $I_{out}(t)$ are input and output currents of the RMS-to-DC converter, respectively.

A mathematically equivalent expression, but more precise considering the offset of the system [4], is given by:

$$I_{out} = \left\{ \frac{I_{in}^2(t)}{I_{out}} \right\}$$  \hspace{1cm} (2)

where $\{ ... \}$ represents the averaging operation.

The block diagram of proposed converter is shown in Fig.1, in which it consists of a squarer/divider and a low pass filter [4].

![Figure 1. Block diagram of the RMS-to-DC converter[4]](image-url)
3. Circuit Design

3.1 Current Conveyor

The CCII is a three terminal (X, Y, and Z) device whose responses \( I_Y, V_X \) and \( I_Z \) to the applied excitations; \( V_Y, I_X \) and \( V_Z \) are given by the following matrix representation [9]:

\[
\begin{bmatrix}
I_x \\
V_y \\
I_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & \pm 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_x \\
I_x \\
V_x
\end{bmatrix}
\]

(3)

The node Y is an infinite impedance node with the voltage applied to it is replicated at the node X. Also when a current is injected in the node X, the same current is injected in to node Z. The notation CCII+ denotes a positive Z output current conveyor (Z+) whereas CCII- denotes a negative Z output current conveyor (Z-). This performance can be achieved by combining a voltage follower placed between terminals Y and X, with non-inverting and inverting current buffers (mirrors) between terminals X and Z (+ and -).

Fig. 2 shows block diagram of the proposed current conveyor. The unity gain feedback of op-amp at the front end forces \( V_x \) to be equal to \( V_y \) and the current mirror at the back end lead to \( I_z \) to be equal to \( I_x \) in CCII+ (and \(-I_x \) in CCII-).

![Figure 2. Block diagram of the input of CCII](image)

Fig. 3 shows circuit diagram of the proposed current conveyor. The conveyor consists of a voltage follower and a current mirror. The voltage follower itself is realized by two stages: a pair of complimentary differential amplifiers and a complimentary common source amplifier. Transistors M1-M5 and M6-M10 are employed for NMOS-input and PMOS-input differential amplifiers, respectively. Transistors M9 and M10 are used for common source amplifier, in which the output of the common source amplifier is fed back to the inputs of differential amplifiers to insure of voltage follower operation. The CCII is designed in MOS technology and features low voltage supply and low circuit complexity, which lead to low voltage applications.

![Figure 3. Circuit diagram of the proposed CCII](image)

3.2 Squarer/divider

In this subsection a modular scheme of the current-mode squarer/divider by using of CCII is as the basic active building block is presented. Figure 4 shows the proposed circuit for the squarer/divider employing CCII. The circuit consist of two CCII block and 4 diodes.

The I-V relationship for diode is given by:

\[
I_D = I_s \exp \left( \frac{V_D}{\eta U_T} \right)
\]

(4)

Using Kerchief voltage law (KVL) for the voltage of the diodes in the loop and the I-V relationship of diodes it is obtained:

\[
I_{D_k} = \frac{I_{D_k+} \cdot I_{D_k-}}{I_{D_k}}
\]

(5)

By replacing \( I_{D_k+} = I_{D_k-} = I_m \), \( I_{D_k+} = I_{ rms } \), \( I_{D_k-} = \pm I_Z \) it results:

\[
I_Z = \frac{I_m^2}{I_{ rms }}
\]

(6)

Equation (6) shows the squarer/divider behaviour of the the proposed circuit in the Fig. 4.

3.3 Filter

For a current-mode first-order low-pass filter, output current \( I_{outf} \) and input current \( I_{inf} \) in Laplace domain are related as [10, 11]:

\[
\frac{I_{outf}(s)}{I_{inf}(s)} = \frac{1}{1 + \frac{s}{\omega_c}}
\]

(7)

in which, \( \omega_c = 1/\tau \) is the cut-off frequency of the filter.

Fig. 5 shows the basic circuit of the proposed low-pass filter. For this circuit the I-V relationships of transistor Mf1 in saturation region and its derivation can be expressed by [10]:

\[
I_{outf} = \frac{B}{2} \left( V_{cap} - V_{th} \right)^2
\]

\[
\frac{dI_{outf}}{dt} = \sqrt{2B \cdot \frac{dV_{cap}}{dt}}
\]

(8)

in which, \( V_{cap} = V_{gs} \) is the voltage of capacitor C.
Using (8) and also equation $I_{\text{cap}} = \frac{dV_{\text{cap}}}{dt}$, it results:

$$I_{\text{cap}} = \frac{C\omega_c}{2\beta_{\text{out}}}(I_{\text{in}} - I_{\text{outf}})$$  \hspace{1cm} (9)

Considering the cut-off frequency of the filter as:

$$\omega_c = \frac{\sqrt{2\beta_{\text{out}}}}{C}$$  \hspace{1cm} (10)

and then, substituting (10) into (9) gives:

$$I_{\text{cap}} = I_{\text{in}} - I_{\text{outf}}$$  \hspace{1cm} (11)

Fig. 6 shows the proposed low-pass filter circuit based on (11), which consists of a capacitor and only one transistor.

Comparing this filter with other proposed filters which are realized based on the switched capacitor technique [6] or is implemented by translinear loops [7], or by two class-AB transconductors [8], shows that this analysis gives a much simpler circuit. To obtain this simple circuit, as equation (10) indicates, the cut-off frequency of the filter is allowed to vary with output current. This dependency to $I_{\text{outf}}$, and also the maximum acceptable output ripple determine the suitable values for capacitor $C$. This subject is discussed next. The output current of the RMS-to-DC converter is a DC current $I_{\text{true-RMS}}$ with an ac ripple $I_{\text{ripple}}$ on it. In order that converter gives a good performance the amplitude of this ripple should be small compared to $I_{\text{true-RMS}}$. This requires suitable values for the cut-off frequency of the filter.

As it is mentioned above, $\omega_c$ is proportional to the output current of the converter; however the value of the capacitor can be calculated in such a way that it eliminates the effect of this dependency and also achieves enough accuracy in the output of the converter [12, 13]. To this end and for the first step, (7) in time domain can be written as:

$$\frac{dI_{\text{outf}}}{dt} = \omega_c(I_{\text{in}} - I_{\text{outf}})$$  \hspace{1cm} (12)

Multiplying both sides of (13) by $I_{\text{outf}}$ gives:

$$\frac{d}{dt}I_{\text{outf}} = \omega_c(I_{\text{in}}^2 - I_{\text{outf}}^2)$$  \hspace{1cm} (14)

Equation (14) is time domain representation of a current-mode filter with input of $I_{\text{in}}^2$, output of $I_{\text{outf}}^2$ and cut-off frequency of $2\times\omega_c$. In Laplace domain, the equation can be rewritten as:

$$\frac{I_{\text{outf}}^2(s)}{I_{\text{in}}^2(s)} = \frac{1}{1 + \frac{s}{2\omega_c}}. \hspace{1cm} (15)$$

Assuming that the input current is a sinusoidal function we have:

$$I_{\text{in}} = \sqrt{2}I_{\text{true-RMS}}\cos(\omega t)$$  \hspace{1cm} (16)

where $\omega$ is the frequency of the input current of the converter. Squaring both sides of (16) gives the input signal as follows:
\[ I_{in}^2 = 2I_{true-RMS}^2 \cos^2(\omega t) \rightarrow I_{in}^2 = 2I_{true-RMS}^2 \left(1 + \cos(2\omega t)\right). \]  
(17)

Using input signal of (17) in low pass filter of (15) gives:
\[ I_{out}^2 = I_{true-RMS}^2 \left(1 + B \cos(2\omega t + \phi)\right) \]  
(18)

where
\[ B = \frac{1}{\sqrt{1 + (2\omega/2\omega_c)^2}}, \quad \phi = -t \arctan\left(\frac{2\omega}{2\omega_c}\right). \]  
(19)

Assuming that \( \omega_c << \omega \) and using Taylor series expansion gives:
\[ I_{out} \approx I_{true-RMS} \sqrt{1 + B \cos(2\omega t + \phi)} \approx I_{true-RMS} \left(1 + \frac{B}{2} \cos(2\omega t + \phi) + \frac{B^2}{8} \cos^2(2\omega t + \phi) + \ldots\right) \]
\[ \approx I_{true-RMS} \left(1 - \frac{B^2}{16} + \frac{B}{2} \cos(4\omega t + 2\phi) + \ldots\right) \]  
(20)

From (20), the values of RMS and peak-to-peak ripple at the output current are expressed as:
\[ I_{RMS, out} = \left(1 - \frac{B^2}{16}\right)I_{true-RMS} \]  
(21a)
\[ I_{RMS, out} = \left(1 - \frac{1/16}{1 + (2\omega/2\omega_c)^2}\right)I_{true-RMS} \]  
(21b)
\[ I_{ripple, out} = \frac{B}{2} I_{true-RMS} \]
\[ I_{ripple, out} = \frac{1/2}{\sqrt{1 + (2\omega/2\omega_c)^2}} I_{true-RMS} \]  
(21b)

From (21) it can be concluded that if the frequency of the input signal is at least five times bigger than the cut-off frequency of the filter (\( \omega \geq 5\omega_c \)), then the accuracy of more than 1% can be obtained at the output. In such case, the output current of the RMS-to-DC converter is a DC current \( I_{rms} \) with an ac ripple on it. The amplitude of this ripple is small compared to \( I_{rms} \), i.e., \( I_{out} \approx I_{rms} \).

Considering these conditions and also using (10) it results that the values of the capacitor to achieve the accuracy of more than 1% is:
\[ C \geq \frac{2 \beta I_{rms, max}}{\omega_{min}} \]  
(22)
in which, \( \omega_{min} \) is the lower end of the frequency range and \( I_{rms, max} \) is the output current higher end of the converter.

From (22), it can be seen more accuracy at the output of the converter can be achieved by decreasing the cut-off frequency of the filter by employing larger capacitances or reducing linear transconductance of the transistor of the filter.

4. Simulation Results

Fig. 7 shows the complete circuit diagram of the proposed RMS-to-DC converter based on block diagram of Figs. 1 and 4 and circuit diagrams of Figs. 3 and 6. The circuit was simulated using HSPICE with 0.18um AMS CMOS process parameters. \( V_{dd}=0.93V\), \( V_{dd}=0.93V \) and \( C=900nF \) were employed. Fig. 8 show the steady-state time response of the RMS-to-DC converter for a 60uA peak-to-peak and 10kHz frequency of sinusoidal input currents. The relative error of the output current of converter for different amplitudes of the sinusoidal input currents is calculated, which shows the error less than 3% is achieved for amplitudes between 10uA and 50uA.

**Figure 7.** Complete circuit diagram of the proposed RMS-to-DC converter

**Figure 8.** Time response of a sinusoidal input current and output current of the converter

5. Conclusion

A RMS-to-DC converter by employing a new squarer/divider based on current conveyor is designed. The proposed squarer/divider circuit uses MOS transistors that
are operating in strong inversion region and works in low supply voltage. The results of implemented converter designed based on the proposed squarer/divider and simplified filter show that it can be used in RMS measuring integrated circuits.

References


Author Biography

Ebrahim Farshidi was born in Shoushtar, Iran, in 1973. He received the B.Sc. degree in 1995 from Amir Kabir University, Iran, the M.Sc. degree in 1997 from Sharif University, Iran and the Ph. D. degree in 2008 from electrical engineering at IUT, Iran, all in electronic engineering. He worked for Karun Pulp and Paper Company during 1997–2002. From 2002 he has been with shahid chamran university, Ahvaz, where he is currently assistant professor and head of electrical engineering department. He is author of more than 26 technical papers in electronics. His areas of interest include current-mode circuits design, low power VLSI circuits, and data converters.