ADDER FOR LOSSY ADDITION IN QCA

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Abstract - Recent trends in microelectronics technology have gradually changed the strategies used in very large scale integration (VLSI) circuits. Complementary Metal Oxide Semiconductor (CMOS) technology has been the industry standard for implementing VLSI for the past two decades, but due to scale-down issues of ultra-low dimension achievement is not achieved so far. Hence it paved a way for Quantum Cellular Automata (QCA). It is only one of the many alternative technologies proposed as a replacement solution to the fundamental limit problem that CMOS technology will impose in the years to come. In this brief, presented a new adder that possesses high speed of operation occupying less area is proposed. This adder is designed especially for error tolerant application. Hence in the proposed adder, the overall area (cell count) and simulation time are reduced by 88 and 73 percent respectively. Various results of the proposed adder are shown and described.

Index Terms - Quantum cellular automata, carry look ahead adder, Ripple Carry Adder, lossy application, majority gate, crossover.

I. INTRODUCTION

Quantum Cellular Automata or QCA is an abstract model of quantum computation devised in analogy to conventional model of cellular automata introduced by Von Neumann. Quantum logic circuits are created by orientating pair of quantum electrons and their functionality and properties are defined in [1]. The QCA is advantageous over CMOS technology by extremely small size, high density low power requirement and potentially high processing speed. For the above said reasons the QCA has attracted tones of researchers to get hook in QCA technology. Various QCA circuits, including combinational and sequential circuits have been proposed. Initially these QCA devices mainly focused on arithmetic circuits but now memories, processors, etc. were under development. With the detailed knowledge of the basics of QCA [1]-[9], various adders were designed [10]-[16]. Many adders were designed since addition operation is the key for many complex operations. QCA are designed similar to CMOS in operation. In CMOS, usually the addition is performed with ex-or function, the same function is exploited in QCA also. Hence various logic gates are realised in QCA in the form of majority gates [6]. There are various adders like Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Flow Adder (CFA), Brent-Kung Adder (BKA), etc. are designed in QCA. But recent development in QCA makes these adder design more efficient with less delay, low power consumption and less areas shown in [12]-[16]. The main component in the QCA cell is the majority gate (MG). With this MG, all the logic operations are possible in QCA. The first 1-bit full adder is designed with 5 MG and 2 invertors as shown in [11]. With these results, RCA, CFA and so many adders are designed with reduction in number of MG. Ripple carry adder and carry look ahead adder are presented in [12]. The carry flow adder, explained in [13] is an improved version of RCA of [12] with decreased area and better efficiency. Brent-kung adder (BKA), Ladner-Fischer adder with parallel prefix architecture is explained in [14] and [16]. These parallel prefix architectures are found for pipelining operation that will improve the speed of operation. Hence at most of 3 MG and 1 invertor addition operation is done in QCA.

Fig. 1 Proposed Adder

In this paper, a novel adder is proposed for speedy and scanty addition for error tolerant application as shown in figure 1. The technique discussed in [15] can be exploited for realization of lossless addition operation whereas for lossy addition the proposed adder can be used. The parallel processing architecture is handled here for reducing the delay in addition operation. By the usage of this method the overall area is reduced by 88%. The obtained results are discussed in this paper.

The rest of the paper is organised as follows: a brief basic concepts of QCA and handling methodologies are given in section 2; Existing adder techniques are discussed in section...
3; the proposed innovative is propounded and manifested in section 4; the experimental results on simulation and the outcomes are discussed in section 5; Finally in section 6 conclusion of the work is elucidated.

II. BASICS

QCA is a novel emerging technology in which logic states are not stored as voltage levels but rather the position of individual electron. QCA are used to represent binary state of a system. QCAs are physically implemented as metal QCA, molecular QCA, magnetic QCA. These fabrication are discussed in [1].

![QCA Cell](image1)

![QCA Wire Orientations](image2)

![Invertor](image3)

![Majority Gate](image4)

![Clocking Scheme](image5)

The general QCA cell is a square nanostructure with four quantum dots as shown in figure 2. The two electrons are kept inside the QCA, but due to columbic force of repulsion these electron occupies diagonal dots. This diagonal placement of electron in QCA cell contributes two logics as 0 and 1 as shown in figure 2. The chain of QCA cell forms QCA wire as in figure 3. There are two orientation for wire to come across in QCA as discussed in [4]. They are coplanar crossing and multilayer crossing as shown in figure 3a and 3b respectively. Comparing both coplanar crossing is economical since multilayer crossing is complex during fabrication. The wiring and problems in crossing techniques are discussed in [4]. With the understanding of this QCA cell, a new cell structure called majority gate is proposed as in [5] and shown in figure 4b. The operation of majority gate is given as in (1)

\[ MG(A, B, C) = AB + BC + AC \] (1)
The QCA cells are used to implement Boolean functions. These Boolean functions are broken down into efficient majority gate logic using the theorems proposed in [9]. Initially 1-bit adder is designed and presented in [3]. Here the adding function is performed with three MG and two invertors. As the sum and carry are given as

$$S_i = A_iB_iC_i + A_iB_i\bar{C}_i + \bar{A}_iB_iC_i = M(M(A_i, B_i, C_i), M(A_i, B_i, \bar{C}_i), C_i)$$

$$C_{i+1} = A_iB_i + B_iC_i + C_iA_i = M(A_i, B_i, C_i)$$

For CLA architecture in [15] & [16] are proposed. For this architecture, consider two n-bit addends A=an-1, an,……,0; B=bn-1,bn,……,0. For i<sup>th</sup> position, carry look ahead adder poses two signal generate G, generate and P, propagate signals are computed as G=Ai Bi and P=Ai + Bi. But the former carry propagation delay is relieved. So for this faster carry propagation two MGs are cascaded and carry is generated. Further for sum generation, two MGs and one invertor are linked to worst case path of adder possessing (n/2)+3 MG and one invertor as whole for n-bit addition as shown in figure 6&7.

$$C_{i+2} = M(M(Ai+1, Bi+1, Gi), M(Ai+1, Bi+1, Pi) C_i)$$

Hence this architecture is the most efficient adder design. But when using this design in both lossless or error sensitive and lossy or error tolerant areas, this will increase the area occupancy, delay and also minimises the speed. For such lossy applications, small, high speed and compact adder is required. Hence a speedy, scanty adder is proposed.

### IV. PROPOSED METHOD

The main objective of any electronic design is to achieve low power, less area and minimum delay. For this QCA, the overall performance can be improved by reducing the number of cells which simultaneously causes the power and delay to reduce. Here a new adder is proposed as in Figure 8.

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>ACCURATE OUTPUT</th>
<th>APPROXIMATED OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>Cin</td>
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<tr>
<td>0</td>
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Fig. 6 Carry Chain of CLA Adder[18]

Fig. 7 Sum Chain of CLA Adder[18]
A fault tolerant system is a system that continues to function with little degraded accuracy but it will not affect the efficiency of the system. Usually the sum and carry signals are generated by adding two addends. For such systems the proposed adder can be used. So that the area and delay can be minimised. Consider two 1-bit addends, the sum and carry are related by the following table. The result of adding a and b is sum and the overflow bit is carry.

In this novel adder, the sum is proposed as inversion of carry. Here the sum is inversion of carry for all combination except for the combination of (0 0 0) & (1 1 1). Thus for the inputs (0 0 0) & (1 1 1) faulty output will be obtained as discussed in [23]. Since this adder suits only for error tolerant
design this failure is tolerable in the system. The performance of this adder is explained in the table I. In this table, the accurate and approximated results are shown. Here in the approximated results the tick mark indicates correct output and cross indicates wrong output. For this adder the error occurs only at sum for two combination of inputs such as (0 0 0) & (1 1 1) and not at any of the carry. The obtained results and simulations are discussed in the below section.

<table>
<thead>
<tr>
<th>DIFFERENT ADDERS</th>
<th>INPUTS</th>
<th>NO. OF CELLS USED</th>
<th>TOTAL SIMULATION TIME</th>
<th>AREA (m²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDER [18]</td>
<td>32</td>
<td>6775</td>
<td>67</td>
<td>2.2</td>
</tr>
<tr>
<td>PROPOSED ADDER</td>
<td>32</td>
<td>791</td>
<td>18</td>
<td>0.3</td>
</tr>
</tbody>
</table>

V. RESULTS

The QCA design is simulated in QCADesigner 2. The QCA Designer tool facilitates rapid design, layout and simulation of QCA circuits by providing powerful CAD features available in more complex circuit design tools. The layout of the proposed adder is shown in Figure 9. The obtained results are shown in figure 10 and tabulated in table II. The overall performance of the 32-bit addition is depicted and their outputs are verified. The proposed adder is better than the former adder in terms of area, delay, clock phases etc. The overall cell count obtained in this adder is 791 whereas for adder in [18] is 6775. The layout is also simple for this adder comparing other adders. For the proposed adder, the area is decreased about 88%, simulation time by 73% and clock phases by 63%. Hence for lossless addition, this adder can adapted. The performance analysis of the adders are shown in figure 11.

VI. CONCLUSION

QCA is a technology that provides a gateway of ultra small electronics. A new adder is designed and presented for error tolerant application which posses a area and time reduction of 88% and 73% respectively. This adder occupies a total area of 791 cells and total simulation time of 18ns. On comparing layout strategies and timing strategies the proposed adder performs much better than the conventional adders. Thus for lossless addition adder in [18] and for lossy addition this newly proposed adder can be used.

REFERENCES


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