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Research Article

Realizing an Omega-Shaped Gate MoS_2 Field-Effect Transistor Based on a SiO_2/MoS_2 Core–Shell Heterostructure

Dong-Hui Zhao, Zi-Liang Tian, Hao Liu, Zheng-Hao Gu, Hao Zhu,* Lin Chen, Qing-Qing Sun,* and David Wei Zhang

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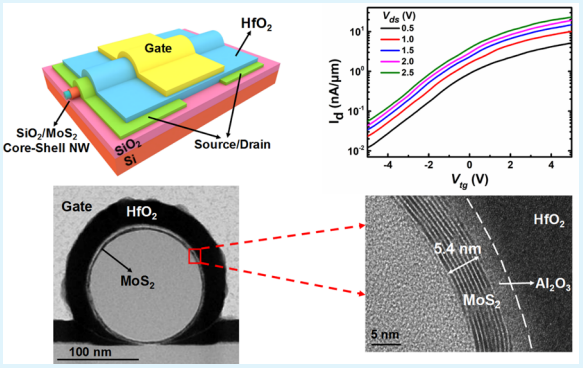
ABSTRACT: Substantial progress has been made in the experimental synthesis of large-area two-dimensional transition metal dichalcogenide (TMD) thin films in recent years. This has provided a solid basis to build non-planar structures to implement the unique electrical and mechanical properties of TMDs in various nanoelectronic and mechano-electric devices, which, however, has not yet been fully explored. In this work, we demonstrate the fabrication and characterization of MoS_2 field-effect transistors (FETs) with an omega (Ω)-shaped gate. The FET is built based on the SiO_2/MoS_2 core–shell heterostructure integrated using atomic layer deposition (ALD) technique. The MoS_2 thin film has been uniformly deposited by ALD as wrapping the SiO_2 nanowire forming the channel region, which is further surrounded by the gate dielectric and the Ω-gate. The device has exhibited n-type behavior with effective switching comparable to the reference device with a planar MoS_2 channel built on a SiO_2/Si substrate. Our work opens up an attractive avenue to realize novel device structures utilizing synthetic TMDs, thereby broadening their potential application in future advanced nanoelectronics.



KEYWORDS: *MoS_2, field-effect transistor, Ω-shaped gate, core–shell, nanowire, atomic layer deposition*

INTRODUCTION

In the past decade, transition metal dichalcogenides (TMDs) have emerged as an attractive class of two-dimensional (2D) layered materials with potential in various research fields because of their unique structures and rich properties.[1−5] Molybdenum disulfide (MoS_2) is a typical and widely studied TMD semiconductor, which has a tunable band structure with film thickness[6−8] and robust optical[9,10] and mechanical[11,12] properties. So far, different techniques to synthesize high-quality large-area TMD thin films have been extensively studied to overcome the shortcomings of the conventional mechanical exfoliation method such as uncontrollable flake size, thickness, and location. For example, chemical vapor deposition (CVD) using MoO_3 and S powders is effective in growing large-scale crystalline MoS_2 films based on the vertical stacking of the triangle-shaped flakes which, however, can lead to a nonuniform film in a limited scale.[13] CVD synthesis of MoS_2 can also be achieved by simply sulfurizing the pre-deposited Mo[14,15] or MoO_3[16] layers. However, the film roughness is generally unsatisfactory because of the limited control of metal/oxide deposition techniques. Alternatively, atomic layer deposition (ALD) can also be used to synthesize large-area ultra-thin MoS_2 films following the layer-by-layer deposition mechanism.[17−19] The synthesized TMD films retain the inherent advantages of the ALD process, including wafer-scale thickness uniformity, thickness controllability, reproducibility, and high conformity.[20,21] More importantly, because of the self-limiting nature of the surface reaction in the ALD process, such a deposition approach can be widely applied in the construction of advanced non-planar geometry devices like fin field-effect transistors (FinFETs) and gate-all-around (GAA) FETs.[22] Thus, the integration of 2D TMDs as the active conduction channel in a non-planar FET by ALD technique is very attractive, as it will leverage the advantages afforded by the novel TMD semiconductors with the vast infrastructure of current semiconductor technology. Yet, up to now, most of the research works focusing on MoS_2 devices are based on planar geometry using mechanical exfoliation or synthetic methods on various substrates. Although some experimental exploration has been attempted on the integration of MoS_2 in three-dimensional (3D) electrical devices such as FinFET, the synthetic methods are largely based on CVD, which cannot form a continuous and uniform

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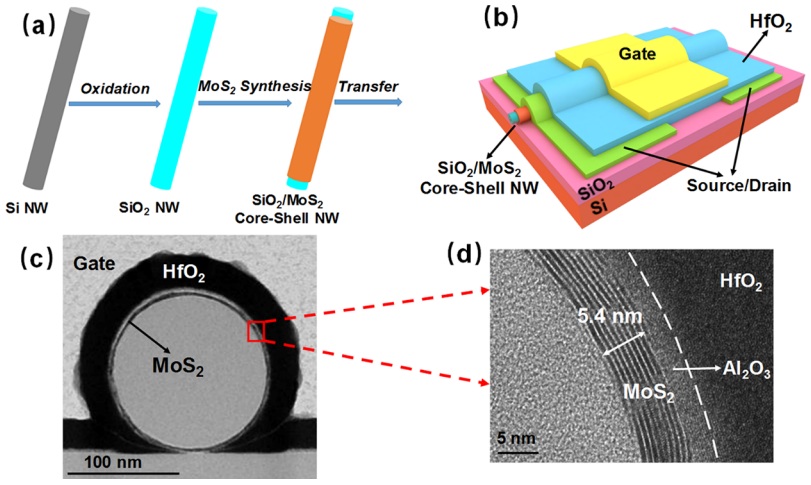

Figure 1. (a) Schematic illustration of the fabrication process of the SiO_2/MoS_2 core−shell nanowire heterostructure. (b) The 3D schematic of the MoS_2 FET based on the SiO_2/MoS_2 core−shell heterostructure. (c) Cross-sectional TEM image of the SiO_2/MoS_2 core−shell nanowire-based FET. (d) HRTEM image focusing on the MoS_2 channel material, which shows that the MoS_2 film was well crystallized with a layered structure.

thin film, especially on the surface of structures with a high aspect ratio. For example, Chen et al. demonstrated 3D FinFETs with hybrid Si/MoS_2 channels,[23] and Lan et al. successfully fabricated a complementary logic inverter based on MoS_2 fin-shaped FETs.[24] However, continuous and uniform MoS_2 films have not been achieved by using the CVD method toward large-scale device fabrication.

Recently, semiconductor nanowire[25−28] and nanotube[29−31] FETs have been intensively studied as the fundamental building blocks of future nanoelectronic device and circuit technologies. The surround-gate structure formed in a nanowire/nanotube FET allows excellent electrostatic gate control over the channel, suppressing the short-channel effects and lowering the power consumption.[32,33] Moreover, as compared to the planar bulk, the larger surface-to-volume ratio of the nanowire can boost the efficiency of nanowire-sensing devices, which can be an effective addition to the TMD-based sensors.[34] However, the combination of the ultra-thin TMD film with the nanowire/nanotube architecture has rarely been reported so far, largely due to the lack of robust film preparation and device fabrication techniques. Here, in this work, we report the design and fabrication of the MoS_2 FET with an omega (Ω)-shaped gate. The device is built based on the SiO_2/MoS_2 core−shell heterostructure, which is formed by depositing a few-layer MoS_2 film by ALD on the surface of SiO_2 nanowires followed by the deposition of the gate dielectric and the Ω-shaped top gate electrode. The uniform MoS_2 layer and the gate stack surrounding the SiO_2 core are confirmed by characterization including electron microscopy, Raman spectroscopy, and X-ray spectrometry mapping. Such an Ω-gate MoS_2 FET has exhibited a well-defined n-type semiconductor behavior with an on/off current ratio of $\sim 10^2$ and an electron mobility of ~0.02 $cm^2\ V^{-1}\ s^{-1}$, which are comparable to the performance of the device fabricated on a planar SiO_2/Si substrate. This work has provided new strategies for promoting the future electronic device application of TMD materials beyond 2D geometry.

RESULTS AND DISCUSSION

Figure 1a schematically illustrates the preparation steps of the SiO_2/MoS_2 core−shell nanowire heterostructure, which forms the channel region in the subsequently fabricated Ω-shaped gate MoS_2 FET (see details in the Experimental Methods). Generally, the single-crystal Si nanowires were first grown in a low-pressure chemical vapor deposition (LPCVD) furnace following the vapor−liquid−solid (VLS) mechanism, which was further oxidized in SiO_2 nanowires by dry oxidation. Few-layer MoS_2 was then deposited surrounding the SiO_2 nanowire core by ALD and was annealed at high temperatures in a sulfur atmosphere to improve the crystallinity and reduce the defects. After transferring the SiO_2/MoS_2 core−shell nanowire to the SiO_2/Si substrate, the MoS_2 FET with the Ω-shaped gate was fabricated by depositing the HfO_2 dielectric layer and the gate electrode (Figure 1b). Figure 1c shows a cross-sectional transmission electron microscopy (TEM) image of the FET. A clear Ω-shaped top gate structure has been obtained, which is expected to enhance the gate control over the non-planar channel. The MoS_2 layer has been grown on the surface of the SiO_2 nanowire forming the SiO_2/MoS_2 core−shell hetero-structure, which is further surrounded by the Al_2O_3/HfO_2 dielectric layer and the Ω-shaped gate. Furthermore, the high-resolution TEM (HRTEM) image focusing on the channel material (Figure 1d) indicates that the MoS_2 film was well crystallized with a layered structure, and the thickness is about 5 nm. It should be noted that there is a slight variation in the thickness of the MoS_2 film circumferentially around the nanowire (Figure S1), which is mainly due to the slight nonuniform growth of the MoS_2 film caused by different surface topographies of the SiO_2 nanowires at different locations. Additionally, the energy-dispersive X-ray spectrometry (EDX) elemental mapping is performed based on the TEM (Figure 2a) of the cross section of the MoS_2 transistor. Figure 2b−d shows the elemental mapping images of Hf, Mo, and S elements, respectively, which further confirm the 3D structure of the MoS_2 FET device.

In order to characterize the uniformity, crystallinity, and stoichiometry of the as-synthesized MoS_2 layer, we have used ALD to grow few-layer MoS_2 on the surface of both the planar SiO_2/Si substrate and the SiO_2 nanowire for comparison. In our previous work, MoS_2 ultra-thin films have been successfully grown on a sapphire substrate by using the ALD-based techniques.[19,21] The Al_2O_3 substrate is more favorable to be used for TMD deposition, as compared to the SiO_2/Si substrate because of the smaller lattice mismatch between

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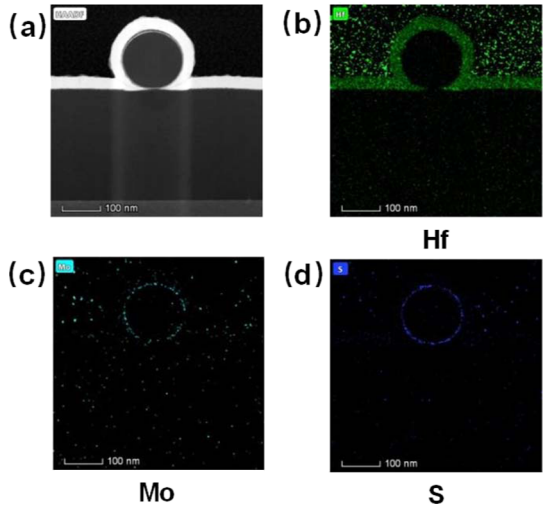

Figure 2. (a) TEM image of the cross section of the MoS_2 FET used for EDX mapping. EDX elemental maps of (b) Hf, (c) Mo, and (d) S from the TEM image shown in (a).

Al_2O_3 and hexagonally arranged TMDs and the dielectric screening effect causing a reduction in Coulomb scattering by using Al_2O_3.[14,35] However, the MoS_2 deposition on the surface of Al_2O_3 is not compatible with most Si-based device fabrication processes, and the aforementioned issues of deposition on the SiO_2 surface can be relieved by using the ALD techniques with more deposition cycles, namely longer incubation periods.[36]

Characterization of the MoS_2 film deposited by 40 ALD cycles on a planar SiO_2/Si substrate (2 in.) and on the surface of SiO_2 nanowires was performed, and are shown and compared in Figure 3. The surface morphology of the MoS_2 film on the planar substrate is characterized by atomic force microscopy (AFM). As illustrated in Figure 3a, the film surface is uniform and smooth with a root-mean-square roughness of 0.63 nm over a scanned area of 5 μm × 5 μm. The film thickness is ~5.5 nm, which is estimated by X-ray reflectivity (XRR) measurements (Figure S2), and is in good agreement with the thickness of the MoS_2 layer deposited on SiO_2 nanowires (Figure 1d). This indicates that the thickness of the MoS_2 film is independent of the surface geometry and can be precisely controlled by the ALD deposition cycle number. We have further obtained the MoS_2 nanotubes by removing the SiO_2 core of the SiO_2/MoS_2 core–shell heterostructure using wet etching (Figure S3), which also suggests the uniform deposition of MoS_2 on the surface of SiO_2 nanowires by ALD. Figure 3b shows the Raman spectra at the excitation laser wavelength of 532 nm obtained from five different locations of the MoS_2 film on the 2 in. planar SiO_2/Si substrate. Featured Raman peaks have been clearly observed with the peak at 382.448 cm^{-1}, which is originated from the E^1_{2g} (in-plane vibration of Mo and S atoms) mode, while the peak at 406.927 cm^{-1} corresponds to the A_{1g} (out-of-plane vibration of S atoms) mode. More importantly, the identical E^1_{2g} and A_{1g} peak positions in the spectra obtained from all the five selected locations suggest excellent uniformity of the MoS_2 film. This also provides a technical basis for the formation of the SiO_2/MoS_2 core–shell structure in which the MoS_2 layer is uniformly coated surrounding the SiO_2 nanowire. The frequency difference (Δk) between the E^1_{2g} and A_{1g} modes is 24.48 cm^{-1}, which is consistent with the reported Raman results of the MoS_2 film with a similar thickness.[37] In addition, Figure 3c illustrates the scanning electron microscopy (SEM) image of the SiO_2/MoS_2 core–shell nanowires obtained by depositing 40 ALD cycles of MoS_2 on the surface of SiO_2 nanowires. High-density nanowires have been grown from the Au catalyst on the substrate, and Raman spectroscopy can be utilized to characterize the MoS_2 layer. As shown in Figure 3d, five different locations are also selected from the substrate covered with SiO_2/MoS_2 core–shell nanowires. The Raman

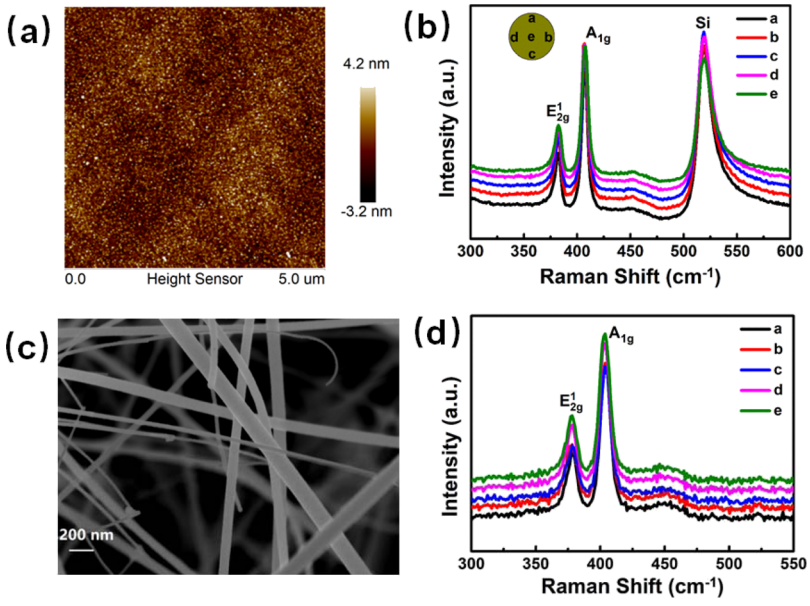

Figure 3. (a) AFM image of the MoS_2 film deposited on a planar SiO_2/Si substrate with 40 ALD cycles over an area of 5 μm × 5 μm. (b) Raman spectra (λ_{exc} = 532 nm) of the MoS_2 film obtained from five different locations on a 2 in. planar SiO_2/Si substrate. (c) SEM image of the SiO_2/MoS_2 core–shell nanowires obtained by depositing 40 ALD cycles of the MoS_2 film on the surface of SiO_2 nanowires. (d) Raman spectra of the SiO_2/MoS_2 core–shell nanowires obtained from five different locations on the sample.

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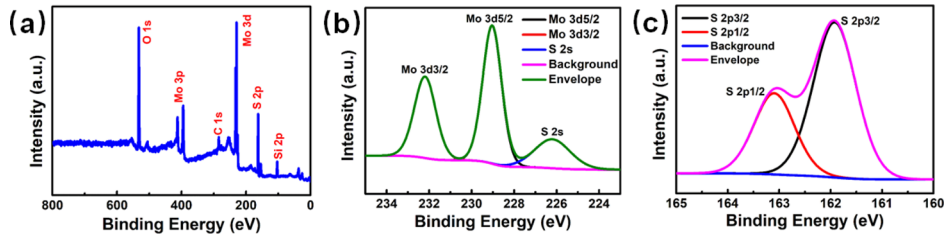

Figure 4. (a) Full range XPS spectrum with the binding energy ranging from 0 to 800 eV. XPS spectra showing the (b) Mo 3d and (c) S 2p core level peaks.

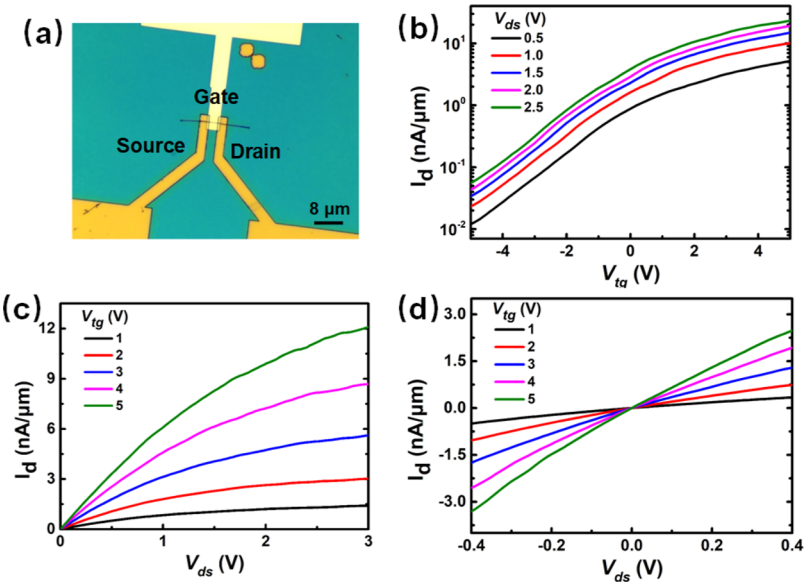

Figure 5. (a) Optical microscopy image of the Ω-shaped gate MoS_2 FET. The channel length is 4 μm. (b) Transfer and (c) output characteristics of the device. (d) I_d−V_{ds} curves at a small V_{ds} level.

peaks observed at 378.178 and 403.742 cm^{-1} correspond to the E^1_{2g} and A_{1g} modes of the MoS_2 film, respectively, representing a well-crystallized MoS_2 film on the SiO_2 nanowire surface. It should be noted that no Si peak was observed from the Raman spectra in Figure 3d, which means that the Raman signals are obtained from MoS_2 surrounding the SiO_2 nanowire, instead of the planar substrate underneath. In addition, both the E^1_{2g} and A_{1g} modes of the SiO_2/MoS_2 core−shell nanowires exhibit a red-shift of ∼4 cm^{-1} compared to that of MoS_2 on the planar SiO_2/Si substrate (Figure 3b), which can be attributed to the 3D cylindrical geometry of the core−shell structure affecting the vibration modes of atoms in the MoS_2 lattice.

The chemical bonding and stoichiometric properties of the MoS_2 films obtained with 40 ALD cycles are studied by X-ray photoelectron spectroscopy. The full spectrum with the binding energy ranging from 0 to 800 eV is displayed in Figure 4a. Figure 4b,c shows the Mo 3d and S 2p core level spectra of the MoS_2 film, respectively. In Figure 4b, the peaks at 232.19 and 229.03 eV correspond to Mo $3d_{3/2}$ and Mo $3d_{5/2}$ core levels, respectively.[18,21] In addition, the relatively weaker peak at 226.20 eV is assigned to the S 2s core level. As shown in Figure 4c, the S 2p core level spectra exhibit two peaks at 163.09 and 161.92 eV, which are ascribed to the S $2p_{1/2}$ and S $2p_{3/2}$ core levels of the Mo−S bonding of MoS_2.[18,21] The calculated atomic ratio of S/Mo is 2.11:1, exhibiting excellent stoichiometry of the MoS_2 film deposited by ALD-based techniques.

By transferring the prepared SiO_2/MoS_2 core−shell nanowire heterostructure onto another SiO_2/Si substrate, we have further fabricated MoS_2 FET devices with an Ω-shaped gate by forming the source/drain electrodes followed by depositing HfO_2 and Ti/Pt layers as the gate dielectric and the gate electrode, respectively (see Experimental Methods for details). To evaluate the electrical performance of the Ω-shaped gate MoS_2 FETs, the electrical measurements were performed at room temperature in an ambient atmosphere using a probe station with a Keysight 4200 semiconductor parameter analyzer. Figure 5a shows the optical microscopy image of an Ω-shaped top-gate MoS_2 FET with 4 μm channel length, and the diameter of the core−shell nanowire is ∼149 nm. The typical transfer characteristics (drain current vs top-gate voltage, I_d−V_{tg}) of the device are shown in Figure 5b, for V_{ds} values ranging from 0.5 to 2.5 V with a 0.5 V step (where V_{ds} is the voltage between the drain and the source). No ambipolar behavior is observed. The I_d−V_{tg} curves show a typical n-type FET behavior with an on/off current ratio of ∼4.3×10^2. As compared to the performance of the reported MoS_2 FETs fabricated on a planar sapphire substrate, the relatively small on/off ratio obtained here is largely due to the SiO_2/MoS_2 interface with a larger lattice mismatch[38] and the contamination introduced during the wire transfer process. Nevertheless, the >10^2 on/off ratio is still sufficient for effective switching in nanoelectronic devices. The output characteristics are illustrated in Figure 5c under five different V_{tg} values. Smooth I_d−V_{ds} curves have been observed. Furthermore, as

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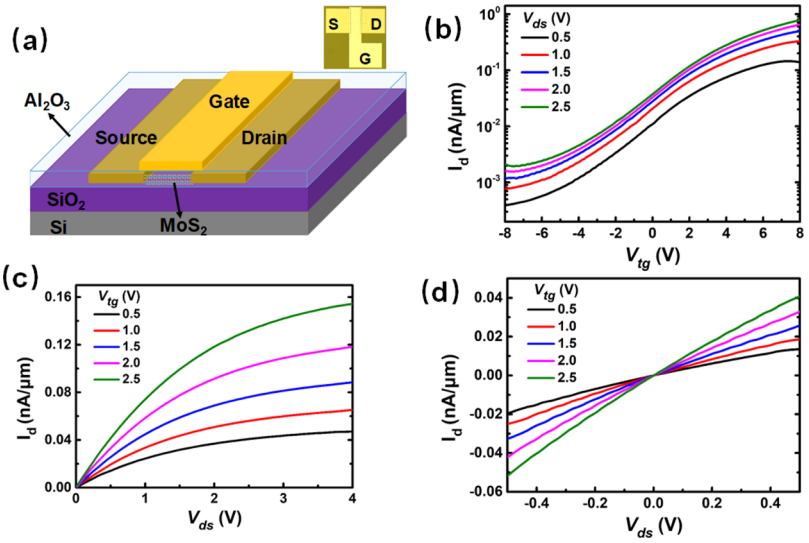

Figure 6. (a) 3D schematic structure of the top-gate FET with planar channel geometry fabricated on a SiO_2/Si substrate. The inset (top right) is the optical image of a fabricated device. (b) Transfer and (c) output characteristics of the MoS_2 FET with 30 μm channel length and 40 μm channel width. (d) I_d–V_{ds} curves at a small V_{ds} level.

shown in Figure 5d, the linear dependence of I_d on V_{ds} at a small V_{ds} level indicates the negligible series resistance at the source and drain.

The field-effect mobility μ_{FE} of the MoS_2 FET is further extracted from the linear regime of the I_d–V_{tg} curves (Figure 5b) using the following equation

$$\mu_{FE} = \frac{\partial I_d}{\partial V_g} \times \frac{L}{WC_{ox}V_d} \quad (1)$$

where L is the channel length, W is the channel width, $C_{ox} = \varepsilon_r\varepsilon_0/t_{ox}$ is the gate dielectric capacitance per unit area, $\varepsilon_r = 15$ is the dielectric constant of the gate dielectric layer, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum dielectric constant, and $t_{ox} = 30$ nm is the thickness of the gate dielectric layer. The calculated field-effect mobility of this Ω-gate MoS_2 transistor is 0.02 $cm^2\ V^{-1}\ s^{-1}$. We have fabricated multiple Ω-gate MoS_2 FET devices in our study, and a similar electrical performance has been achieved from other devices (Figure S4), suggesting the reproducible fabrication process of the MoS_2 FET with an Ω-shaped gate as well as good homogeneity of the ALD-based MoS_2 synthesis.

For comparison, a top-gate MoS_2 FET with planar channel geometry was also fabricated on a conventional SiO_2/Si substrate by the same ALD-based MoS_2 synthesis. Figure 6a shows the 3D schematic structure of the top-gate MoS_2 FET with a 25 nm Al_2O_3 gate dielectric layer. The transfer and output characteristics of the MoS_2 FET with 30 μm channel length and 40 μm channel width are displayed in Figure 6b,c, respectively. N-type FET transport behavior has also been observed. The on/off current ratio and the room-temperature mobility are ~3.5×10^2 and 0.01 $cm^2\ V^{-1}\ s^{-1}$, respectively. In addition, the good metal contacts at the source and drain are confirmed by the I_d–V_{ds} curves in Figure 6d. In comparison, the electrical performance of Ω-shaped gate MoS_2 FETs is comparable to that of the MoS_2 FET with planar geometry. Although the electrostatic gate control of the channel in the Ω-gated device is expected to be improved, the electrical performance did not exhibit clear superiority over the MoS_2 FET in planar geometry. By comparing the I–V curves shown in Figures 5 and 6, the Ω-shaped FET exhibited a higher off-state current, but a larger on-state current, as compared to the planar device. We attribute the relatively high off-state current to the contamination at the surface of the SiO_2/MoS_2 core–shell nanowires, which was introduced during the wet transfer process. Such contamination can lead to a large number of channel/dielectric interface traps, which are generally positively charged resulting in a higher off-state current. Moreover, the switching behavior of the device can also be degraded because of the existence of interface traps. Although the electrical performance of the MoS_2 FET needs to be improved by further engineering of material processing and device fabrication, our work provides a promising solution for the future nanoelectronic applications of MoS_2 in 3D devices and systems.

CONCLUSIONS

In summary, we have successfully demonstrated the design and fabrication of MoS_2 FETs with an Ω-shaped gate based on the SiO_2/MoS_2 core–shell nanowire heterostructure, which is achieved by uniformly depositing a few-layer MoS_2 film on the surface of the SiO_2 nanowire using ALD technique. Such a device structure is a good example showing great potential for the ALD-based synthesis of the novel TMD semiconductors extending to a wider scope of nanoelectronic devices with advanced non-planar device geometry. The electrical characterization has shown that the Ω-gate MoS_2 FET has an n-type transport behavior with an on/off current ratio of ~10^2 and a field-effect mobility of ~0.02 $cm^2\ V^{-1}\ s^{-1}$, which are comparable to the MoS_2 FET with planar channel geometry built on a SiO_2/Si substrate. We believe that our work enables a promising strategy to further exploit unique materials properties of the novel TMD semiconductors through the implementation of novel 3D nanoelectronic devices.

EXPERIMENTAL METHODS

MoS_2 Film Synthesis. A Beneq TFS-200 ALD system was employed to carry out the growth of the MoS_2 film in our study. Molybdenum(V)chloride ($MoCl_5$) and hexamethyldisilathiane (HMDST) were used as a molybdenum source and a sulfur source,

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respectively. The temperatures of $MoCl_5$ and HMDST precursors were set to 120 and 25 °C, respectively, to ensure sufficient vapor pressure. N_2 was used as a carrier gas. The typical ALD process for one deposition cycle is as follows: pulse $MoCl_5$ for 4 s, purge N_2 for 8 s, pulse HMDST for 1 s, and purge N_2 for 5 s (Figure S5a). The deposition temperature was set to 400 °C. To improve the crystallinity and reduce the defects, the as-grown MoS_2 film was annealed under a sulfur atmosphere. The MoS_2 sample was placed at the center of a horizontal quartz cube furnace with sulfur powder (0.6 g, 99.999%) placed at the upstream end (30 cm away from the MoS_2 sample) (Figure S5b). Ar (8 sccm) was used as a carrier gas. The center region was heated to 900 °C for 30 min, then kept for 1 h before naturally cooling down to room temperature. Additionally, the comparison of the Raman results of the as-grown and annealed MoS_2 films is shown in Figure S6.

Fabrication of SiO_2/MoS_2 Core−shell Nanowires. The Si substrate covered with thermally oxidized SiO_2 was first cleaned sequentially with acetone, isopropyl alcohol, and deionized water. Then, an Au catalyst film (~2 nm) was deposited on the SiO_2/Si substrate by sputtering. The Si nanowires were grown following the VLS mechanism[39] in a LPCVD furnace at 450 °C for 2.5 h in an ambient SiH_4 stream. The nanowires are ~30 μm in length. The nanowire diameter is within a range of 10−200 nm. After the Si nanowire growth, the wires were thermally oxidized at 1000 °C for 160 min in a CVD furnace to form the SiO_2 nanowires. After that, the MoS_2 layer was uniformly deposited on the surface of SiO_2 nanowires using the ALD-based method described above forming the SiO_2/MoS_2 core−shell heterostructure.

Fabrication of Ω-Gate MoS_2 FETs. After the formation of the SiO_2/MoS_2 core−shell heterostructure, the nanowires were suspended in isopropyl alcohol solvent by an ultrasonic method and transferred onto a 300 nm SiO_2/Si substrate. The source and drain contacts were defined by electron-beam lithography and formed by the deposition of Ti/Pt (10/70 nm) metal using sputtering and lift-off processes. A thin Al_2O_3 layer (~2 nm) was then deposited by electron-beam evaporation (EBE) on the MoS_2 channel film as a seeding layer for the subsequent dielectric deposition.[40] Afterward, a layer of 30 nm HfO_2 was deposited as a top-gate dielectric by ALD at 300 °C with TDMAH and H_2O as precursors. Finally, the gate electrode (10 nm Ti/70 nm Pt) was patterned and formed using a similar fabrication process as the source/drain contacts. Because the SiO_2/MoS_2 core−shell nanowires are laterally located on the surface of the substrate, the gate dielectric and the gate metal electrode cannot be deposited uniformly surrounding the nanowire. As a result, the gate structure formed was in Ω-shape.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.9b21727.

Thickness of the MoS_2 film measured at four different locations in the cross-sectional TEM image of Ω-gate FETs, XRR result of the MoS_2 film deposited on a planar SiO_2/Si substrate, SEM images of the MoS_2 nanotubes obtained by etching the SiO_2 core, characterization of another two MoS_2 FETs with an Ω-shaped gate, ALD-based synthesis of the MoS_2 film, and Raman spectra of the as-grown and high-temperature annealed MoS_2 film on a SiO_2/Si substrate (PDF)

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Notes

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