# Radio frequency reliability studies of CMOS RF integrated circuits for ultra-thin flexible packages

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This Letter presents for the first time radio frequency (RF) reliability studies of fully integrated CMOS RF integrated circuits (RFICs) for next generation wireless communication applications involving conformal bodies where wireless communication RFICs will be embedded on ultra-thin flexible packages. As a test case, RF characteristics of a CMOS voltage-controlled oscillator (VCO) chip with multiple die-substrate thicknesses were measured and results are analysed. The CMOS VCO chip under study was designed and fabricated using 180 nm RF-CMOS process. Reliability of performances of the VCO chips are characterised and results are compared before and after die thinning from 250 to 50, 35, and 25 µm, respectively. Critical RF performance parameters such as frequency of oscillation, output power, and phase noise are considered for analysis, respectively. All the dies are placed face-up for probing on the top of a metal chuck with ground connection inside the micro-chamber of a probe station. While the deviations of frequency and output power are within ±1% and ±1 dB, respectively, due to the die thinning affect, the phase noise deteriorations are observed significant. It confirms the well-known fact of phase noise sensitiveness to the substrate thickness due to the leakage and SOI CMOS is discussed widely to minimise these parasitic effects.

*Introduction:* Next-generation electronic products are pushing the semiconductor industry to integrate more ultra-thin and flexible integrated circuits (ICs). Ultra-thin and flexible ICs promote more efficient and cost-effective solutions that impact many applications like wireless communications, wearable electronics, Internet of Things, and healthcare monitoring. One of the main challenges of realising flexible and ultra-thin ICs is the effect of die-substrate thinning on RF performances of an IC.

There are lot of challenges involved in realising extremely thin ICs are due to the necessity of highly precise handling process of the ultra-thin ICs and probable electrical performance degradation as a result of die-substrate thinning [1]. The active regions of an extremely thin IC could be damaged due to ultra-thinning and subsequently adversely affect the overall performance of the ICs [2]. Most of the previous works [2–4] show the different aspects of IC substrate thinning, but only down to 40 µm. Most of them focus on electrostatic discharge performance [2], thermal characterisation, and modelling of ultra-thin chips [5]. Though in [6], the effects of reducing substrate thickness on an RF transformer are analysed, the impact of substrate thinning on overall RF performances of a fully integrated RFIC was never investigated before.

This Letter presents RF performance reliability studies of CMOS RF integrated circuits (RFICs) chips with various die thicknesses down to 25 µm for ultra-thin flexible electronic applications for the first time to the best of authors' knowledge. As a test case, fully integrated voltage-controlled oscillator (VCO) chips, designed and fabricated using 180 nm CMOS process, were used to perform the study and analysis. The impact on important VCO parameters such as operating frequency, RF output power, phase noise, and DC performances due to die-substrate thinning was studied through measurement in this work.

*Thinning and characterisation of VCO chips:* The standard die-substrate thickness of CMOS process is 250–300 µm [7]. Fig. 1 demonstrates a layer map for 1-poly 6-metal 180 nm CMOS process technology, which has a substrate thickness of 250 µm. In order to study RF reliability of CMOS RFIC for ultra-thin flexible electronic applications, an LC cross-coupled VCO was considered with differential output to provide better noise performance and even-harmonic cancellation. In order to accommodate die-to-die variations and some measurement error, 20 VCO chips have been used before and after thinning the die-substrate thickness in this study. Variations of measured results between dies with same thickness are averaged out. In first step, 20 VCO chips with default die-substrate thickness of 250 µm are characterised with respect to RF performances, in particular, frequency tuning range, RF output power, and phase noise. In second step, 20 VCO chips are thinned and diced into four different die-substrate thickness tiers as follows: five chips with substrate thickness of 50 µm, five chips with substrate thickness of 35 µm, five chips with substrate thickness of 25 µm, and five chips with substrate thickness of 15 µm. All of the thinned dies are mounted on a thermal-release wafer tape, each having a temporary handle attached, and ready to be assembled with ultra-thin ICs [8].

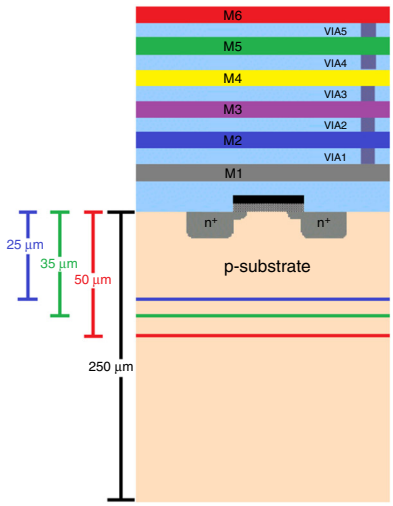


**Fig. 1** *Layer map for 1-poly 6-metal 180 nm CMOS process technology (the figure is not to the scale)*

Fig. 2*a* shows schematic of the VCO integrated with buffer stage. Two diode-connected NMOS transistors (TN3 and TN4) are used as variable capacitors for tuning the frequency. A common-source buffer is used in order to provide output isolation needed to improve frequency stability of VCO, and also 50 Ω output impedance matching [9].

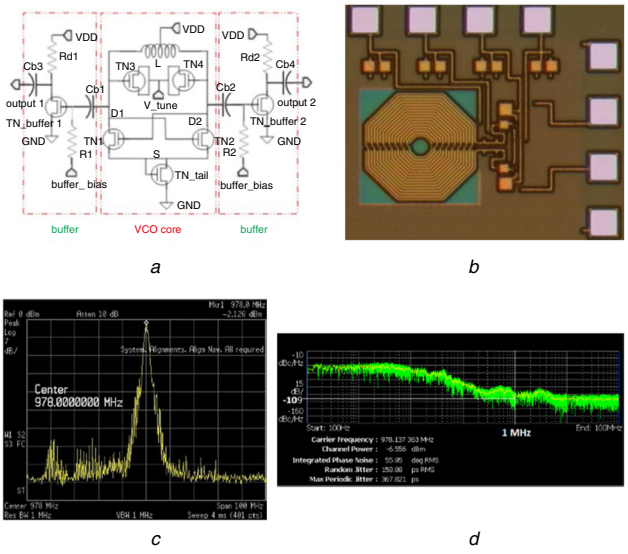


**Fig. 2** *CMOS VCO characterisation with default die-substrate thickness of 250 µm*

*a* Circuit schematic
*b* Die photo
*c* RF output power spectrum
*d* Phase noise

*Results and discussions:* All the VCO chips were characterised using a *Tektronix RSA3408B* spectrum analyser. Fig. 2*b* shows the die photo of the fabricated VCO chip using 180 nm CMOS process. Total size of the VCO chip with buffer is 0.738 mm × 0.606 mm including DC and RF bond-pads [9]. Before die-substrate thinning, 20 VCO chips with substrate thickness of 250 µm were characterised with respect to frequency tuning range, RF output power, phase noise, and DC parameters. Fig. 2*c* shows single-ended output power of the VCO chip with default

die-substrate thickness of 250 µm. The RF output power was measured to be 0.62 dBm at the frequency of 978 MHz after de-embedding a cable loss of 1.5 dB. In addition, Fig. 2*d* demonstrates phase noise of the VCO measured at 1 MHz offset from the centre frequency of 978 MHz, and the value is −109 dBc/Hz. Therefore, the average of those data is set as a reference for each performance parameter. Die-substrate thickness factor ($X$) is defined in (1) in order to have a better representation of data to compare the effect of different die-substrate thickness on the measured RF parameters

$$X = \log(T)/\log(T_0) \tag{1}$$

where $T$ is the die-substrate thickness of chip in µm, and $T_0$ is the default die-substrate thickness of 250 µm. Fig. 3 shows normalised frequency deviation of VCO chips versus die-substrate thickness factor ($X$). It is observed that the operating frequency of VCO chip deviates <1% for die-substrate thickness >25 µm. The frequency tuning range of the VCO chips over tuning voltage 0–3.5 V for different die-substrate thickness was studied, which is demonstrated in Fig. 4. It is observed that the frequency tuning range remains fairly unyielding for a substrate thickness of 25 µm and above. Fig. 5 illustrates normalised RF output power deviation of VCO chips versus die-substrate thickness factor of $X$. It is observed that RF output power increases by 0.5 dB for substrate thickness of 50 µm, by 1 dB for 35 µm and by 1.1 dB for 25 µm, which indicates good feasibility towards flexible electronic applications realisation. Fig. 6 demonstrates phase noise of VCO chips for different substrate thickness. It is observed for die-substrate thickness >25 µm, the deviation is <15 dB from the VCO phase noise with default die-substrate thickness of 250 µm. The degradation was thought mainly due to the reduced quality factor ($Q$) of the circuit components as a result of ultra-thinning [6]. It is also well-known that phase noise can be very sensitive to the die-substrate thickness due to the leakage to the substrate. The DC parameters for VCO chips for different die-substrate thicknesses are summarised in Table 1, which shows that the DC parameters remain fairly similar for different substrate thicknesses. The DC parameters of 20, 5, 5, and 5 chip samples were measured for die-substrate thickness of 250, 50, 35, and 25 µm, respectively, to calculate the average and standard deviation for the VCO and buffer drain currents. To reinforce the validity of this reliability study, five VCO chips with substrate thickness of 15 µm were also characterised. However, during the characterisation the chips cracked while probing, which indicates a limitation for minimum realisable die-substrate thickness.

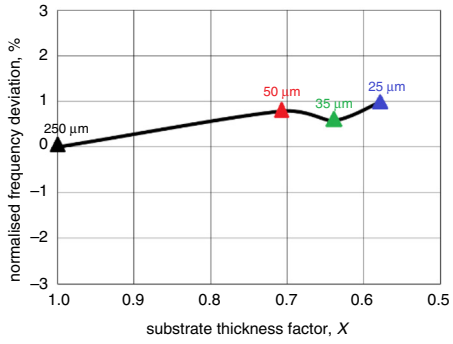


**Fig. 3** *Normalised frequency deviation of VCO chips versus die-substrate thickness factor (X)*

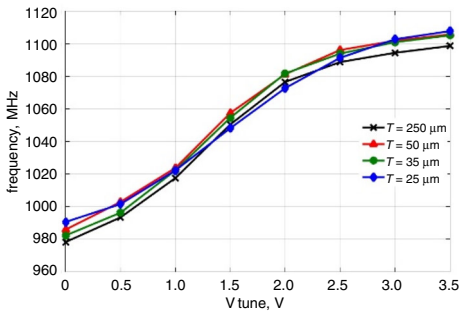


**Fig. 4** *Frequency tuning range of the VCO over tuning voltage for different die-substrate thickness*

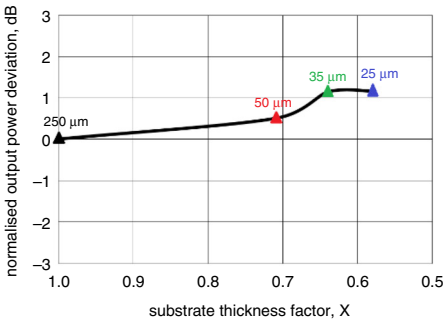


**Fig. 5** *Normalised RF output power deviation of VCO chips versus die-substrate thickness factor (X)*

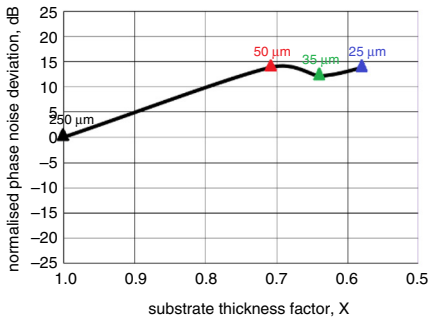


**Fig. 6** *Normalised phase noise deviation of VCO chips versus die-substrate thickness factor (X)*

**Table 1:** Comparison of DC parameters for VCO chips for different die-substrate thickness

| Substrate thickness (µm) | VCO drain current | | Buffer drain current | |
|---|---|---|---|---|
| | Average (mA) | Standard deviation ($\sigma$) | Average (mA) | Standard deviation ($\sigma$) |
| 250 | 5.08 | 0.13 | 19.47 | 0.27 |
| 50 | 4.64 | 0.26 | 19.73 | 0.17 |
| 35 | 4.73 | 0.06 | 20.30 | 0.09 |
| 25 | 4.50 | 0.10 | 19.70 | 0.11 |

*Conclusion:* Reliability studies on RF performances of a fully integrated CMOS RFIC for ultra-thin flexible electronic applications are presented for the first time to the best of authors' knowledge. The impact on RF performances such as frequency range, RF output power variation, phase noise variation, and DC parameters due to die-substrate thinning of a CMOS VCO, designed and fabricated in 180 nm CMOS process, was observed and measured results were analysed as a test case. The thinning process affected the performances of the VCO such as oscillation frequency and output power within an accepted range for most of the applications where VCOs will be integrated into the RFIC for wireless communication application. The phase noise degradation was observed to be significant. This needs to be addressed at the chip level either by choosing SOI CMOS where substrate will be isolated from the active circuits or by using shielded dummy metals fills while doing RFIC layout so that active circuits shielded more from the bulk CMOS substrates.

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One or more of the Figures in this Letter are available in colour online.

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