Multi-probe Two-Dimensional Mapping of Off-State Degradation in DeNMOS Transistors: How and Why Interface Damage Predicts Gate Dielectric Breakdown

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Abstract

Through a combination of measurements techniques, we show that the generation of both interface and bulk traps during off-state stress in drain extended NMOS transistors are driven by the same physical mechanism and as such have similar time and voltage dependencies. We also show that the peak interface damage location (obtained from charge pumping measurement) along with asymmetric percolation model successfully interpret the observed Weibull slope of dielectric breakdown during off-state stress. Our analysis suggests the intriguing possibility of replacing time consuming off-state TDDB measurements by simple charge pumping analysis.

Introduction

Device dimension and supply voltage (V_{DD}) for core logic transistors have been scaled dramatically since the 1980s, but those of the I/O transistors (e.g. DeNMOS, LDMOS, *etc.* [1]-[3]) have not. For an I/O transistor, the geometry is constrained by the core process and the operating voltages by interface requirements to outside world. As such, it is not surprising that the unique reliability issues of I/O transistors often cannot be reduced to elementary combinations of classical mechanisms of HCI, NBTI, TDDB, *etc.* For example, while Drain extended NMOS (DeNMOS) degrades under *off-state* hot-carrier (HCI) stress (V_G=0, V_D>5V), but it fails by gate dielectric breakdown (TDDB) [4]. Classical literature – unfortunately – provides no guidance for reliability projection under such correlated breakdown.

In this paper, we use a wide variety of (characterization) probes to stitch-together a two-dimensional map of defect generation N(x,y,t) for a DeNMOS transistor under off-state stress. This analysis shows that for these transistors, both N_{IT} (HCI-related damage) and N_{OT} (leading to TDDB) correlate well because they share common generation mechanism, and that the voltage-acceleration of N_{IT} (γ_{NIT}) is an excellent and unambiguous predictor for voltage-acceleration of TDDB ($\gamma_{TDDB} \equiv \gamma_{NOT}$). Moreover, we use the voltage-ratio and current-ratio [5] methods to locate the gate dielectric breakdown spots outside the gate-edge (co-located with the peak N_{IT} generation) and use the corresponding asymmetrical percolation model to interpret observed TDDB Weibull slope (β). Since both γ_{TDDB} and β can be determined by the N_{IT} measurements, *our analysis for the first time explains how and why N_{IT} can be used as an inexpensive and fast predictor of TDDB for correlated off-state degradation in DeNMOS transistor.*

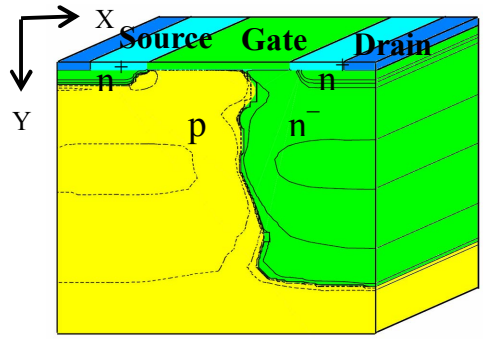

Fig.1. Device structure of drain extended NMOS transistor.

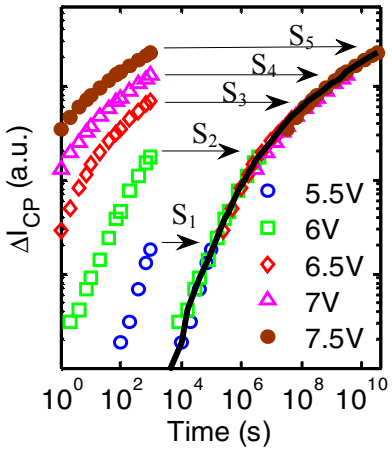

Fig.2. Interface damage measured by CP during off-state stress (V_G=0V, V_D>5V). Individual degradation curves can be scaled laterally to form a universal curve [6].

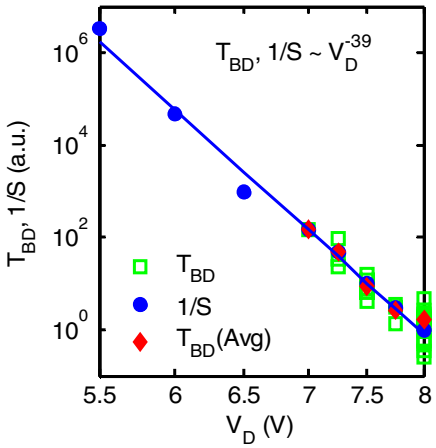

Fig.3. Voltage accelerations for N_{IT} and TDDB lifetime show excellent correlation. This is possible *if and only if* both N_{IT} and N_{OT} have similar generation kinetics.

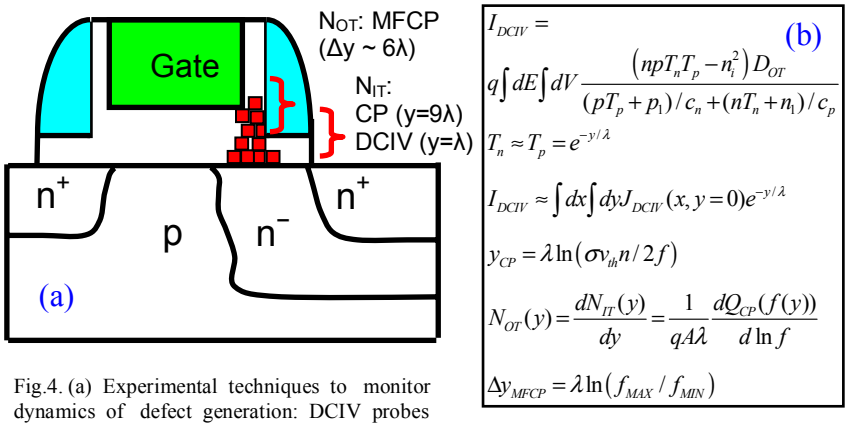

Fig.4. (a) Experimental techniques to monitor dynamics of defect generation: DCIV probes near-interface traps; N_{IT}=N(x,y≈0,t). CP (f=800kHz) measures integrated trap density within the scanning length y_{CP}; N_{IT}=∫N(x,y,t)dy. Multi-frequency CP (f_{MIN}=5kHz, f_{MAX}=2MHz) measures bulk traps within the scanning width Δy_{MFCP}; N_{OT}=N(x,y,t). (b) Relevant equations; $T_{n,p}$ are tunneling probabilities, $c_{n,p}$ are capture rates, n, p are surface carrier concentration, λ is tunneling length, σ is capture cross section, v_{th} is thermal velocity, f is CP frequency, Q_{CP} is charge pumped per cycle and A is degraded gate area.

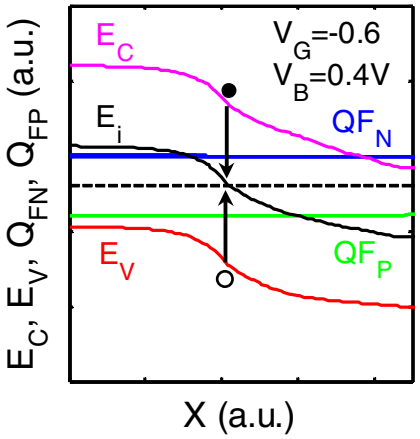

Fig. 5. Energy bands at Si/SiO_2 interface for DCIV bias conditions. Recombination rate maximizes when average of quasi Fermi levels intercept mid-gap level. This location shifts laterally with applied V_G, and enables lateral profiling of N_{IT}.

TDDB Voltage Acceleration through N_{IT}/N_{OT} Correlation

Fig. 2 shows the time evolution of N_{IT} for various stress biases, and demonstrates that the underlying degradation is universal [6]. It was shown previously that N_{IT} damage is driven by hot carriers generated through impact ionization of surface band-to-band tunneling current and that N_{IT} is due to broken ≡Si-O bonds and not due to broken ≡Si-H [6]. As such, one might anticipate that the bulk-N_{OT} generation – also due to broken ≡Si-O bonds and responsible for TDDB – might be related to N_{IT} generation. To test this hypothesis, Fig. 3 plots the voltage acceleration factors (γ_{NIT}) obtained from the scaling factors used to obtain universal degradation curve [6], along with the TDDB lifetime. Indeed, γ_{TDDB} appears to be *perfectly* correlated to γ_{NIT}. This is only possible if both N_{IT} and N_{OT} have similar kinetics. Checking if it is indeed the case is not trivial, however, because no simple technique probes N(x,y,t) at various depths within the gate dielectric simultaneously. As such we must map the spatio-temporal dynamics of defect generation using a collage of snapshots from space-resolved DCIV [7] to probe N_{IT}=N(x,y≈0,t), space-resolved classical CP [8] to probe near-interface *integrated* N_{OT}, *i.e.* N_{IT}=$\int_0^{y\approx 7Å}$N(x,y,t)dy, and multi-frequency CP (MFCP) [9] to probe deep N_{OT}=N(x,y≈7-12Å,t) (see Fig. 4).

Specifically, the surface recombination current measured by DCIV is proportional to N_{IT} at peak recombination location (see Fig. 5). Fig. 6 shows the time evolution of peak DCIV current (corresponding to peak N(x,y≈0,t)), and exhibit universal behavior similar to CP current. The peak recombination location shift laterally with applied gate bias, and can be used to obtain spatial profiling of N_{IT}. Fig. 7 shows the N_{IT} profile obtained from DCIV and CP measurements, and both techniques consistently identify

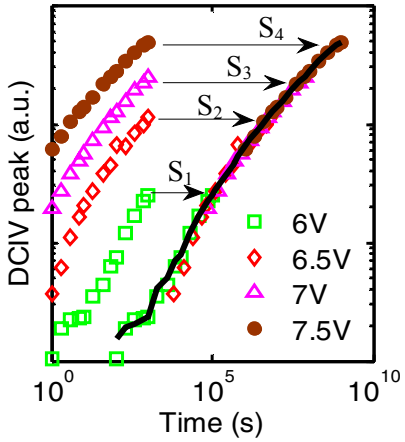

Fig. 6. Time evolution of peak DCIV current exhibit universal behavior similar to CP. This suggests similar generation kinetics for near-interface traps probed by DCIV and deeper traps probed by CP.

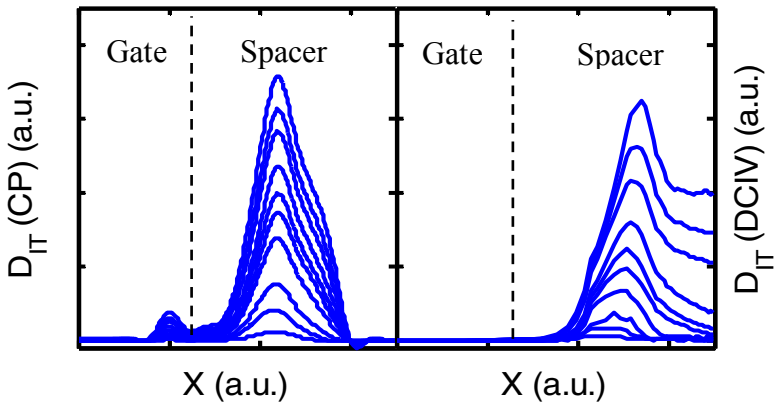

Fig. 7. Spatial N_{IT} profile at various stress times from CP and DCIV measurements. Both techniques are in good agreement and locate peak interface damage outside the gate edge. DCIV show *absolutely no* N_{IT} in the gate region, while CP shows a small hump, possibly from traps lying deeper in the oxide (see Fig. 15).

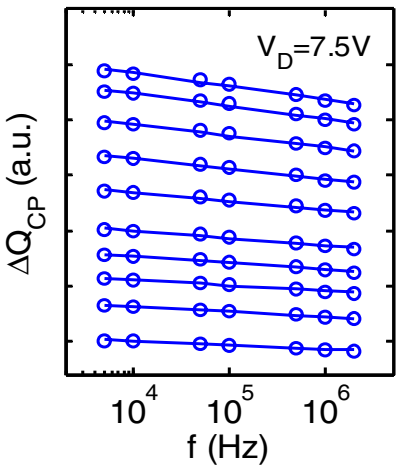

Fig. 8. Charge pumped per cycle vs. frequency at various stress times. Straight line fit implies uniform N_{OT} in the scanned width. N_{OT} is proportional to slope of the straight line fit and increases with stress time.

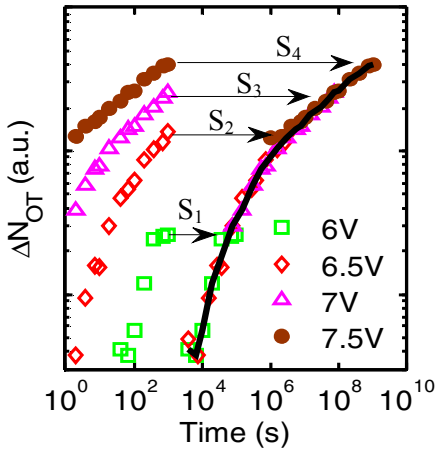

Fig. 9. N_{OT} values obtained from MFCP exhibit universal behavior similar to CP and DCIV. This suggests similar generation kinetics for both N_{IT} and N_{OT}.

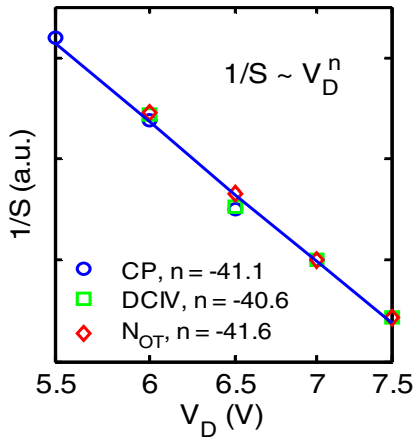

Fig. 10. Voltage acceleration for N_{IT} and N_{OT} obtained from universal scaling factors. Similar time and voltage dependence for both N_{IT} and N_{OT} indicates similar generation mechanism.

the peak N_{IT} generation to occur outside the gate edge. N_{OT} generation probed using MFCP (see Fig. 8) also shows a universal behavior similar to CP and DCIV measurements (Fig. 9). Moreover, voltage acceleration factors γ_{NIT} and γ_{NOT} from various measurements techniques show a *perfect* correlation (Fig. 10). Similar time and voltage dependence for N_{IT} and N_{OT} proves similar generation mechanism for both, and explains why γ_{NIT} can be used as a predictor for γ_{TDDB}.

Weibull Slope

While the agreement of voltage acceleration of TDDB and N_{IT} is now understood, the interpretation of the Weibull based on classical percolation model [10] is unsatisfactory (Fig. 11). Specifically, given that Tox≈26A, and time exponent of trap generation n=0.16, the Weibull slope β=1.66 requires trap-size of 2A, an unphysical result. To resolve this puzzle we begin by noticing a curious feature of the N_{IT} generation, i.e. the peak N_{IT} generation occurs outside the gate edge (see Fig. 7). If N_{IT} and N_{OT} are correlated, then the breakdown spot (X_{BD}) must also be located in spacer region. We used voltage-ratio (VR) and current ratio (CR) methods (see Fig. 12, 13) for a number of devices to prove that this is indeed the case, as shown in Fig. 14. Now since the BD spots remain outside the gate edge, the classical homogenous percolation model [10], [11] must be generalized to include the formation of asymmetric path that proceeds along the local field and terminates in the poly-silicon (Fig. 15). As shown in Fig. 16, a percolation model based simulation of such damage profile could successfully interpret the observed Weibull characteristics. Apart from the theoretical consistency with Weibull slope, the absence of N_{IT} in gate region for DCIV measurement (but present in CP as a possible reflection of N_{OT}, see Fig. 15) also suggests a meandering percolation path from spacer to gate.

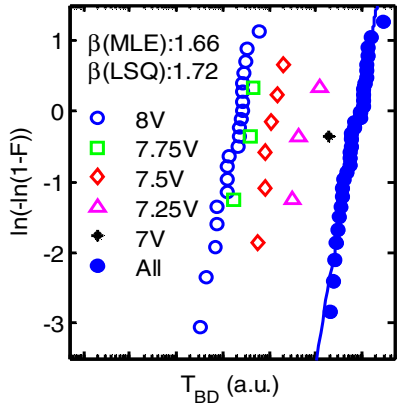

Fig. 11. T_{BD} distribution for various stress biases. Individual curves were combined using γ_{NIT} to obtain β. Percolation model simulation required unphysical a=2A value for breakdown path in the gate oxide region.

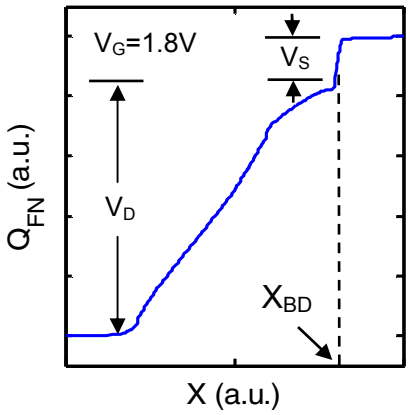

Fig. 12. Potential profile along the channel at VR measurement bias. For a non-uniform device with series resistance degradation, potential profile is non-linear, and a full simulation is required for accurate X_{BD} determination.

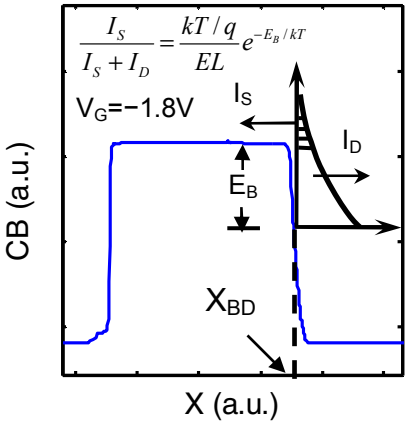

Fig. 13. Conduction band profile at CR measurement bias. Electrons above the barrier diffuse to the source, while the rest drift towards the drain. CR gives the barrier height and hence X_{BD}. E is electric field and L is channel length.

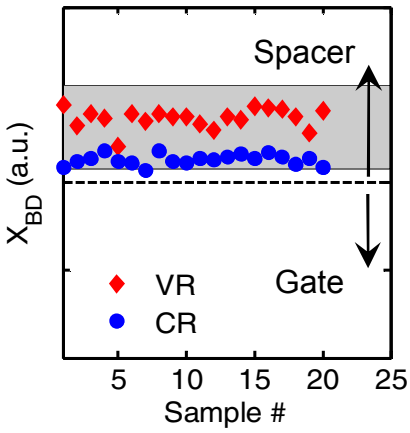

Fig. 14. Both VR and CR methods locate the X_{BD} outside the gate edge (co-located with N_{IT} damage shown by shaded region). Absence of N_{IT} in the gate region suggests that X_{BD} cannot occur in the gate oxide. The small offset between the two techniques might be due the fact that CR strongly weighs injection towards the gate edge, unlike the VR method.

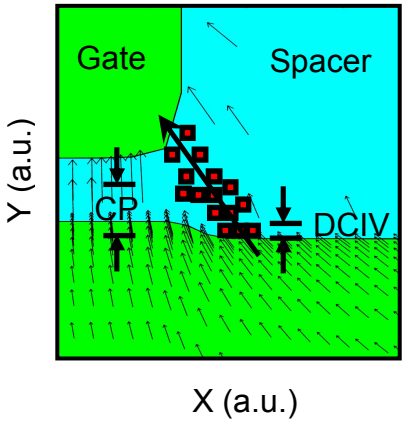

Fig. 15. Possible percolation path during off-state TDDB. Trap generation could follow internal electric field (shown by the arrows) from Si/SiO_2 interface to the gate electrode.

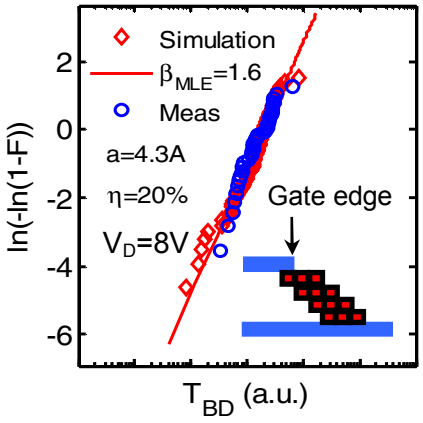

Fig. 16. Non-uniform percolation model interprets the observed β with reasonable value of a=4.3A. This implies that Weibull parameters depend on X_{BD} as well as T_{OX}.

Conclusion

We find that γ_{NIT} measures γ_{TDDB} and the location of the N_{IT} peak – along with asymmetric percolation – determines β. Hence, a complete characterization of asymmetric *off-state* TDDB failure can be reduced to measurement of N_{IT} and as such provides – for the first time – a new method for reliability projection for correlated degradation of HCI and TDDB.

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