Reconfigurable hardware implementation of BinDCT

C.W. Murphy and D.M. Harvey

Enhancing the coding gain and operand throughput of a data compression application through dynamic hardware reconfiguration is described. A novel implementation of the BinDCT, a discrete cosine transform (DCT) approximation, has been realised on a run-time reconfigurable custom XC6200 field-programmable gate-array-based dynamic coprocessor, coupled to a TMS320C40 digital signal processor system.

Introduction: Xilinx XC6200 field-programmable gate arrays (FPGAs) are one of a few devices that can exhibit dynamic run-time reconfigurable (RTR) properties. The Xilinx XC6200 FPGAs have a FastMAP™ interface that facilitates partial reconfiguration [1]. While this occurs, unaffected regions of the FPGA remain active, enabling them to exhibit virtual hardware characteristics [2]. Virtual hardware can increase the computational density by reusing and redeploying FPGA hardware resources dynamically during run-time.

The design of the BinDCT [3] algorithm has provided an application most suited for this technology. Using XC6264 FPGAs, a dynamic coprocessor implementation has been designed that demonstrates the feasibility of using RTR hardware to enhance system performance [4].

BinDCT algorithm: The BinDCT is a multiplier-less fixed-point-friendly approximation of Chen's fast discrete cosine transform (DCT) [5] implementation. Within the BinDCT Chen DCT type butterflies and plane rotations have been replaced by a series of dyadic lifting steps. Lifting steps can be considered as scaling and addition operations using integer fix-point implementation-friendly values.

A characteristic of lifting steps is that an input can be reconstructed from an output response without error if identical coefficient values are used in both operations. Using this property, nine dyadic lifting step configurations were developed [3], known as BinDCT-C1 to BinDCT-C9. Each generated an approximation of the DCT algorithm, having varying degrees of accuracy. The respective processing complexity of each BinDCT configuration (BinDCT-C1 to BinDCT-C9) reduced as the DCT approximation error increased.

Research: BinDCT configurations were evaluated using Ramp, DC level, Mexican Hat, Unit Step, and Impulse input functions. Results obtained indicated that BinDCT root mean square error (RMSE) was dependent upon the configuration used and the frequency content of the inputs [4].

Forward BinDCT approximations generated the largest MSEs. For an input coefficient range from 0 to 255 the maximum RMSE of an 8-bit forward BinDCT (FBinDCT-C9) was 70.8 for a step input function, and less for other inputs. The reverse BinDCT transforms' RMSEs were very small (typically 2.2 × 10⁻⁶) and considered negligible. This can be attributed to the loss-less data reconstruction characteristics of lifting ladders, with numerical error due to finite word lengths only to blame. Results concluded that BinDCT-C9 achieved the greatest inherent data redundancy of all nine configurations while also exhibiting the greatest RMSEs.

To investigate the DCT coding gain, the most accurate (BinDCT-C1) and least accurate (BinDCT-C9) BinDCT configuration forward transform coefficients were used. For high frequency input data, higher compression ratios were obtained using BinDCT-C1 compared to BinDCT-C9. Paradoxically, for low frequency content inputs BinDCT-C9 generated greater loss-less compression ratios than BinDCT-C1. The design was therefore required to determine which transform configuration generated the most efficient coding gain for each 8 × 8 pixel tile in an image.

The optimal BinDCT configuration used for each input sequence was determined through analysing input data frequency content, which would normally vary within a real-time operation. If the BinDCT configuration remained static, with the input image data-stream frequency content varying, optimal loss-less DCT coding gain and throughput would be unobtainable. This is because the BinDCT configuration most suited to each image tile would not be configured all the time. To correct this and achieve maximum compression all the time, the BinDCT configuration must be updated for each image tile during system operation. This operational notion provided the basis for increasing loss-less compression and operand throughput by using dynamic RTR hardware implementation.

Hardware implementation: Dynamically reconfigurable forward and reverse BinDCT transforms have been constructed using VHDL and implemented on a DSP/dynamic hardware development platform. This consists of a commercial TIM-40 TMS320C40 (C40) parallel processor, custom designed XC6200 FPGA prototype environment, and software development tools [4, 6]. Both systems interact within a host PC, enabling the XC6200 FPGA to be configured as a C40 dynamic RTR coprocessor, and/or inter-node routing and processing engine.

Transforms BinDCT-C1 and BinDCT-C9 have been configured within an XC6264 FPGA functioning as a C40 memory mapped coprocessor. Compared to the latest static FPGA architectures, XC6260 FPGAs suffered from inefficient limited logic and routing resources, but were unique in being dynamically reconfigurable. This restricted BinDCT transform implementation to serial pipeline architectures and forced active transform selection to be conducted within the C40. The XC6264 hardware statistics of transforms BinDCT-C1 and BinDCT-C9 are listed in Table 1.

Table 1: XC6264 BinDCT hardware implementation characteristics

<table>
<thead>
<tr>
<th>BinDCT throughput (at maximum frequency)</th>
<th>Configuration</th>
<th>Maximum frequency</th>
<th>Pipeline full</th>
<th>Pipeline empty</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MHz</td>
<td>ops/s</td>
<td>ops/s</td>
<td></td>
</tr>
<tr>
<td>FBinDCT-C1</td>
<td>5.16</td>
<td>257.7kBinDCT</td>
<td>43.0kBinDCT</td>
<td></td>
</tr>
<tr>
<td>FBinDCT-C9</td>
<td>5.3</td>
<td>265.1kBInDCT</td>
<td>88.3kBInDCT</td>
<td></td>
</tr>
<tr>
<td>RBinDCT-C1</td>
<td>4.5</td>
<td>225.2kBInDCT</td>
<td>37.5kBInDCT</td>
<td></td>
</tr>
<tr>
<td>RBinDCT-C9</td>
<td>4.17</td>
<td>208.4kBInDCT</td>
<td>69.4kBInDCT</td>
<td></td>
</tr>
</tbody>
</table>

Dynamic update of the active BinDCT transform was performed using a novel custom designed 'self-configuration' control mechanism (Fig. 1). A self-configuration controller, and interfaces to the C40 global bus and an external configuration store were designed and run on the XC6264. The BinDCT processor hardware was implemented within the remaining XC6264 coprocessor function area, approximately 77% of the configurable logic cell (CLC) area. RTR was instigated by the C40 through the coprocessors (XC6264) address space. Once RTR commenced, the XC6264 configuration was updated from the 262 kbyte configuration store. This process occurred using partial configuration through the XC6264's FastMAP™ interface independently of the C40 or host PC.

Custom software tools have been developed that reduce the volume of RTR configuration data required. These function by analysing two successive XC6260 configurations to determine the routing and logic changes that occur between them. To switch between transform configurations C1 and C9 requires 6401 (12 ms) and 6751 (12.5 ms)

Hongya Liao, M.K. Mandal and B.F. Cockburn (Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada)

References
Using this dynamic technique an additional 1956 (Dynamic BinDCT–True DCT) forward transform coefficients generated were at zero compared to the respective static configuration versions (BinDCT-C1: 38777, BinDCT-C9: 3335, True DCT: 38899, Dynamic BinDCT: 40855). This gave a DCT coding gain of 5%.

For the test image (Fig. 2), 2D forward then reverse BinDCTs were run on the XC6264 designs to assess pixel errors. The static BinDCT-C1 had a RMSE of 0.0738, the static BinDCT-C9 an RMSE of 0.0439 and the dynamic BinDCT only an RMSE of 0.0027. Therefore the dynamic BinDCT was more accurate than the individual static BinDCTs tried for the test image.

At the beginning of this research, the XC6200 FPGA family were the only commercially available dynamic RTR FPGAs. Limitations within the XC6200 FPGA architecture restricted BinDCT transform implementations and RTR performance. Comparison to cutting edge FPGA and processor technologies, the operating properties of this operation appear inefficient. However, this image processing application has practically demonstrated how RTR hardware can be used to increase both the compression ratios and operand throughput. Merged with the loss-less compression properties of the BinDCT configurations, dynamic BinDCT implementation provides a basis for enhancing speed-dependent low-power consumption compression applications.

Conclusions: The implementation of dynamic coprocessor hardware has demonstrated how RTR implementations can improve the compression ratio, accuracy and operand throughput of a BinDCT application. Through RTR of two BinDCT modes (BinDCT-C1 and BinDCT-C9), image data DCT coding gain has increased by 5%, and operand throughput can be increased by over 200%. With improved dynamic semiconductor technologies, reconfiguration times will decrease and all nine BinDCT configurations could be used, allowing even more dramatic results.

© IEE 2002 28 May 2002
Electronics Letters Online No: 20020711
DOI: 10.1049/el.20020711

C.W. Murphy and D.M. Harvey (Coherent Electro Optics Research Group, School of Engineering, Liverpool John Moores University, Byrom Street, Liverpool, L3 3AF, United Kingdom)

References
1 'XC6200 FPGA family data sheet', April 1997, (Xilinx, Version 1.10)

Compact all-fibre on-line power monitor via core-to-cladding mode coupling

Qun Li, C.-H. Lin, A.A. Au and H.P. Lee

An on-line all-fibre power monitor is demonstrated in which light from the core mode is first coupled to the cladding mode using an acousto-optic tunable filter, and then coupled to an InGaAs pin detector bonded to the fibre. Detection efficiency for different cladding modes and fibre cladding diameters are presented.

Introduction: Loss filters such as long-period fibre gratings (LPGs) [1], blazed fibre Bragg gratings (FBGs) [2], and acousto-optic