Time-to-Digital Converter with Direct Successive Charge Redistribution

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Abstract- In the paper, the enhanced version of time-to-digital converter with self-timed successive charge redistribution is presented. In the proposed solution, time-to-charge mapping realized by constant rate charge accumulation is run concurrently to the charge redistribution in the binary-weighted capacitor array. By introducing concurrent charge accumulation and redistribution, the conversion is characterized by reduced conversion time and conversion time jitter, reduction of die area of the chip, and of the number of state transitions per a single conversion cycle.

I. Introduction

The continued down scaling of CMOS technology forces decreasing the supply voltage of integrated circuits and systems. For example, in the nanoscale technologies with the feature size lower than 100 nm, the maximum operating voltage is close to 1V. In the context of analog-to-digital converters with quantization of signal amplitude, the technology scaling decreases conversion accuracy due to a reduction of a quantization step size (LSB) [1]. In the high resolution ultra-low voltage ADCs, the quantization step size approaches noise level. Therefore, encoding signal values in time as an alternative approach to conventional encoding signals in the amplitude domain has become a technique of increasing importance in modern electronic instrumentation and signal processing [2],[12].

In particular, time encoding is used in a new class of ADCs called asynchronous analog-to-digital converters (A-ADCs) developed in the last decade [3]-[5]. In A-ADCs, an asynchronous mapping of analog signal value into the time domain replaces a conventional sampling. This process might be considered as analog-to-quasi-digital conversion (AQDC) because as known the time parameters combine analog and digital signal properties [6]. The examples of the AQDCs are the level-crossing sampler [3],[4], or the time-encoding machines (TEMs) [2],[12]. On the other hand, an example of the TEM attractive for analog-to-digital conversion is the asynchronous Sigma-Delta modulator [5],[7]. The level-crossing sampler belongs to the class of instantaneous converters, and the TEMs are mean value converters. In the second step of asynchronous analog-to-digital conversion, the time parameters in a form of the asynchronous sequence of time intervals are discretized in the time-to-digital converter (TDC) according to the resolution of a reference clock [3],[5],[8].

Due to recent progress of theory, the methods and algorithms for loss-free recovery of bandlimited signals encoded in the time domain using the time-encoding machines have been developed [2],[7].

Since time encoding is essentially an asynchronous process, the clock is no longer needed to trigger sampling operations. However, the reference clock has been still used for quantizing time intervals that encode signal values in the time domain.

In [9], we have proposed a new method for time quantization that enables eliminating the clock even from the time quantization block and developing fully clockless ADCs. In our approach to time-to-digital conversion, the discretized time interval is first translated to the corresponding charge packet, and next processed in the charge domain by self-timed successive charge redistribution in the binary-scaled capacitor array [9]. The concept of the time-to-digital conversion based on successive redistribution consists in applying the well-known binary search principle to the conversion in the time domain. A significant issue is that the time-to-digital conversion with successive charge redistribution differs from the known technique of charge redistribution used in classical digital-to-analog converters with the binary-weighted capacitors because the charge transfer process is self-timed in the former whereas it is clock-driven in the latter.

The motivation to use the time-based binary search scheme is a desire of reducing the number of state transitions in the circuit in order to reduce the power consumption. In the n-bit TDCs with a high frequency reference clock,
the relationship between the number of bits of resolution and the number of clock cycles needed per a single conversion is exponential and equal to 2^n [3],[5],[8]. In the time-based energy-efficient ADC presented in [10], the exponential relationship of state transitions has been substituted by a linear relationship, and the number of required transitions is 5n. In the charge-redistribution-based TDC introduced in the [9], a number of transitions per a single conversion is (n+2) only.

Moreover, the Successive Charge Redistribution Time-to-Digital Converter (SCR-TDC) architecture proposed in [9] is extremely simple and self-timed. The n-bit SCR-ADC is built of the binary-weighted capacitor array with (n+1) capacitors, two asynchronous comparators, one or two current sources, the asynchronous state machine, and a group of controlled switches. Compared to the conventional successive-approximation ADCs, the SCR-TDC does not contain a digital-to-analog converter and does not need an external clock. Furthermore, the SCR-TDC does not use any time base and any reference voltage. The only reference used is the sum and the ratio of capacitances of the capacitors. The implementation of the SCR-TDC scales well with CMOS technology.

In the present paper, the enhanced version of the SCR-TDC called Direct Successive Charge Redistribution Time-to-Digital Converter (DSCR-TDC) is presented. A principal difference introduced in the DSCR-TDC compared to the SCR-TDC is that the charge accumulation and redistribution are run in the former concurrently instead of sequentially as applied in the latter. Several benefits are obtained due to this enhancement.

First of all, the DSCR-TDC is characterized by significantly reduced conversion time. More specifically, the conversion time is shorter in the DSCR-TDC by the charge accumulation time which is equal to the quantized time interval length T_{in}. In particular, the conversion time is reduced at least twice for short time intervals, and at least four times for long time intervals. Moreover, the conversion time jitter (i.e., the difference between the maximum and minimum conversion time) is reduced twice in the DSCR-TDC in relation to the SCR-TDC. The advanced analysis and comparison of the conversion time between the SCR-TDC and DSCR-TDC is presented in [11].

Second, in the DSCR-TDC, the capacitor array contains only a number of n sections, instead of (n+1) as is in the SCR-TDC, because the section containing the capacitor C_0 of the largest capacitance is removed. The die area is thus reduced twice since the input capacitor C_0 equals approximately the sum of the other capacitances C_{n,1},...C_{0} in the SCR-TDC capacitor array. The latter benefit is of significant importance since the die area required to implement the capacitor array occupies usually a large majority of the die area of the whole converter architecture.

Finally, the number of state transitions per a single conversion in the DSCR-TDC equals (n+1) instead of (n+2) in the SCR-TDC, which gives promise of decreasing power consumption.

II. DSCR-TDC Architecture and Operation

The DSCR-TDC operation cycle consists of two phases. In the first phase, the discretized time interval T_{in} is translated to the corresponding charge packet and simultaneously processed in the charge domain by self-timed successive charge redistribution in the binary-scaled capacitor array. The duration of time-to-charge mapping, realized by charge accumulation at constant rate, equals the width of the time interval T_{in}. If the T_{in} is shorter than duration of charge redistribution process, then, after termination of the discretized time interval T_{in}, the next conversion phase consists in redistributing the residual charge according to the same algorithm as used previously.

A. Converter Architecture

The block diagram of the Direct Successive Charge Redistribution Time-to-Digital Converter (DSCR-TDC) is presented in Fig. 1. The architecture of the DSCR-TDC is in general the same as the architecture of the classical Successive Charge Redistribution Time-to-Digital Converter (SCR-TDC) reported in [9]. The only difference concerns the number of the capacitors in the binary-weighted capacitor array and the algorithm of operation of the asynchronous state machine that implements the binary search scheme. More specifically, instead of n+1 capacitors used in the SCR-TDC, the binary-weighted capacitor array in the DSCR-TDC contains a number of n capacitors since the sampling capacitor is absent.

The DSCR-TDC circuit diagram is shown in Fig. 2. Each cell in the capacitor array contains a capacitor C_i and three controlled switches: S_{Hi}, S_{Lo}, S_{Hi} i=0,1,...,n-1. These switches are controlled by the signals D_{n,1},...,D_{0} and I_{0,1},...,I_{0} produced by the asynchronous state machine. The switch S_{Hi} is controlled by the signal D_{Hi}. The cells differ from each other only by a value of the capacitance of C_i. In the i-th cell, the capacitance C_i equals 2^{i}C_{in}, where C_{in} is a unit capacitance located in the cell corresponding to the LSB. Each capacitor C_i corresponds to the appropriate bit b_i in the output digital word.
B. Concurrent charge accumulation and redistribution

The DCSR-TDC operates as follows. Assume the time interval, whose duration $T_{ih}$ is converted to a digital number, is provided in a form of a pulse signal to the DCSR-TDC input. Detecting a leading edge of the pulse by the asynchronous state machine causes the capacitor $C_{n,1}$ corresponding to the most significant bit (MSB) to be charged by the current source of constant intensity $I_{h}$ (Fig. 2).

If a voltage on the capacitor $C_{n,1}$ reaches the prespecified threshold $V_L$ before the trailing edge of the pulse $T_{ih}$ is detected by the asynchronous state machine, the most significant bit $b_{n-1}$ is set to ‘one’. Then, the consecutive capacitors $C_{n,2}, C_{n,3}, \ldots$ are charged sequentially in order to decreasing capacitances by the current source $I_{h}$. Assume that the discretized time interval $T_{ih}$ ends in the $k$th step of charge accumulation where $k \in \{1, \ldots, n\}$, i.e., during the time when the capacitor $C_{n,k}$ is charged. The trailing edge of the pulse $T_{ih}$ stops to provide charge from the current source $I_{h}$, and starts to redistribute in the subsequent steps the residual charge stored in the latterly charged capacitor $C_{n,k}$ into the set of binary-weighted capacitors $C_{n,k+1}, \ldots, C_0$ (Fig. 3). The residual charge redistribution is carried out by the current source $I_{h}$ (in the version of DCSR-TDC with a single current source) or by an extra current source $I_{h}$ (in the version of DCSR-TDC with two current sources). The effectiveness of the current source $I_{h}$ should be higher than of the current source $I_{h}$ in order to accelerate the residual charge transfer process. In the configuration with two current sources, the conversion time of the DCSR-TDC is independent of the duration of discretized time interval $T_{ih}$. In the possible configuration with a single current source used both during the charge accumulation and the redistribution, the DCSR-TDC conversion time depends on the $T_{ih}$. Both current sources are activated respectively by the control signals $C_{S1}$ and $C_{S2}$ produced by the asynchronous state machine. The index value $(n-k)$ of the capacitor $C_{n,k}$ depends on the width of the converted time interval $T_{ih}$. The number $k$ is equal to one for very short time intervals, and respectively equals $n$ for the time intervals $T_{ih}$ whose width is close to the converter range.

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Conversion step number: 1 2 \ldots k-1 k k+1 k+2 \ldots n
Bit index: b_{n-1} b_{n-2} \ldots b_{n+k-1} b_{n+k} b_{n+k+1} \ldots b_0
Bit state: 1 1 \ldots 1 0 x x \ldots x
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$x = \{0, 1\}$

Figure 3. Sequence of conversion phases in the DCSR-TDC
C. Residual charge redistribution

In the first step of residual charge successive redistribution, which is at the same time the \((k+1)\)th conversion step, the capacitor \(C_{i,k}\) starts to operate as the first source capacitor whereas the role of the destination capacitor plays the capacitor \(C_{n,k+1}\). Further conversion proceeds in the same way as in the SCR-TDC as follows.

If a voltage on the capacitor \(C_{n,k+1}\) reaches the prespecified threshold \(V_t\), then the bit \(b_{n,k+1}\) is set to ‘one’. Next, the remaining charge stored in the input capacitor \(C_{n,k}\) is transferred in the second step of residual charge redistribution to the capacitor \(C_{n,k+2}\) that takes over the role of the next destination capacitor.

However, if the capacitor \(C_{n,k}\) is discharged before the voltage on the capacitor \(C_{n,k+1}\) reaches the threshold \(V_t\) during the first conversion step, then the bit \(b_{n,k+1}\) is set to ‘zero’. Furthermore, in the second step of residual charge redistribution, the capacitor \(C_{n,k+2}\) plays the role of the next source capacitor and the charge is then transferred from the \(C_{n,k+1}\) to the \(C_{n,k+2}\). The cycle is repeated for the subsequent steps. Each conversion step produces one bit more precise discrete estimate of the input time interval.

Each conversion cycle is followed by the relaxation phase when the asynchronous state machine reconfigures the switch positions in order to discharge all the capacitors.

D. Selection of Current Source and Current Destination Capacitors

In the \(i\)th conversion step, the charge is transferred from the particular capacitor that operates currently as a source capacitor \(Source\_C(i)\) to a current destination capacitor \(Dest\_C(i)\). In fact, during the concurrent charge accumulation and redistribution, the capacitors \(C_{n,1}, C_{n,2}, \ldots, C_{n,k}\) act as the destination capacitors. Then, the source of charge collected in the destination capacitors is the current source \(I_c\). All the bits \(b_{n,1}, b_{n,2}, \ldots, b_{n,k+1}\) corresponding to the capacitors \(C_{n,1}, C_{n,2}, \ldots, C_{n,k+1}\) are evaluated to ‘one’ since all these capacitors have been charged to the desired voltage \(V_t\) before the trailing edge of the pulse \(T_{bh}\) is detected. In general, the bit \(b_{n,k}\) corresponding to the capacitor \(C_{n,k}\) charged when the converted time interval \(T_{bh}\) ends, is the most significant bit whose state is set to ‘zero’ (Fig. 3). Theoretically, the bit \(b_{n,k}\) can be set to one in the ideal situation if the process of charging the capacitor \(C_{n,k}\) is stopped exactly when the trailing edge of the time interval \(T_{bh}\) is detected by the asynchronous state machine. In such situation, the conversion phase is completed exactly after termination of the charge accumulation phase, and time-to-digital conversion is characterized by a non-redundant conversion time.

However, in further discussion, we assume a real scenario when the charge accumulation phase stops when the voltage on the currently charged capacitor is not equal to the desired level \(V_t\), thus the bit \(b_{n,k}\) is set to ‘zero’.

As stated, during the first step of the residual charge redistribution, which is on the other hand the \((k+1)\)th conversion step, the status of the first source capacitor is assigned to the \(C_{n,k}(Source\_C(k+1)=C_{n,k})\) that acted as the last destination capacitor in the charge accumulation phase in the \(k\)th conversion step. The subsequent conversion steps go ahead according to the same algorithm as in the classical Successive Charge Redistribution Time-to-Digital Converter (SCR-TDC) reported in [9].

The destination capacitors in subsequent steps are chosen successively according to the order of decreasing capacitances both during charge accumulation and redistribution:

\[
Dest\_C(i+1) = Dest\_C(i) - 1; i = 1, \ldots, n - 1
\]

The role of source capacitor is handed over in the conversion step \((i+1)\) to the capacitor \(C_{n,i}\) if the state of the bit \(b_{n,i}\) has been fixed and set to ‘zero’ in the previous conversion step. Otherwise, the index of the source capacitor is not changed in the \((i+1)\)th step:

\[
Source\_C(i+1) = \begin{cases} 
Source\_C(i); & \text{if } b_{i} = 1 \\
Dest\_C(i); & \text{if } b_{i} = 0
\end{cases} i = 1, 2, \ldots, n
\]

In Table 1, the course of 6 initial steps of \(n\)-bit DSCR-TDC conversion cycle is specified based on the exemplified states of output bits. Note that \(Source\_C(6)=Dest\_C(5)=C_{n,5}\) during step 6 since \(b_{n,5}=0\). Furthermore, \(Source\_C(5)=Source\_C(4)=C_{n,3}\) during the step 5 since \(b_{n,3}=1\). Note also that \(n-3\) is the index of \(Source\_C(5)\) and \(Source\_C(4)\), and on the other hand is also the least significant bit among the bits \(b_{n,4}, b_{n,3}\) whose states have been already known in step 5 and evaluated to ‘zero’. The conversion is completed after the \(n\)th step when the role of a destination capacitor plays the capacitor \(C_{n}\).

Generalizing, during the \(i\)th step of charge redistribution when the states of the number of \((i-1)\) most significant bits \(b_{n,i-1}, b_{n,i-2}\) are already fixed, the capacitor \(C_{n,i}\) operates as the destination capacitor \(Dest\_C(i)\):

\[
Dest\_C(i) = C_{n-i}
\]

where \(i = 1, \ldots, n\).
The status of the source capacitor Source_C(i) in the step \(i, i \geq 2\) is assigned to the capacitor \(C_j, j \leq n-i\) such that:

\[
\text{Source}_-\text{C}(i) = C_j;
\]

where

\[
j = \min(k; k = n - i + 1, \ldots, n - 1: b_k = 0), \text{ for } i \geq 2
\]

As follows from the formulae (4)-(5), the capacitor \(C_j\) acts as the source capacitor Source_C(i) in \(i\)th conversion step where \(i \geq 2\) provided that the bit \(b_j\) is the least significant bit among the bits \(b_{n+1}, b_{n+2}, \ldots, b_{n-i}\) whose state has been evaluated to ‘zero’.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Conversion step index (i)</th>
<th>Source_C(i)</th>
<th>Dest_C(i)</th>
<th>Index of bit evaluated</th>
<th>Example of evaluated bit states</th>
<th>Active control signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relaxation</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>D_{n,1}, D_{n,2}, I_{n,1}</td>
</tr>
<tr>
<td>Charge Accumulation/Redistribution</td>
<td>1</td>
<td>C_{n,1}</td>
<td>n-1</td>
<td>1</td>
<td>C_{n,1}, D_{n,1}, I_{n,1}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>C_{n,2}</td>
<td>n-2</td>
<td>1</td>
<td>C_{n,2}, D_{n,2}, I_{n,2}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>C_{n,3}</td>
<td>n-3</td>
<td>0</td>
<td>C_{n,3}, D_{n,3}, I_{n,3}</td>
<td></td>
</tr>
<tr>
<td>Residual Charge</td>
<td>4</td>
<td>C_{n,4}</td>
<td>n-4</td>
<td>1</td>
<td>C_{n,4}, D_{n,4}, I_{n,4}</td>
<td></td>
</tr>
<tr>
<td>Redistribution</td>
<td>5</td>
<td>C_{n,5}</td>
<td>n-5</td>
<td>0</td>
<td>C_{n,5}, D_{n,5}, I_{n,5}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>C_{n,6}</td>
<td>n-6</td>
<td>...</td>
<td>C_{n,6}, D_{n,6}, I_{n,6}</td>
<td></td>
</tr>
</tbody>
</table>

### E. Event-driven conversion control

In the circuit diagram shown in Fig. 2, the DSCR-TDC conversion is managed by the asynchronous state machine (ASM), and consists in controlling charge accumulation at first, and next in residual charge redistribution through a dynamic reconfiguration of states of controlled switches. The switches are reconfigured as a response to internal events occurring in the conversion process and reported by both comparators. These events are:

- detection of leading edge of the converted time interval of \(T_{in}\) duration,
- detection that the voltages on the capacitors \(C_{n,1}, C_{n,2}, \ldots, C_{n,k}, \ldots\) reach the value \(V_L\),
- detection that trailing edge of the converted time interval,
- detection that the voltages on the capacitors \(C_{n,1}, C_{n,2}, \ldots, C_{n,k}, \ldots, C_0\) reach the value \(V_L\), and/or that the capacitors \(C_{n,k}, C_{n,k+1}, \ldots, C_0\) are completely discharged.

The aim of switch reconfiguration in each step is:

- establishing the path between the current source \(I_k\) and the capacitors \(C_{n,1}, C_{n,2}, \ldots, C_{n,k}\) operating as the destination capacitors during charge accumulation,
- selection of the source \(\text{Source}_-\text{C}(i)\) and destination Dest_C(i) capacitors for \(i = k+1, \ldots, n\), and establishing the path between both capacitors to redistribute the residual charge by the use of the current source \(I_k\) (in the version with two current sources, Fig. 2) or \(I_h\) (in the version with a single current source).

Transfer of residual charge results in growing the voltage on the destination capacitor Dest_C(i), and falling the voltage on the source capacitor Source_C(i). If the former voltage reaches \(V_L\) before the latter falls to ‘zero’, the comparator \(K2\) signals to the ASM that the Dest_C(i) is charged to a desired voltage \(V_L\). Then the ASM sets the bit \(b_{n-i}\) in the output digital codeword corresponding to the Dest_C(i) to ‘one’, and changes the destination capacitor according to the condition (1) by appropriate switch reconfiguration.

If the voltage on the source capacitor Source_C(i) falls to ‘zero’ before the voltage on the destination capacitor Dest_C(i) reaches a desired level \(V_L\), the comparator \(K1\) reports to the ASM that the Source_C(i) is discharged. Then, the ASM sets the output bit \(b_{n-i}\) to ‘zero’, and reconfigures the states of switches to change both the source and the destination capacitors according to the conditions (1) and (2), respectively.

The other tasks managed by the ASM is to discharge all the capacitors during relaxation phase before a new conversion cycle.

### F. Switch Control

In Table I, the control signals produced by the ASM that are active in the relaxation, concurrent charge accumulation/conversion and during residual charge successive redistribution are listed. These signals are referred to the converter architecture presented in Fig. 2.
As seen in Fig. 2, apart from three controlled switches $S_{th}$, $S_{le}$, $S_{gi}$ assigned to the $i$th cell in the capacitor array, there is also an extra switch $S_{out}$ that is closed only during the relaxation phase. The switches are controlled by the signals $I_i$ and $D_i$ produced by the asynchronous state machine. A pair of switches $S_{gi}$, $S_{le}$, assigned to a given capacitor $C_i$, is controlled by the same signal $I_i$, $i = 0, 1, \ldots, n$. Therefore, if a bottom plate of the capacitor $C_i$ is grounded, its top plate is at the same time coupled to the rail $L$. The switch $S_{th}$ is controlled by the signal $D_i$. The active state of the control signal $I_{0i}$ selects respectively the current destination capacitor $Dest\_C(i)$ (Table I). During the residual charge redistribution, the active state of $D_i$ indicates the current source capacitor $Source\_C(i)$. On the other hand, during the charge accumulation, the signal $D_{n+1}$ is activated (Table I). The cells that are not currently involved in the charge redistribution are driven with inactive states of both control signals $I_i$ and $D_i$ (see Table I).

### III. Conclusions

The paper deals with developing self-timed ultra low power and low voltage time-to-digital converter designed in general for asynchronous analog-to-digital conversion. The proposed method successfully addresses multiple design criteria such that minimizing the conversion time and its jitter, reducing die are of the chip and power consumption which is mainly represented by a number of the state transitions in the circuit.

### References


