Low-voltage digitally controlled current differencing buffered amplifier and its application

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Abstract

In this paper, a design of a low-voltage digitally controlled current differencing buffered amplifier (DC-CDBA) is introduced. The realization scheme is through the cascade connection of a current differencing circuit, a current division network (CDN) and a buffered voltage amplifier. To achieve the digital control of the current gain of the circuit, a novel CDN is also proposed. The proposed DC-CDBA can operate with the low supply voltage of ±1.25 V. PSPICE simulations using standard 0.5-µm CMOS process parameters are in agreement with the theory. An application example using the proposed DC-CDBAs as active elements in the realization of the digitally tuned current-mode universal filter is also included. © 2008 Elsevier GmbH. All rights reserved.

Keywords: Current differencing buffered amplifier (CDBA); Current division network (CDN); MOS transistor; Current-mode circuit

1. Introduction

Programmable tuning characteristic of an analog circuit is an attractive feature that is widely used in several useful applications. In analog signal processing area, there are many engineering applications which require programmable characteristics such as, adaptive filters, music synthesizers, formant speech synthesizers and tracking filters [1–4]. Generally, analog or digital tuning can be employed to control the circuit parameters. However, in low-voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, the digital control is more attractive [5]. Another example utilizing digital control is the interface with the digital signal processing (DSP) unit in the modern digital system. For example, in modern wireless systems, all of the baseband signal processing are implemented digitally by DSP unit. There are baseband analog blocks required in the integrated wireless receiver such as highly linear filter section for out-of-band blockers attenuation, tunable filter section for channel selection, and variable gain amplifier for providing programmable gain setting and a primary requirement of those baseband analog blocks are to be digitally controlled [5]. Therefore, digitally programmable tuning characteristics have been an ongoing research topic for a number of years.

In 1999, a new active building block circuit, namely current differencing buffered amplifier (CDBA), was first introduced to provide new possibilities in the circuit synthesis and to simplify the circuit implementation [6,7]. The CDBA is suitable for integrated circuit (IC) implementation in both bipolar and CMOS technologies [7–12]. Moreover, since the CDBA can be considered as a collection of current- and voltage-mode unity gain cells, it has large dynamic range and quite wide bandwidth similar to its current-mode counterparts such as, current feedback operational amplifiers (CFAs) and second generation current conveyors (CCIIs). Owing to these advantages of the CDBA, in this paper we present...
a digitally controlled CDBA (DC-CDBA) with low supply voltage operation. The proposed DC-CDBA is realized by interconnecting a current differencing circuit, a current division network (CDN), and a unity-gain voltage amplifier. The novel CDN circuit is also proposed in order to provide the digital control of the current gain of the DC-CDBA. An application of the proposed DC-CDBA in realizing digitally programmable current-mode universal filter with the advantage of linearly tuned frequency to the digitally controlled parameter has also been discussed. PSPICE simulation results of the proposed low-voltage DC-CDBA and its application are included.

2. Circuit configurations

2.1. Basic concept

The proposed DC-CDBA is a versatile analog building block, described symbolically as shown in Fig. 1(a) and mathematically by the following matrix equation:

\[
\begin{bmatrix}
    i_z \\
    v_w \\
    v_p \\
    v_n
\end{bmatrix}
= \begin{bmatrix}
    0 & 0 & 0 & -z \\
    1 & 0 & 0 & 0 \\
    0 & 0 & 0 & 0 \\
    0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
    v_z \\
    i_w \\
    i_p \\
    i_n
\end{bmatrix},
\]

where \( z \) is the current gain that is controlled digitally. According to the above matrix equation, this device consists of three stages as shown in Fig. 1(b). The input stage is a current differencing circuit to provide the difference of the input currents (\( i_p \) and \( i_n \)) through the terminals \( p \) and \( n \) into the \( x \)-terminal current \( i_x \). The second stage is a CDN, which is based on the linear current division principle. At this stage, the current \( i_x \) is copied to the \( z \)-terminal and is digitally controlled by the current gain parameter \( z \). The last stage is simply a voltage buffer, since the voltage at the \( w \)-terminal follows the voltage of the \( z \)-terminal. Therefore, the operation of each stage will be described in the following section.

2.2. Current differencing circuit

Fig. 2 shows an NMOS-based circuit with a low-input resistance terminal [13]. From the elementary small-signal circuit analysis, the input resistance of this configuration can be calculated as

\[
r_{in} = \frac{1}{g_{m1}} \left( \frac{1}{1 + F} \right),
\]

where \( F = ((g_{m2}g_{m4}r_{OB})/(g_{m2} + g_{m3})) \) and \( g_{mi} \) represents the transconductance of the transistors \( M_i \) \( (i = 1, 2, 3, 4) \) and \( r_{OB} \) denotes the output resistance of the current source \( I_B \). Usually \( r_{OB} \approx 1/g_{mi} \), then \( F \gtrsim 1 \). Therefore, the input resistance of this circuit is very low.

Based on the use of the low-input resistance input stage of Fig. 2, the unity gain current amplifier can be realized as shown in Fig. 3. The biasing circuit comprising the transistor \( M_6 \) and the current source \( I_B \) is used to bias the input terminal at ground potential. By direct analysis, the output
current $i_{\text{out}}$ of this circuit can be expressed as

$$i_{\text{out}} = - \left( \frac{F}{1+F} \right) i_{\text{in}}. \quad (3)$$

Usually $F \gg 1$, the output current $i_{\text{out}}$ can be approximated to

$$i_{\text{out}} \approx - i_{\text{in}}. \quad (4)$$

Fig. 4 shows the proposed CMOS current differencing circuit, which is composed of two unity-gain current amplifiers ($M_{1A}-M_{5A}$) and ($M_{1B}-M_{3B}$). Due to the current mirror $M_{7}-M_{8}$, the signal current flowing out of the terminal $x$ ($i_{x}$) can be expressed as

$$i_{x} = i_{p} - i_{n}. \quad (5)$$

In this case, the input resistances of the terminals $p$ and $n$ can also be written as

$$r_{p} = \left( \frac{1}{g_{m1A}} \right) \left( \frac{1}{1+F_{p}} \right), \quad (6)$$

and

$$r_{n} = \left( \frac{1}{g_{m1B}} \right) \left( \frac{1}{1+F_{n}} \right), \quad (7)$$

where $g_{m1A}$ and $g_{m1B}$ represent respectively the transconductance of the transistors $M_{1A}$ and $M_{1B}$ ($i=1, 2, 3, 4, 5$), $F_{p} = ((g_{m2A}g_{m4A}r_{0B})/(g_{m2A}+g_{m3A}))$ and $F_{n} = ((g_{m2B}g_{m4B}r_{0B})/(g_{m2B}+g_{m3B}))$. Therefore, the input resistances $r_{p}$ and $r_{n}$ are very low due to the factors from the feedback $(1+F_{p})$ and $(1+F_{n})$, respectively.

2.3. Current division network (CDN)

Fig. 5(a) shows the proposed current division cell (CDC). It should be noted that this cell is mainly composed of the unity-gain current amplifier ($M_{1C}-M_{5C}$) of Fig. 3 and a current divider ($M_{7}-M_{8}$). According to the current division principle, the output currents ($i_{i}, i_{o}$, and $i_{o}$) of the proposed CDC related to the input current ($i_{i+1}$) are respectively obtained as follows:

$$i_{i} = i_{i} + \frac{1}{2}, \quad (8)$$

$$i_{o} = a_{i} \left( \frac{i_{i} + 1}{2} \right), \quad (9)$$

and

$$i_{o} = a_{i} \left( \frac{i_{i} + 1}{2} \right), \quad (10)$$

where $a_{i}$ is the digital control bit of this cell. The circuit symbol of the proposed CDC is depicted in Fig. 5(b).

The proposed CDN, consisting of $n$ CDCs, is shown in Fig. 6(a). As can be seen from Fig. 6(a), the output current $i_{i}$ of the CDC ($i=0, 1, 2, \ldots, n$) is used as an input current of the next stage and the current $i_{0}$ is added to $i_{o}$. Therefore, the output current ($i_{\text{out}}$) of the proposed CDN can be described by

$$i_{\text{out}} = \left( \frac{1}{2^{n+1}} \right) \left[ 1 + \sum_{i=0}^{n} a_{i}2^{i} \right] i_{x} \quad (11)$$

or

$$\alpha = \frac{i_{x}}{i_{p} - i_{n}} = \frac{i_{\text{out}}}{i_{x}} = \left( \frac{1}{2^{n+1}} \right) \left[ 1 + \sum_{i=0}^{n} a_{i}2^{i} \right]. \quad (12)$$

From Eq. (12), the current gain ($\alpha$) of the proposed CDN can be controlled digitally, where $\alpha$ is less than, or equal to, unity. An electrical circuit symbol of the proposed CDN is also shown in Fig. 6(b).

2.4. Buffered voltage amplifier

The circuit of Fig. 7 is a unity-gain voltage amplifier, which is based on the use of the low-input resistance input stage ($M_{1D}-M_{4D}$) from Fig. 2. From the configuration, the transistor $M_{11}$ and two bias current sources $I_{B}$ are connected
as voltage level shift. Therefore, the relationship of the voltages at the terminals \( w \) and \( z \) (or \( v_w \) and \( v_z \)) can be given by

\[
v_w = \beta_w v_z
\]

and

\[
\beta_w = \left( \frac{g_{m11} r_{oB}}{1 + g_{m11} r_{oB}} \right) \left[ \frac{g_{m1D} \left( 1 + \frac{g_{m4D} r_{oB}}{2} \right)}{g_w + g_{m1D} \left( 1 + \frac{g_{m4D} r_{oB}}{2} \right)} \right],
\]

where \( g_w = 1/R_w \) and \( R_w \) is the resistor connected at the terminal \( w \). If \( g_{m11} r_{oB} \gg 1 \) and \( g_{m1D} \left( 1 + \left( g_{m4D} r_{oB} / 2 \right) \right) \gg g_w \), then \( v_w \approx v_z \). Since transistors \( M_{1D} - M_{4D} \) performs a
low-input resistance stage, the resistance of the terminal \( w \) \((r_w)\) becomes quite low and is equal to

\[
r_w = \left( \frac{1}{g_{m1D}} \right) \left( \frac{1}{1 + F_w} \right), \tag{15}
\]

where

\[
F_w = \left( \frac{g_{m2D}S_m4DR_{oB}}{g_{m2D} + g_{m3D}} \right). \tag{16}
\]

If \( r_{oB} \gg 1/g_{m11} \), the input resistance looking into the terminal \( z \) \((r_z)\) becomes a high value and is approximated to

\[
r_z = \frac{r_{oB}}{2}. \tag{17}
\]

### 2.5. Proposed low-voltage DC-CDBA

Fig. 8 shows the proposed low-voltage DC-CDBA, which is constructed by the cascaded connection of the current differencing circuit in Fig. 4, the CDN in Fig. 6 and the buffered voltage amplifier in Fig. 7. From the circuit diagram, it can be considered from the positive to the negative supply voltages that the proposed circuit uses only two MOS transistors and one bias current source. Therefore, the circuit can operate at a low power supply voltage of \( V_{DD} \) and \( V_{FB} \), where \( V_{DS} \) and \( V_{FB} \) are the drain-to-source voltage of the MOS transistor and the voltage drop at the bias current source \( I_B \), respectively. As an example, for the standard 0.5-\( \mu \)m CMOS process parameters, the threshold voltages \( V_{TN} \) and \( V_{TP} \) of the NMOS and PMOS transistors are about 0.64 and 0.91 V, respectively. If the bias current sources \( I_B \) are realized by the basic current mirrors, as a result, the minimum supply voltage is about \( [2(0.64 \text{ V}) + (0.91 \text{ V})] = 2.19 \text{ V} \) or \( \pm 1.095 \text{ V} \).

**Table 1.** The model parameters set of 0.5-\( \mu \)m CMOS SCN05H technology

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### 3. Simulation results

The performance of the proposed DC-CDBA of Fig. 8 has been simulated using PSPICE program with 0.5-\( \mu \)m CMOS SCN05H technology provided by MOSIS. The model parameters of 0.5-\( \mu \)m CMOS process are given in Table 1, and the aspect ratios of the transistors used are \( W/L = 20 \mu m/1 \mu m \) for the NMOS devices and \( W/L = 40 \mu m/1 \mu m \) for the PMOS devices, respectively. The supply voltages used are taken as: \( +V_{DD} = -V_{SS} = 1.25 \text{ V} \), and \( n = 3 \) (4 bits). All the biasing currents are set to \( I_B = 100 \mu A \). Grounded resistors \( R_z = 1 \text{ k}\Omega \) and \( R_w = 10 \text{ k}\Omega \) are connected at the terminals \( z \) and \( w \), respectively.

Fig. 9 shows the DC current characteristics of the terminal \( z \) versus \( i_p \) and \( i_z \) when the digitally controlled word parameter \( z \) is scanned from 0.125 to 1.000 in steps of 0.125.
Fig. 9. DC current transfer characteristics of the proposed DC-CDBA for different values of $\alpha$.

Fig. 10. AC current transfer characteristics of the proposed DC-CDBA for different values of $\alpha$. 
In Fig. 10, the AC current responses of the terminal \( z \) for the same \( \alpha \) setting are shown, which can be seen that the bandwidth is approximately equal to 100 MHz.

Fig. 11 shows the \( u \)-terminal voltage (\( v_u \)) when the \( z \)-terminal voltage (\( v_z \)) is swept from \(-1 \) to \(1 \) V for different values of \( \alpha \) ranging from \(0.125 \) to \(1.000 \) with \(0.125 \) step. It can be seen from the figure that the inclination of the voltage transfer error starts to increase when \( v_z \) greater than \(+0.8 \) V. This effect is mainly caused by the limitation of the operating range at the terminal \( w \). It is noted that, in the configuration of Fig. 8, the maximum value of \( v_w \) is restricted to be less than \([V_{DD} - V_{TP} - V_{DS,\text{sat}(M1D)}]\). The \( u \)-terminal AC voltage response is shown in Fig. 12 from which it can be found that the bandwidth is approximately located at 500 MHz. Therefore, the high-frequency limitation of the proposed DC-CDBA is located at about 100 MHz.

### 4. Application example

As an application example for the proposed device, the digitally tuned current-mode universal filter with three inputs and one output shown in Fig. 13 is realized. The configuration consists of only three DC-CDBAs, two resistors and two grounded capacitors. Routine circuit analysis using Eq. (1) yields the following current transfer function:

\[
I_{\text{out}} = \alpha_3 \left[ \frac{D(s)I_1 - (sR_1C_1\alpha_2)I_2 - (\alpha_1\alpha_2)I_3}{D(s)} \right],
\]

where \( D(s) = (s^23R_1R_2C_1C_2 + sR_1C_1\alpha_2 + \alpha_1\alpha_2) \) and \( \alpha_3 \) denotes the parameter \( \alpha \) of the \( i \)th DC-CDBA \((i = 1, 2, 3)\). From Eq. (18), it can be summarized that:

1. if \( I_1 = I_2 = 0 \), and \( I_3 = I_{\text{in}} \) (an input current), the lowpass (LP) response can be realized;
2. if \( I_1 = I_3 = 0 \) and \( I_2 = I_{\text{in}} \), the bandpass (BP) response can be realized;
3. if \( I_1 = I_2 = I_3 = I_{\text{in}} \), the highpass (HP) response can be realized;
4. if \( I_3 = 0 \) and \( I_1 = I_2 = I_{\text{in}} \), the bandstop (BS) response can be realized;
5. if \( I_3 = 0 \) and \( I_1 = I_2/2 = I_{\text{in}} \), the allpass (AP) response can be realized.

Therefore, the filter can realize five standard types of the biquadratic filtering functions without any component matching condition requirements. The DC gain (\( H \)), the
Fig. 13. Proposed digitally tuned current-mode universal filter using DC-CDBAs.

Fig. 14. Simulated frequency responses of the proposed DC-CDBA based current-mode universal filter of Fig. 13.

Fig. 15. BP frequency responses with different current gains $\alpha(=\alpha_1 = \alpha_2)$.

natural frequency ($\omega_0$) and the bandwidth ($\omega_0/Q$) of the proposed filter are found to be

$$H = \alpha_3,$$  

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2}{3R_1R_2C_1C_2}}.$$  

and

$$\frac{\omega_0}{Q} = \frac{\alpha_2}{3R_2C_2}.$$  

It can readily be shown from Eqs. (19)–(21) that the parameters $H$, $\omega_0$, and $\omega_0/Q$ for all the filter responses can be controlled digitally using $\alpha_3$, $\alpha_1$, and $\alpha_2$, respectively.
The proposed digitally tuned filter of Fig. 13 has been simulated using PSPICE program with $R_1 = R_2 = 1 \Omega$, $C_1 = C_2 = 2 \text{nF}$ and $x_3 = 1$ to obtain the filter response for $H = 1$. The simulation results of the LP, BP, HP and BS responses when $x_1 = x_2 = 1$ are shown in Fig. 14. From the simulations, the natural frequency is found to be $f_0 = \omega_0 / 2\pi = 45.43 \text{kHz}$, which is very close to the calculated theoretical value. Fig. 15 represents the simulated BP response of tuning $f_0$, using different values of $x = x_1 = x_2$, while $Q$ is constant at 1.732. The simulations yield the natural frequency of $f_0 \approx 10.85, 22.50, 34.17$ and $45.43 \text{kHz}$, while their theoretical values are $f_0 \approx 11.48, 22.97, 34.46$ and $45.94 \text{kHz}$, respectively. Similarly, the frequency response for the AP function, both for gain and phase, is shown in Fig. 16 and is in conformity with the theory.

5. Conclusion

A novel digitally controlled current differencing buffered amplifier (DC-CDBA) is proposed in this paper. Based on the use of the low-input resistance input stage as a core circuit, the proposed circuit is realized by the cascade connection of the current differencing circuit, the current division network (CDN) and the unity-gain voltage amplifier. A novel current division technique has also been proposed in order to provide digital control on the current gain. To demonstrate the versatility of the proposed DC-CDBA, an application on the digitally controlled current-mode universal filter has been included.

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Fig. 16. AP frequency responses with different current gains $x (=x_1 = x_2)$.

References

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