A 15 GHz 256/257 Dual-Modulus Prescaler in 120 nm CMOS

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Abstract

A completely integrated 15 GHz prescaler with programmable division ratios of 256 and 257 is presented. The prescaler uses high speed differential current-mode logic and merged AND-gates. Over a frequency band of 14 GHz the prescaler features an enhanced input sensitivity of less than −5 dBm. The circuit draws 77 mA from a single 1.5 V supply. An output buffer is also included in the circuit to drive 50 Ω loads. The circuit is manufactured in 120 nm CMOS technology.

1. Introduction

High speed programmable prescaler ICs are critical functional blocks in frequency synthesizers. These type of prescalers with two selectable divide ratios are used to extend the frequency range of programmable prescalers. For this application two divide ratios differing by one (P and P+1) are desirable.

To date, impressive results have been achieved with realizations in GaAs [1] and SiGe bipolar [2]. In contradiction CMOS P/P+1 prescalers have achieved operation frequencies up to 5.5 GHz [3]. However, the fastest of these, more than divide by two prescalers, use fixed divide ratios [4], [5] or tricky modified logic [6] which requires feedback networks between the latches.

We have designed a dual-modulus divide by 256/257 prescaler, which is the core of a PLL for 17 GHz WLAN. This circuit is optimized for high speed and high sensitivity operation. The circuit uses static CML logic for maximum bandwidth. Inputs and outputs are designed for differential operation and are suitable for 50 Ω measurement systems.

2. Circuit Design

Figure 1 shows the block diagram of the prescaler. The prescaler is based on a widely-used architecture which consists of a synchronous divide-by-four/divide-by-five stage and an asynchronous six-stage divider with a divide ratio of 64. The overall prescaler ratio is 256 or 257, depending on the level of the Modulus Control MC signal.

![Prescaler block diagram](image)

Figure 1. Prescaler block diagram

This high speed 4/5 prescaler consists of three flip-flops and requires two additional AND gates in the signal path to allow selection of the divide ratio. These gates reduce the maximum operating frequency compared to a conventional divider circuits with fixed divide ratio. As shown in figure 1 the flip-flops and the AND gates are merged to omit additional gate delays. This leads to a higher operating speed compared to the conventional topology.

Input stage matching is realized with two 100 Ω resistors and a resistive DC level shifter which also acts as an ESD protection. The input DC level is 0.9 V and was optimized for fast switching [7].
In figure 2 the master-slave flip-flop is shown. All transistors in the latch data path are of the same size and are 3/5 the width of the clock transistors. These larger clock devices increase the input sensitivity. In the high frequency part low-$V_T$ NMOS devices are used, because of their higher speed compared to regular-$V_T$ NMOS and PMOS transistors. 100 Ω Poly-silicon resistors are used as low capacitive loads for the latches. The simulated internal voltage swing is typical two times 600 mV$_{pp}$.

The current sources consist of two stacked NMOS transistors with a gate length of 180 nm. The upper transistor is a low-$V_T$ device and the bottom is a regular-$V_T$ device. This cascode configuration results in a flat current source characteristic above 0.4 V low-$V_T$ drain voltage.

The significant increase of the operating speed is achieved by using merged AND-gate flip-flops. At the same time the power consumption is reduced because the two current sources required for the separate AND gates can now be omitted. This principal is shown in figure 3. The CML AND-gate is connected in series to the clock transistor and introduces an additional logic function to the master-slave flip-flop. To ensure a symmetrical transfer function of the AND-gate a cascode transistor is used on the right data path (input B).

The asynchronous divider operates at frequencies that are factor of 4 or 5 lower than the input frequency of the prescaler. Therefore the tail current of each stage is reduced with increasing division factor. This results in a reduced power consumption. The Modulus Control input in figure 1 is connected in the middle of the OR gate chain to omit modulus control timing problems.

The dual stage output buffer in figure 4 is used to create sufficient output voltage swing. It consists of a pair of differential amplifier stages. The last differential amplifier is designed to provide enough voltage swing over a 50Ω or a capacitive load. The differential stages use internal 600 Ω and 300 Ω load resistors for DC biasing.

Differential signals are used throughout the prescaler to achieve high noise immunity. Furthermore all interconnects are kept as short as possible. Especially the lines between slave outputs and master inputs are affecting the maximum operation frequency, due to their capacitive load. The input
sensitivity of the prescaler is sufficient without an additional preamplifier at the input. A simple and robust bias network generates the bias voltages for the current sources used in all flip-flops.

### 3. Technology

The circuit is fabricated in a 120 nm CMOS technology with six-layer copper metallization. The chip size is 0.47 x 0.63 mm$^2$. The chip size is determined mainly by the pad frame. Figure 5 shows a micrograph of the prescaler. Due to fill structures in all metal layers, only diffuse outlines could be displayed. The manufactured NMOS transistors have a cut-off frequency $f_T$ of 100 GHz and a maximum oscillation frequency $f_{\text{max}}$ of 50 GHz, respectively [8].

![Figure 5. Chip micrograph (0.47 x 0.63 mm$^2$)](image)

### 4. Experimental Results

To evaluate the circuit performance the chip was mounted on a 30x30 mm$^2$ 0.51 mm RO4003 microwave substrate ($\varepsilon_r = 3.38$) with SMA connectors for input and output signals. Figure 6 shows this evaluation board mounted on a high frequency test fixture. The measured data represent the performance of the prescaler and include the loss caused by the bond wires, microstrip lines on the test board. The differential input signal was generated by a 180° hybrid coupler.

Figure 7 gives the input sensitivity versus input frequency. The circuit shows broadband performance up to operation frequencies of 14 GHz with input levels of about $-5$ dBm. The maximum operation frequency is 15 GHz at 1.5 V. This is the highest operating frequency reported so far for a dual-modulus prescaler in CMOS. The highest input sensitivity is measured at 12 GHz for both division ratios. The lack of sensitivity below 2 GHz is caused by the cut off frequency of the hybrid coupler (2 GHz) and the limited slew rate of the sinusoidal input signal. At low frequencies a square wave signal should be applied, to reach the maximum bandwidth.

![Figure 6. High frequency test fixture 30x30 mm$^2$](image)

![Figure 7. Measured prescaler sensitivity versus input power](image)

Figure 8 shows the output transient signals at 15 GHz input frequency. The measured single-ended output voltage swing on an external 50Ω load is about 250 mV$_{pp}$ for each output or 1 V$_{pp}$ at 2 pF $\parallel$ 1 MΩ probe head.
The total supply current is 77 mA at 1.5 V. Because all circuit parts share the same VSS and VDD pads, the individual currents of 4/5 divider, the asynchronous divider and the buffer can not be measured. According to simulation results, the prescaler divide by 4/5 core draws 36 mA, the asynchronous divider 30 mA, the output buffer 9 mA, and the bias network 2 mA from a single 1.5 V supply. At this supply voltage, the prescaler consumes 115 mW. Table 1 gives a summary of the prescaler data.

### Table 1. Technical data

<table>
<thead>
<tr>
<th>Maximum input frequency</th>
<th>15 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage on 50Ω</td>
<td>2 x 250 mV_{pp}</td>
</tr>
<tr>
<td>Output voltage on 2pF</td>
<td>2 x 1 V_{pp}</td>
</tr>
<tr>
<td>Divide ratios</td>
<td>256 / 257</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Supply current</td>
<td>77 mA</td>
</tr>
<tr>
<td>Chip size</td>
<td>0.47 x 0.63 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>120 nm CMOS</td>
</tr>
</tbody>
</table>

5. Conclusions

We have presented a fully integrated high speed 256/257 prescaler in 120 nm standard CMOS, which operates up to 15 GHz. The prescaler features high input sensitivity, output buffer and does not require any external adjustments. To the author’s knowledge, this is the highest reported value so far for a dual modulus prescaler realized in a CMOS technology.

6. Acknowledgments

The authors wish to thank M. Rest for supporting us with the layout and Infineon technology group for manufacturing the chip.


