Statistical Analysis of Resistive Switching Characteristics in ReRAM Test Arrays

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Abstract—**The design and the manufacturing of ReRAM test structures allow deeper insight in the performance of the FORMING, RESET, and SET operations at array level, providing details on the process induced variability of the technology, and on the potential sources of failures. Test structures allow also demonstrating the integration capability of the ReRAM technology using a CMOS-compatible process ramping up such non-volatile memory to a maturity level.**

Index Terms—**ReRAM; test-structure; array; statistics**

I. INTRODUCTION

Resistive memories (ReRAM) are one of the most promising candidates to become a key memory in several consumer and embedded applications not only from the non-volatile usage perspective, but also for FPGA-integration and neuromorphic computation [1]–[4]. From a technological standpoint, embedded HfO_2-based ReRAM devices are interesting because they offer compatibility with the standard CMOS backend-of-line (BEOL) process scheme and very fast operation times, mostly below the 100 ns limit [3].

A significant progress has been made in understanding the physics of the resistive switching behavior in the last decade, although most of the investigations were carried on 1T-1R architectures, where a select transistor device or a diode is connected the resistive switching element [1]. However, although the 1T-1R architecture demonstrated fast switching times and a resistance ratio R_{OFF}/R_{ON} (i.e., the cell resistance in the OFF- and ON-state, respectively) > 10, which is a requirement for an easy design of the memory read circuity [4], single devices are not ideal to study the statistical distribution of the inter-cell variability of memory elements. Moreover, that solution does not allow a thorough characterization of the typical issues evidenced in a memory product such as disturbs, cells interaction or cell faults due to process induced variability. Hence, in order to overcome these drawbacks, 4 kbits memory array test structures with the associated control circuitry were designed using a 0.25 μm CMOS technology node [5].

In this work we present a statistical characterization of the most relevant parameters for ReRAM technology: namely the switching voltage and the resistance ratio. The analysis of such
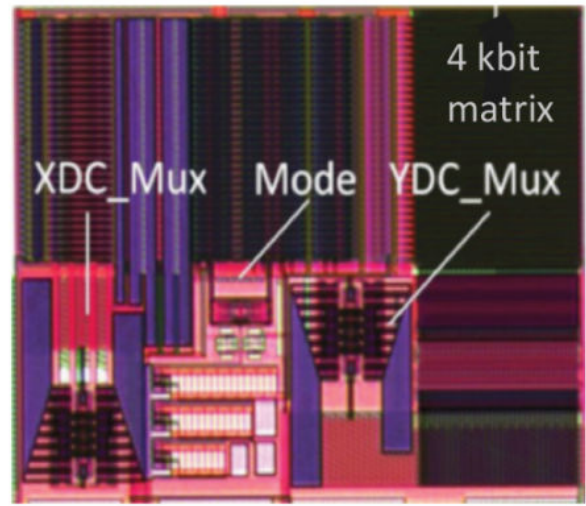

Fig. 1. Microphotograph of the 4 kbit array test structure with evidence of the constituting blocks.

parameters allows evidencing the intrinsic device-to-device variability and to investigate specific reliability concerns due to cell faults. In order to increase the consistency of the results two different realization of the arrays, manufactured with different resistive elements area, are considered.

II. TEST STRUCTURE ARCHITECTURE

The structure of the 4kbits memory array (Fig. 1) is described by four architectural blocks: the array of 4096 1T-1R ReRAM cells; a wordline (WL) address decoder (XDC MUX); a bitline (BL) address decoder (YDC MUX); and an operation control circuitry (Mode). The array schematics is depicted in Fig. 2. The memory cells are constituted by a select NMOS transistor featuring W=1.14 μm and L=0.24 μm in series to a variable resistor connected to the bitlines.

The variable resistor is a Metal-Insulator-Metal (MIM) stack (Fig. 3) fabricated on 150 nm TiN bottom electrodes deposited by magnetron sputtering with sheet resistances in the order of 10-50 Ωsq^{-1}. Next, HfO_2 films of 9nm thickness were grown
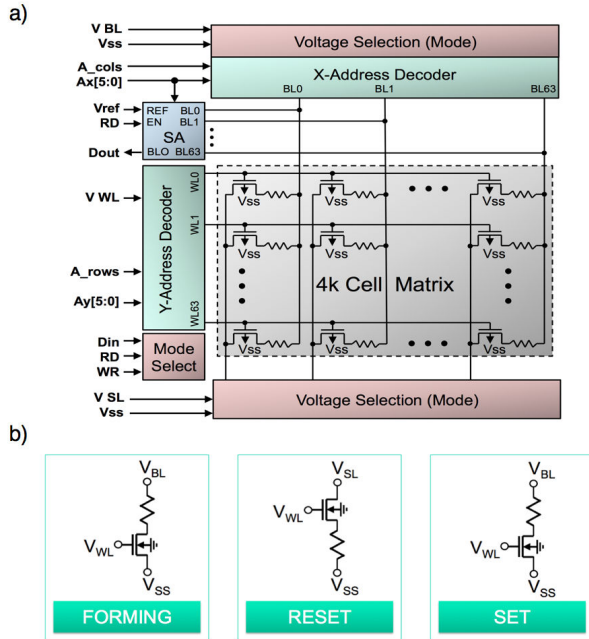
Fig. 2. Simplified block diagram of the 4 kbits memory array (a). Bias scheme for the FORMING, RESET, and SET mode (b).
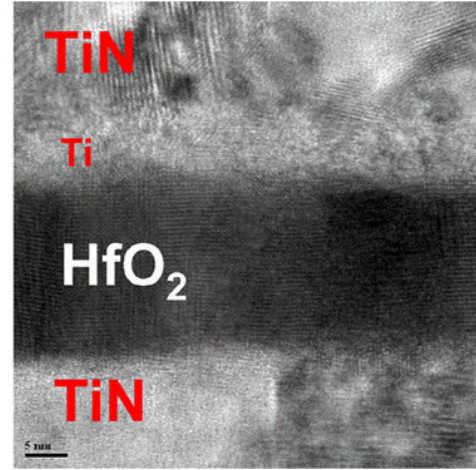

Fig. 3. Cross-Sectional STEM Image of the integrated MIM stack in the ReRAM Cell.
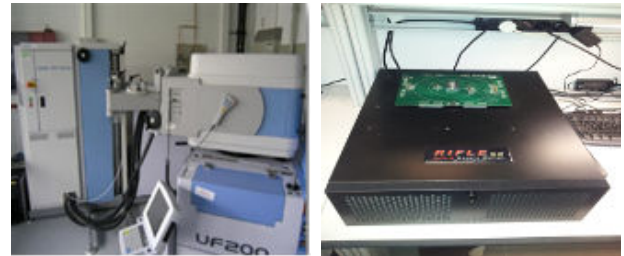

Fig. 4. Test equipments exploited for the analysis of the ReRAM array test structures. The wafer testing station (left) and the packaged samples testing station (right).

in an AVD chamber at 320 °C using Hf[N(MeEt)]$_4$ precursor and O$_2$ as reactive gas. Finally, 10 nm Ti and 150 nm TiN were sputtered onto the HfO$_2$ layer [6], [7]. To investigate the impact of the MIM area on the memory performances and variability two different arrays have been integrated using 0.6 μm^2 and 1 μm^2 resistor area, respectively. To activate the resistive switching behavior in the memory cells it is mandatory a forming process associated to nanomorphological changes and to the introduction of a high oxygen vacancy concentration in the stack, thus driving the HfO$_2$ toward a soft breakdown [8], [9]. FORMING consists in the application of a DC sweep on the BL up to V_{BL} = 3.5 V with step voltage equal to 0.025 V. To prevent hard breakdown, the saturation current of the select transistor is controlled by the WL voltage fixed at V_{WL} = 1.4 V, which translates into a compliance current almost equal to 300 μA. The forming process could be accelerated by selecting multiple rows and/or columns simultaneously using the Mode circuitry. After forming, resistive switching characteristics can be studied by additional DC voltage sweep measurements: the SET operation switches the selected ReRAM cells from a high-resistive state (OFF-state) to a low-resistive state (ON-state) by sweeping V_{BL} up to 3.5 V whereas applying 0 V to the source line voltage V_{SL}; the RESET operation, on the contrary, switches the device to the OFF-state by sweeping V_{SL} up to 3.5 V whereas applying 0 V to V_{BL}. The discrimination between SET and RESET states is performed by applying V_{WL} = 1.4 V and a read voltage V_{BL} considerably lower than the switching voltages.

III. TESTING INFRASTRUCTURE SETUP

The test environment for memory arrays characterization consists of a wafer-level test environment and of a dedicated Automated Test Equipment for packaged devices analysis (Fig. 4). The data retrieved in both testing environment are eventually compared to address possible issues on the memory arrays reliability induced by the packaging process of the test structure samples. For wafer testing it has been exploited the Advantest V93000 SOC test system, whereas for packaged devices testing it has been used the ActiveTechnologies RI-FLE system including arbitrary waveform generators and programmable measurement units resources for testing purposes. The tests performed indicated a negligible deviation between results from wafer and packaged devices.

IV. EXPERIMENTAL FINDINGS

Fig. 5 shows the result of a forming process obtained on a subset of 30 different cells: at $V_{BL} \approx 3$ V a soft break-down occurs, corresponding to the creation of a conductive filament resulting in a sudden switch of the cell resistance [9], [10]. A large variability can be observed since the most conductive cells can be formed at $V_{BL} \approx 2.5$ V, whereas the less conductive need $V_{BL} \approx 3.5$ V (these data refers to 1 μm^2 arrays). The switch to a different conduction regime is

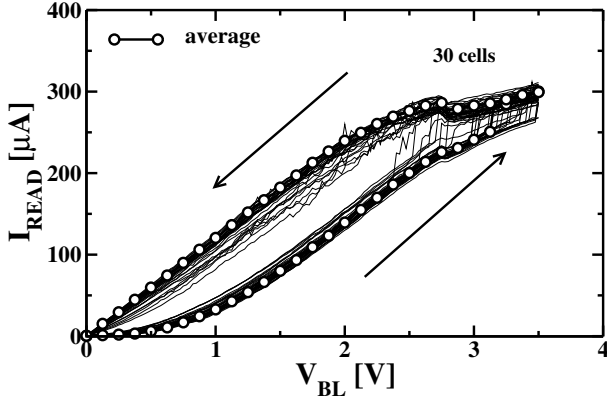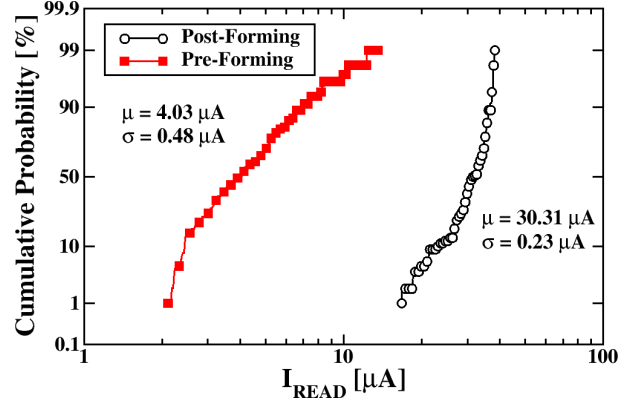Fig. 5. Example of FORMING performed on a cell in the ReRAM array test structure with $1\mu m^2$ MIM area.

Fig. 6. Distributions of the read current in a ReRAM array with $1\mu m^2$ MIM area before and after FORMING with V_{BL} = 0.3 V.

evidenced by performing a backward DC sweep, where the higher current measured confirms the proper creation of the filament. Fig. 6 depicts the cumulative probability data of the read currents measured on the entire array before and after the forming operation. Before forming the read currents are distributed around a mean value $\mu = 4.03$ μA with a standard deviation σ = 0.48 μA, whereas after forming the average current were distributed around $\mu = 30.31$ μA with a standard deviation σ = 0.23 μA. These results are obtained on arrays based on 1 μm^2 MIM area, however similar results are found in 0.6 μm^2 MIM area arrays. The analysis of the pre-forming distribution allows an indirect insight on the process induced variability in the MIM stack. In this technology, pre-forming currents larger than 10 μA usually indicate leaky cells due to fabrication issues such as the intrinsic variability of the HfO_2 deposition process [5]. This source of variability is also responsible for forming failures (i.e., cells that are unable to be formed after a single DC sweep), which is considered as a major contribution for the array yield loss. To tackle this issue a forming retry algorithm has been implemented: the basic idea is to retry the forming operation on the less conductive cells that are unable to form after the first DC sweep. Fig. 7 shows the advantages of this technique: after a single DC sweep 82% of the devices were formed, while 14% formed after the second sweep, 3% after the third and 1% after the fourth sweep. Using this technique the quasi-totality of the array has been formed correctly allowing a 17% yield gain.
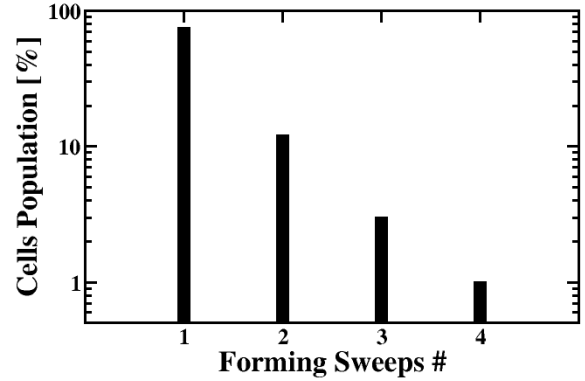
After forming, we investigated the statistical distribution of the switching process. The state switching from ON-state to OFF-state and vice versa is demonstrated in Figs. 8 and 9 representing the RESET and SET kinetics performed on 30 different cells, respectively. The RESET process starts at V_{SL} = 1.9 V, whereas the set operation occurs at V_{BL} = 1.5 V. Variability can be observed in RESET and SET switching voltage as well as previously evidenced in FORMING operation. In particular, the RESET switching voltage variability is quantified in σ = 0.25 V, whereas the SET switching voltage is quantified in σ = 0.18 V. Substantial differences are evidenced in Fig. 10 between the 0.6 μm^2 and the 1 μm^2 arrays both

Fig. 7. Statistics of the FORMING retry algorithm in $1\mu m^2$ MIM area samples. After 4 DC sweep attempts the entire cells array is formed.

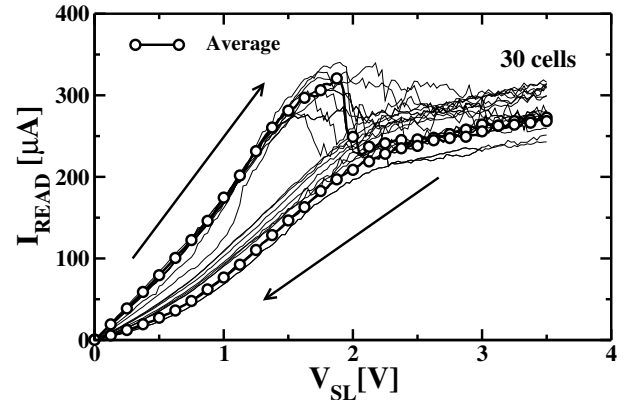

Fig. 8. RESET switching kinetics performed on 30 cells in the ReRAM array test structure with $1\mu m^2$ MIM cells area.

in terms of average switching voltage and variability. Indeed, cells with smaller MIM area are subject to a larger variability (i.e., σ = 0.4 V both for SET and RESET) of the conductive filament shape which impacts in a dominant way [8]. However, smaller MIM area implies a lowered average switching voltage for RESET and SET which has been found at V_{SL} = 1.5 V, and V_{BL} = 1.4 V, respectively [5].
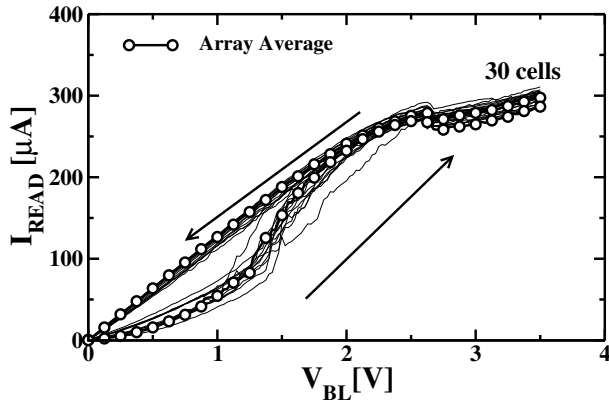
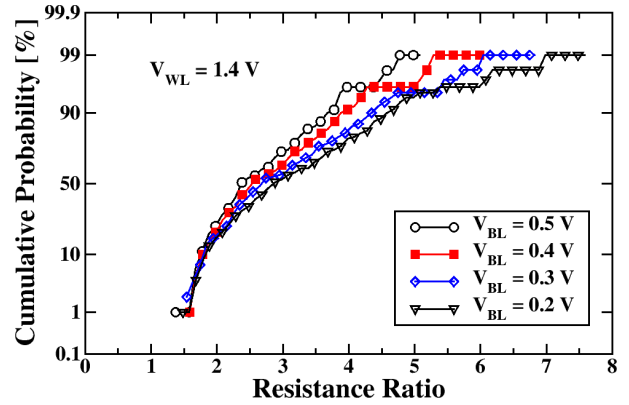Fig. 9. SET switching kinetics performed on 30 cells in the ReRAM array test structure with $1\mu m^2$ MIM cells area.

Fig. 11. Distribution of the Resistance Ratio as a function of VBL voltage in $1\mu m^2$ MIM area samples.

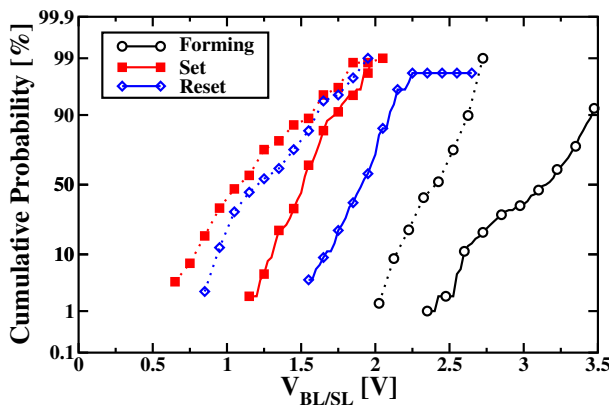
Fig. 10. Distribution of the FORMING, RESET, and SET voltages on the 4kbits ReRAM arrays. Full and dotted lines refer to the $1\mu m^2$ and to the $0.6\mu m^2$ MIM area samples, respectively.

Fig. 12. Example of anomalous SET (a) and RESET (b) kinetics in a $1\mu m^2$ MIM area cell.

In order to qualify the ReRAM technology as a good NVM product it is mandatory to evaluate the offered read margin. The read margin in ReRAM is represented by the analysis of the resistance ratio R_{OFF}/R_{ON}, which should be larger than 1.3 in order to ease the design of the memory read control circuitry [1]. Fig. 11 shows this ratio as a function of the BL voltage exploited during the read operation, proving an average value up to 3.3. A higher read margin is achieved using lower V_{BL} values although the standard deviation of the resistance ratio distribution increases significantly. No significant differences are evidenced between different realizations of the MIM element.

The array structure allows also evidencing low-probability events such as defects of the MIM stack or of the control circuitry. Fig. 12 depicts a memory cell where a defect in the MIM stack causes significant fluctuations on the SET and RESET kinetics.

V. Conclusions

The design and the manufacturing of ReRAM test structures allow deeper insight in the performance of the FORMING, RESET, an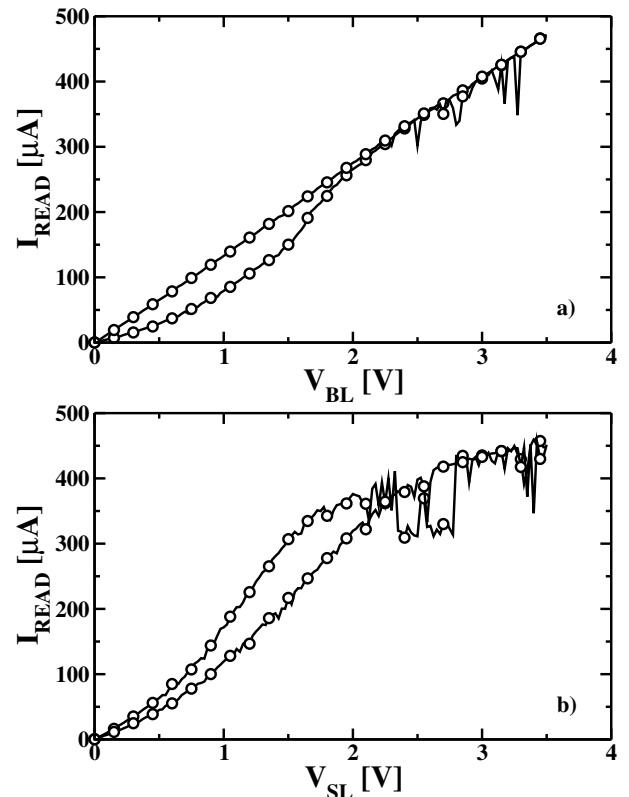d SET operations at array level, providing details on the process induced variability of the technology, and on the potential sources of failures. Test structures allow also demonstrating the integration capability of the ReRAM technology using a CMOS-compatible process ramping up such non-volatile memory to a maturity level.

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