Time-shift Control of LLC Resonant Converters

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Abstract

This paper describes a new control technique for resonant converters that outperforms the direct frequency control (DFC) method implemented in all today’s commercially available control ICs. When applied to LLC resonant converters, the resulting dynamic behavior is that of a low-Q second-order system or that of a first-order system, depending on the operating conditions. Thus closing the control loop to meet stability and dynamic performance specifications becomes considerably easier. Due to its complexity, the mathematical description is limited; the approach is essentially empirical with an extensive use of simulations.

1. Introduction

Many different control methods for resonant converters have been described in the literature [1]-[9]. However, all the integrated controllers for resonant converters available in the market today use the direct frequency control (DFC) method, where the feedback signal directly controls a local oscillator, which the switching frequency of the half (or full) bridge is locked to.

Although simple, intuitive and very easily realizable in integrated form, this method is not devoid of issues. A major one is related to converter’s small-signal dynamics. With reference to the LLC resonant converter (figure 1), today’s most popular resonant converter, the analysis carried out in [10] shows that it is a three-pole system. Additionally, the way these poles move depends on whether the converter is operating below or above resonance and on the load. As a result, the design of a compensator that closes the control loop achieving adequate stability margin and input ripple rejection, as well as acceptable load transient response under all the specified operating conditions is not an easy task.

Fig. 1. LLC resonant half-bridge converter

The novel method proposed in this paper, which has been called time-shift control (TSC), alleviates this issue. In fact, simulations show that the power stage is turned into a low-Q second-order system in some conditions or, in other cases, into a first-order system, plus the zero due to the ESR of the output capacitor. Since dominant pole approximation is allowed, the compensator design is considerably simplified.

The TSC methodology, however, does not solve other issues of the DFC method. One is the dependence of all converter variables on the input voltage, which remains essentially the same as with DFC. Another one is that both DFC and TSC are not robust against parameter variations in the resonant tank: their tolerance shifts the closed-loop operating frequency range (in the case of DFC) or time-shift range (in the case of TSC) of the converter, and any limitation imposed on the control variable must account for this.

2. Time-shift control (TSC)

2.1. The methodology

The TSC methodology consists in controlling the amount of time \( T_D \) elapsing from a zero-crossing of the tank current to the next switching of the half (or full) bridge (i.e. the zero-crossing of the first harmonic of the applied square-wave voltage) as shown in figure 2a. Note that, to achieve soft-switching for the switches Q1 and Q2, the resonant tank current must lag behind the applied square-wave voltage; so, the voltage zero-crossing commanded at the end of \( T_D \) must have the opposite sense with respect to the current zero-crossing that initiated \( T_D \). Figure 2a shows, for example, a negative-going zero-crossing of the applied voltage (the zero reference for its ac component is \( V_{in}/2 \)) commanded after a positive-going zero-crossing of the tank current.
It is important to note that the time-shift $T_D$ imposed by the control circuit is included between $T_{sw}/4$ (under no-load conditions, when current is in quadrature to voltage, figure 2b) and $T_{sw}/2$ (at the boundary with capacitive-mode operation, when current and voltage are in-phase, figure 2c), being $T_{sw}$ the switching period of the converter.

Conceptually, with TSC an inner loop is closed and the outer loop that regulates the output voltage provides the reference for the inner loop. This inner loop is illustrated in figure 3.

The feedback variable is the tank circuit current $i_R$, whose zero-crossings are used as the starting point for the time-shift, while the input quantity to the tank circuit is the applied square-wave voltage $v_{HB}$. In the frequency domain, therefore, the tank circuit is represented by its input admittance $Y(j\omega)$. The block $e^{-j\omega T_D}$ represents the time-shift imposed by the control circuit, while the block designated with $D(I_{Rpk})$ represents the inverter action of the half (or full) bridge.

![Fig. 2.](image)

**Fig. 2.** a) concept of time-shift control; b), c) range of the control variable $T_D$

$T_D$ is the reference for the loop, while converter’s input voltage $V_in$ can be seen as a disturbance.

Since the tank circuit responds primarily to the first harmonic of $v_{HB}$ and negligibly to the higher order harmonics, this loop can be analyzed using the describing function approach [11]. With this method, the non-linear part of the system, i.e. the inverter action of the half (or full) bridge, which in control system terminology is a relay, is represented in the frequency domain by its describing function $D(I_{Rpk})$, where $I_{Rpk}$ is the peak value of the first harmonic of $i_R$. In our case, since the ac voltage applied to the resonant tank oscillates between $\pm V_{in}/2$, it is:

$$D(I_{Rpk}) = \frac{2V_{in}}{\pi I_{Rpk}}. \quad (1)$$

According to the describing function method, the intersection point of the loci of the negative inverse of the describing function (1) and of the transfer function of the linear blocks in the loop ($Y(j\omega)e^{-j\omega T_D}$ in our case) defines a possible limit cycle. The values of $I_{Rpk}$ and of the angular frequency $\omega$ at the intersection point define the amplitude and the frequency of the oscillation, respectively, provided the limit cycle is stable.

Stability can be easily assessed: if the points near the intersection and along the increasing $I_{Rpk}$
side of the curve $-1/D(I_{pk1})$ are not encircled by the locus of the linear part, then the corresponding limit cycle is stable.

Figure 4 shows the Nyquist plots of $-1/D(I_{pk1})$ and $\tilde{Y}(j\omega)e^{-j\omega T_D}$, where $\tilde{Y}(j\omega)$ is the tank circuit’s input admittance normalized to the tank circuit’s characteristic admittance $Y_R = (Cr/Ls)^{1/2}$.

Due to the delay term $e^{-j\omega T_D}$, there are actually infinite intersections and so possible limit cycles; however, considering that $T_{sw}/4 \leq T_D \leq T_{sw}/2$, the only significant intersection is the one falling in the $\omega$ range $(\pi/2 T_D, \pi/T_D)$ shown in figure 4. The corresponding limit cycle, according to the above mentioned criterion, is stable, and this holds true regardless of $T_D$ (provided it is in the correct range) and of the parameters in $\tilde{Y}(j\omega)$.

The driving signals for Q1 and Q2, HG and LG, are locked to this triangular wave as shown in the timing diagram in figure 5. The dead-times between the HG and LG pulses are neglected because not significant in this context.

Modulating the current $I_p$ changes the ramp slope and, then, the oscillation frequency $f_{sw}$, thus performing DFC.

Therefore, TSC features the same property of absolute stability as the self-sustained oscillation (SSO) technique illustrated in [7]-[8]; unlike TSC, SSO controls the phase-shift between the resonant tank current and the applied square-wave voltage, so that it enjoys control robustness as well. However, the implementation of the modulator is relatively complex. The TSC modulator, instead, is obtained with a simple modification in the operation of the oscillator included in a standard control IC.

2.2. TSC modulator implementation

Figure 5 shows the block diagram of the oscillator in a commercially available resonant controller IC, the L6599A, which implements DFC.

A capacitor, $C_T$, is alternately charged and discharged with the same current $I_p$ whenever the voltage across $C_T$ falls below a lower threshold $V_i$ and exceeds an upper threshold $V_p$, respectively. In this way, a series of contiguous ascending and descending ramps is generated, which results in a symmetrical triangular waveform across $C_T$.

The driving signals for Q1 and Q2, HG and LG, are locked to this triangular wave as shown in the timing diagram in figure 5. The dead-times between the HG and LG pulses are neglected because not significant in this context.

Modulating the current $I_p$ changes the ramp slope and, then, the oscillation frequency $f_{sw}$, thus performing DFC.

Figure 6 shows how the oscillator of figure 5 can be modified to perform TSC. A comparator has been added that senses the CS signal, voltage image of the tank current $i_R$ (derived, for example, with a resistor connected in series to it). This comparator, along with the NOR gate, enables the charge of $C_T$ when CS (i.e. $i_R$) is negative and, through the AND gate, its discharge when CS ($i_R$) is positive.
In this way, each ramp across \( C_T \) starts after a zero crossing of CS (\( i_a \)) and lasts until it crosses either \( V_c \) or \( V_{in} \), which causes the half (or full) bridge to be switched. Afterwards, the voltage on \( C_T \) stays flat until the next zero-crossing of CS (\( i_a \)), when another ramp starts. With this mechanism, the duration of a ramp does not determine half the switching period \( T_{sw}/2 \) and, ultimately, the switching frequency \( f_{sw} \), as with the modulator in figure 5. It determines the distance in time \( T_D \) between a zero-crossing of the tank current and the next switching of the half (full) bridge:

\[
T_D = C_T \frac{V_p - V_v}{I_F}. \tag{2}
\]

In this case, modulating \( I_p \) modifies this distance in time, thus performing TSC. The consequent change in frequency is not directly controlled and depends on the phase-shift between \( i_a \) and \( V_{HB} \).

From (2) it is apparent that the TSC modulator is a non-linear block, thereby its gain will change with the operating point (i.e. with \( I_p \)). However, it does not introduce frequency dependence, at least in the frequency range that is interesting for the design of a compensator. The small-signal gain is found by differentiating (2):

\[
G_{Mod} = \frac{\dot{V}_D}{I_F} = -C_T \frac{V_p - V_v}{I_F}. \tag{3}
\]

where \( \dot{\cdot} \) denotes the signal component of \( x \).

### 3. TSC dynamic behavior

#### 3.1. Theoretical considerations

The block diagram of the feedback loop that controls the output voltage of an LLC resonant converter operated with TSC is shown in figure 7.

![Block diagram of the overall control loop](image)

**Fig. 7.** Block diagram of the overall control loop

\( G_i(j\omega) \) is the small-signal transfer function of the power stage, i.e. of the closed-loop control system illustrated in figure 3. Its \( T_D \) reference value is provided by the TSC modulator, whose transfer function \( G_{mod} \) is given by (3).

The modulator is current controlled and a transconductance block \( g_m \) converts the control voltage \( v_c \) (error amplifier output) to the controlling current \( i_p \).

\( G_i(j\omega) \) is the transfer function of the compensated error amplifier. Once all the other blocks in the loop are known, \( G_i(j\omega) \) is designed to meet a design target normally given as phase margin and crossover frequency of the open-loop system.

\( G_i(j\omega) \) can be expressed as follows:

\[
G_i(j\omega) = \frac{v_{out}}{\dot{V}_{in}} = \frac{\dot{v}_{out}}{\dot{f}_{sw}} \frac{\Phi_Z}{T_D}. \tag{4}
\]

Note that the first factor on the right-hand side of (4) is the small-signal transfer function of the power stage with DFC.

The term \( \Phi_Z \) in the other factors is the phase-shift between the tank current and the applied squarewave voltage \( v_{HB} \). In the spirit of the “first-harmonic approximation” approach, as already done in section 2.1 with the describing function method, \( \Phi_z \) is the phase of the input impedance \( Z_i(j\omega) = 1 / Y_i(j\omega) \) of the tank circuit. The second factor is, therefore, the reciprocal of the small-signal expression of \( Z_i(j\omega) \), again with DFC.

The third factor relates phase-shift to time-shift. It can be calculated with the aid of figure 2a:

\[
\Phi_Z = \pi - \frac{T_p/2}{T_s/2} \rightarrow \frac{\Phi_Z}{T_D} = -2\pi f_{sw} = -\omega. \tag{5}
\]

#### 3.2. Empirical approach

As can be inferred from (4), the analytical derivation of \( G_i(j\omega) \) is a challenging task. For this reason, an empirical approach has been preferred in this context: the behavior is characterized by means of a number of simulations carried out on an exemplary LLC resonant converter in both the time and the frequency domains.

The key electrical parameters of the exemplary LLC resonant converter are listed in Table 1. In the time-domain simulations a small step-change \( \Delta V_c \), << \( V_c \), is given to the steady-state value \( V_c \) and the resulting change \( \Delta V_{out} \) in \( V_{out} \) is observed. The amplitude of \( \Delta V_{out} \) and the 10-90% rise/fall times of the response are noted. To minimize the effect of the output voltage ripple on the measurement of \( \Delta V_{out} \), the reading is done via two cascaded second-order filters (40 kHz cut-off frequency and 0.7 damping ratio each).

In the frequency-domain simulations, the test frequency is swept from 10 Hz to 30 kHz. All simulations are carried out at the extremes of the input voltage range and at the nominal input voltage (where the converter runs close to resonance) with 100%, 50% and 10% load.
Parameter | Symbol | Value | Unit
--- | --- | --- | ---
Dc input voltage range | $V_{in,min}$ - $V_{in,max}$ | 300 - 440 | V
Nominal dc input voltage | $V_{in}$ | 400 | V
Regulated output voltage | $V_{out}$ | 12 | V
Maximum output power | $P_{out,max}$ | 250 | W
Transformer turn-ratio | $a$ | 16:1 | ---
Series resonant inductor | $L_s$ | 105 | µH
Parallel resonant inductor | $L_p$ | 560 | µH
Resonant capacitor | $C_r$ | 39 | nF
Output capacitor | $C_{out}$ | 8 x 470 | µF
Output capacitor’s ESR | $R_C$ | 38/8 | mΩ
HB node parasitic capacitance | $C_{int}$ | 180 | pF
Dead-time of driver circuit | $T_d$ | 300 | ns
Q1 and Q2 on-resistance | $R_{DSS(on)}$ | 0.35 | Ω
Secondary diode forward drop | $V_F$ | 0.5 | V
Oscillator capacitor | $C_T$ | 330 | Ω
Oscillator voltage swing | $V_p$ - $V_v$ | 3 | V
V-I block transconductance | $g_m$ | 233 | µS

Table 1. Key parameters of the exemplary LLC resonant HB converter used in the simulations

The time domain simulations, shown in the diagrams of figures 8 to 10, point out an open-loop response that is always overdamped.

However, a close look at the step response with 100% load and $V_{in} = V_{in,min}$, shows that the rise and fall times of $V_{out}$ are not compatible with a single time constant. At lower load and/or higher input voltage, instead, the step response fits an exponential curve very well.

This suggests that $G_2(j\omega)$ might have two real poles, one of which tends to move to high frequency at high input voltage and/or light load.

![Fig. 8. Time-domain simulations at 100% load with $V_{in} = 300, 400, 440$ V; upper traces: $V_c$; lower traces: $V_{out}$ (red), filtered $V_{out}$ (blue)](image)

Fig. 9. Time-domain simulations at 50% load with $V_{in} = 300, 400, 440$ V; same traces as in figure 8

![Fig. 10. Time-domain simulations at 10% load with $V_{in} = 300, 400, 440$ V; same traces as in figure 8](image)

This is confirmed by the results of the frequency-domain simulations in figure 11, where gain and phase lag associated to $\frac{V_{out}}{V_c}$ are shown.

The Bode plots show clearly two real poles at 100% load and $V_{in} = V_{in,min}$. However, with respect to a single pole plot, the extra phase lag at the 3-dB cutoff frequency is only $\approx 6^\circ$. This means that the two poles are separated by about a decade and that using dominant pole approximation is definitely possible at frequencies below crossover (low-Q second-order system).
At lower load and/or higher input voltage, the Bode plots become essentially those of a first-order system.

In all Bode plots, besides the zero due to the ESR of $C_{out}$, an RHP zero seems to lie beyond $\approx 20 \text{ kHz}$: gain slope tends to flatten out or even rise, while phase lag further increases.

Still at 100% load and $V_{in} = V_{in,\min}$, crossover occurs with the lowest phase margin ($\approx 40^\circ$). Therefore, designing the compensator for closed loop stability in these conditions ensures closed-loop stability under all conditions.

4. Summary

A novel control technique for resonant converters, the Time-shift control (TSC), has been presented and its application to LLC resonant converters studied. Large signal behavior and stability have been analyzed with the describing function method. Its dynamic behavior has been characterized by simulations with PSIM and found to be either that of a low-Q second-order system or that of a first-order system. Dominant pole approximation can be used as far as the design of a compensator is concerned.

A possible TSC modulator, derived from the oscillator of a commercially available control IC for resonant converters has been presented. Although not solving all the issues related to the presently most used control technique (Direct frequency control, DFC), the TSC method offers significant improvements to stability.

5. Literature