Electromigration Characteristic of SnAg3.0Cu0.5 Flip Chip Interconnection

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Abstract
Electromigration is a reliability concern of microelectronic interconnections, especially for flip chip solder bump with high current density applied. This study shows that with the line-to-bump geometry in a flip chip solder joint, the current density changes significantly between the Al trace and the bump, while the current crowding effect generates more heat between them. This large Joule heating under high current density can enhance the migration of Sn atoms at the current entrance of the solder bump, and cause the void formation at the entrance point. The present study finds two kinds of electromigration failure modes at the cathode/chip side of the solder bump: the pancake-like and the cotton-like void. The experimental finding shows that the effects of polarity and tilting are key factors to observe in the electromigration behavior of SnAg3.0Cu0.5 solder bumps. Consequently, this study has designed a three-dimensional numerical model and a corresponding test vehicle to verify the numerical finding. The maximum current density is simulated through the finite element method (FEM) to provide a better understanding of local heat and current crowding. This study finds that the current crowding ratio is reduced linearly while the void formation is increased. Furthermore, it is concluded that there is a linear relationship between the growth of the intermetallic compound (IMC) layer and the applied current density at the anode/substrate side.

Introduction
The demand of flip chip technology in high-density packaging has increased dramatically. With the trend of package size minimization, the solder joint became smaller in size, and this thus increased the current density. Consequently, electromigration has become a serious reliability issue in flip chip solder joint, especially in lead-free solder joint. Electromigration is considered as the transportation of metal ions that move in the applied electric field [1-3]. Previous studies about current crowding induced by Joule heating have shown that it accelerates the reliability failure of the flip chip solder joint [4-8]. The polarity effect of lead-free solder in a V-groove sample and flip chip bump has been studied for a better understanding of the impact of local atomic flux [3,6,9]. However, the IMC thickness of the anode side of the flip chip bump needs further investigation. In addition, very few literatures report the tilting effect of the flip chip bump; therefore, it is necessary to provide more information for a deeper understanding of this subject.

The numerical simulation on current crowding induced by Joule heating in solder bump under electric current stressing is reported in previous studies. Through the numerical analysis, the effect of current density distribution and void propagation is provided [7,10-12]. However, no studies regarding a three-dimensional void propagation simulation have been made to provide a better understanding of void propagation mechanism of the solder bump. The growth of the IMC layer in the eutectic solder of Blech specimens and the lead-free solder of a V-groove sample has been reported previously. Similarly, the growth mechanism of the IMC of solder joints after thermal aging has also been evaluated [9,13-15]. The failure modes of the flip chip solder joint under high electrical current density are studied experimentally [16-17]. However, the IMC thickness and the failure modes of the lead-free flip chip solder bump need more discussion. Therefore, the purpose of this study is to provide the abovementioned missing information about the electromigration characteristic of the SnAg3.0Cu0.5 flip chip solder bump.

Experimental Procedure
The test vehicle consisted of SnAg3.0Cu0.5 solder bumps and daisy-chained chips which were prepared as follows: the under bump metallurgy (UBM) on the chip side consists of 0.8 µm Cu, 0.3 µm Ni(V), and 0.4 µm Ti. The bumps mounted on the BT substrate and underfilled consist of 0.05 µm Au, 3 µm Ni, and 32 µm Cu. FIG. 1. shows the schematic diagram of the solder joint structure. The test temperatures were 125, 150, and 165 °C, respectively, and the current densities were 7.38x10³, 1.21x10⁴, and 1.68x10⁴ A/cm², respectively.

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FIG. 1. Schematic diagram of the bump used in this study

Joule heating was investigated by calculating the temperature coefficient of resistance (TCR). It was found that normally, the real temperature would be around 10°C higher than the test temperature. This result implies that the effect of Joule heating is significant for the test.

The current crowding distribution in a solder bump was simulated by a three-dimensional model. The resistivities of the materials used in this simulation as Al, Cu, SnAg3.0Cu0.5, Ti, Ni(V), Ni, and Au were 2.74, 1.68, 10.4, 54, 63.2, 7.4, and 2.35 µΩ-cm, respectively. The direction of the applied current was the same as that in the real experimental sample, in which the electric current flowed from the bottom Cu trace to the top Al trace, implying that the electron flow was in the opposite direction.

Results and Discussion

Current crowding which is induced by Joule heating plays a critical role in the electromigration failure of a flip chip solder bump. Due to the particular line-to-bump geometry in a flip chip solder joint, the current density changes significantly between the Al trace and the bump. The diameter of the solder bump is about two orders of magnitude larger than that of the Al trace’s thickness, and this induced the maximum current density of the Al trace which is typically higher by one to two orders of magnitude than that of the solder bump. Current crowding occurs at the entrance of the Al trace into the bump.

Joule heating is a common phenomenon in electronic devices. This involves the passing of an electrical current through a material, and the resistivity of the material causes the generation of heat. When current crowding occurs, it can generate more heat in the region where there is abrupt geometry change, and the real temperature of the solder bump must be higher than that of the test temperature. In this study, the real temperature measurement of the solder bump was around 10°C, higher than that of the test temperature, which resulted in a higher diffusion rate for the material in the solder bump. This result implies that real temperature measurement is important for a better understanding of the electromigration mechanism.

The high temperature generated by Joule heating can enhance the migration of Sn atoms at the current entrance of the solder bump, and causes the void formation at the entrance point. Voids at the contact area do not only increase the localized maximum current density but also induce significant Joule heating continuously. When the void was extended across the contact of the line-to-bump area, the contact area was decreased, and the heat dissipation from the chip through the solder bump and then to the substrate also became less. Since the void reduced the effective contact area, it blocked the heat transfer from the chip to the substrate and the original electrical patch. Both electrical and thermal effect changed their transmission path from the left to the right corner.

According to the feasibility for electromigration of the solder bump [3], solder bump should be under the highest stressing condition during the test condition of this study, and consequently, the electromigration-induced void should occur at the current entrance of the solder bump. Then the electromigration-induced void was propagated along the interface between UBM and the solder bump. Eventually, this led to an open failure. FIG. 2 shows a sequence of the formation and growth of voids in the SnAg3.0Cu0.5 solder bump. FIG. 2(a) indicates a line-to-bump system with the transparent Al trace, and FIG. 2(b) points to that when the Al trace and UBM are hidden. In this study, the width of the Al trace is 100 µm, the contact diameter between UBM and the solder bump is 60 µm, and the maximum current density of the Al trace is around 20 times higher than that of the solder bump. FIG. 2(c) illustrates the current-crowding-induced void which starts at the entry point of the cathode/chip side of the junction between UBM and the solder bump. FIG. 2(d) - 2(e) demonstrate the growth of voids of the SnAg3.0Cu0.5 bump.

FIG. 2. Simulation of current densities in (a) line-to-bump system; bump system (b) without the void occurring; (c) with 0.4 %; (d) with 1.6 %; (e) with 3.1 % void at the contact window area. Current crowding occurs in the vicinity of the junction of the solder bump and UBM. The eliminated solder is illustrated in the upper-right corner of each diagram.
An experimental test vehicle was used to verify the numerical current crowding simulation and find the starting point of the void. For the purpose of investigating the formation of the starting point of the void, and the IMC accumulation location and its composition, scanning electron microscopy (SEM) and energy dispersive X-ray (EDX) were done. The cross-sectional SEM images of the solder bumps revealed that the Al trace and (Ni,Cu)₃Sn₄ IMC composition remained integral after 7.38x10³ A/cm² to 1.68x10⁴ A/cm² current density applied at 150°C for 450 hours. Furthermore, a void formed at the entry point of the cathode/chip side of the solder bump along the electron flow path.

To quantitatively obtain the current density under current crowding phenomenon, FEM is the most widely used numerical analysis. Therefore, a dimensionless parameter was proposed in this study. The current crowding ratio of the bump system was defined with the maximum current density of line-to-bump system over the average current density of the top layer of the bump. The current crowding ratio of the bump system almost reached a constant level while varying the applied current [8]. This result implies that the current crowding ratio is only influenced by the system geometry. However, the current crowding ratio of the bump system was decreased linearly while the void area was increased. This decrease level is shown in FIG. 3. The three-dimensional simulation results from this study indicate a new finding on current crowding, which differs from the two-dimensional current crowding phenomenon, FEM is the most widely used for 450 hours. Furthermore, a void formed at the entry point of the cathode/chip side of the solder bump along the electron flow path.

The electron flow from the Al trace into the bump will conform to the shortest distance. This phenomenon implies that the electron will flow into the bump at the upper-left corner through a point area, and flow out of the bump at the bottom-right corner. FIG. 2(b) shows that there is a hot spot at the entry point between UBM and the bump. Once the void is formed, the electron will flow from the Al trace into the bump through a line area, but not through the point area anymore. Therefore, the electron flow contact line area between the Al trace and the bump increases, resulting in less current crowding of the line-to-bump system. The slowdown of the current crowding phenomenon continuously accompanies the void propagation until the electron flow contact line area between the Al trace and the bump starts to decrease. Specifically, the current crowding phenomenon of the line-to-bump system will be decreased in the forepart of the void propagation, and the current crowding level will be increased during the latter part of the void propagation.

However, the level of the current density distribution continuously grows during the void propagation at the top layer of the bump. This is because during the void propagation of the bump, the less contact area between UBM and the bump results in severer current crowding. In other words, the average current density of the top layer of the bump will be increased during the void propagation. The difference of the maximum current density of the line-to-bump system and the average current density of the top layer of the bump rises to linearly decrease the current crowding ratio. This linear relationship implies that if the maximum current density of the line-to-bump system can be found, the average current density of the top layer of the bump can be obtained.

**FIG. 3. Current crowding ratio of the bump system during electromigration-induced void propagation**

During this study, two electromigration-induced failure modes of the flip chip solder joint were proposed through the SEM and EDX analysis. FIG. 4(a) illustrates the electromigration-induced pancake-like void failure, and FIG. 4(b) illustrates the electromigration-induced cotton-like void failure at the cathode/chip side. The failure mold and void propagation mechanism of the pancake-like void have been discussed clearly in the previous paragraphs. However, the failure mode and void formation mechanism is different in the cotton-like void. EDX analysis on the same positions of these two types of failure bump and the results are shown in TABLE I. For the pancake-like void failure bump, the material composition in positions 1 and 3 is Cu-Ni-Sn IMC; in position 2, it is 99.6% Sn and 0.6% Ag. For the cotton-like void failure bump, the material composition in positions 1 and 2 contains lots of Al and Sn elements but few Ti, Ni, Cu, and Ag elements; position 3 is comprised of a Cu-Ni-Sn IMC. It was noted that the same IMC composition of (Ni,Cu)₃Sn₄ was formed at the anode/substrate side regardless of the void failure mode that occurred.

For the pancake-like void failure bump, position 1 is at the cathode/chip side. After reflow and current stressing, the thin Cu UBM was dissolved into the solder bump; after which, the solder was reacted with the Ni layer to form Cu-Ni-Sn IMC. Parts of the dissolved Cu were then migrated to the anode/substrate side to form Cu-Ni-Sn IMC in position 3. For the cotton-like void failure bump, it was found that the Al trace, UBM, and the top layer of the solder collapsed, and the Cu was migrated to the anode/substrate side in position 3. This was because the bump had a crack at the cathode/chip side before or during the current stressing. The contact area was limited to this crack. During the current stressing, electric resistance was raised due to the reduction of the contact area in the cathode/chip region. Current crowding and Joule heating were also significantly increased, resulting in the ultra-high temperature at the cathode/chip side which further caused the collapse of the Al trace and the UBM. The cotton-like void failure mode IMC layer at the anode/substrate side was always thicker than that of the pancake-like void failure mode. This was because the higher temperature that occurred in the cotton-like void failure mode enhanced the electromigration effect from the cathode to the anode side.
FIG. 4. Cross-sectional SEM images of the solder bump with (a) pancake-like void; (b) cotton-like void electromigration failure mode.

TABLE. I. EDX analysis results of the pancake-like and cotton-like voids, which correspond to FIG. 4

<table>
<thead>
<tr>
<th>Position</th>
<th>Bump (a)</th>
<th>Bump (b)</th>
<th>Bump (a)</th>
<th>Bump (b)</th>
<th>Bump (a)</th>
<th>Bump (b)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Al</td>
<td>Ti</td>
<td>Ni</td>
<td>Cu</td>
<td>Sn</td>
<td>Ag</td>
</tr>
<tr>
<td>1</td>
<td>0.0</td>
<td>0.0</td>
<td>16.7</td>
<td>30.1</td>
<td>53.0</td>
<td>0.2</td>
</tr>
<tr>
<td>2</td>
<td>52.8</td>
<td>1.9</td>
<td>5.0</td>
<td>4.5</td>
<td>35.6</td>
<td>0.2</td>
</tr>
<tr>
<td>3</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>99.4</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>36.4</td>
<td>3.7</td>
<td>0.5</td>
<td>4.2</td>
<td>54.3</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td>0.0</td>
<td>0.0</td>
<td>13.0</td>
<td>28.7</td>
<td>57.8</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>0.0</td>
<td>10.8</td>
<td>28.6</td>
<td>60.4</td>
<td>0.4</td>
<td></td>
</tr>
</tbody>
</table>

The evidence of the crack before or during the current stressing to form a cotton-like void failure is shown in FIG. 5. The analysis indicated that the maximum tensile or compressive stress was generated in the chip side region. Therefore, the crack could only appear at the chip side. Once a crack exists before or during current stressing, Joule heating would induce ultra high temperature to melt or collapse the margin of the crack. This means that the current crowding-induced void mechanism dominated the pancake-like void bump failure, and the crack-induced void mechanism dominated the cotton-like void bump failure.

FIG. 5. Cross-sectional SEM images of solder bumps at 150 °C with an applied current of (a) 1.68×10^4 A/cm^2 (b) 1.21×10^4 A/cm^2. Cotton-like voids formed along the cracked path.

Because of the fast diffusion and rapid reaction of Ni and Cu in Sn [3], IMC formed at both the cathode and anode sides. However, under the current stressing and electromigration effect, the interaction at the cathode and the anode became different. Electron flowed into the cathode and enhanced the IMC dissolution, whereas in the anode side, the reverse was observed. Electron flowed out of the anode and enhanced the IMC formation. In this study, the polarity effect of the SnAg3.0Cu0.5 solder bump was observed as shown in FIG. 6. Electron flowed into the cathode/chip side and out of the anode/substrate side. The polarity effect was obvious. This phenomenon was caused by the Sn atom of the solder at the cathode side to the anode/substrate side by means of electromigration. The increase in Sn concentration at the cathode side and the anode side induced a phase transformation. FIG. 6(a) shows the cross-sectional SEM images of the solder bumps at 150°C without current stressing. The IMC thickness at the cathode and the anode were similar, which implies that no polarity effect occurred, as compared to the IMC thickness at the anode side in FIG. 6 which is that of current stressing condition. The larger void observed in the cathode, the thicker the IMC at the anode side. This phenomenon is shown in FIG. 6(b) - 6(c). This was because of the less contact area between UBM and the bump, which induced severe Joule heating and then enhanced the electromigration polarity effect.

FIG. 6. Cross-sectional SEM images of the solder bumps at 150°C with an applied current of (a) no-current stressing; (b) 1.21×10^4 A/cm^2 with the smaller void; (c) 1.21×10^4 A/cm^2 with the smaller void.
with the larger void at the cathode/chip side. The IMC thickness of each anode/substrate side was different. The polarity effect was obvious.

FIG. 7. Cross-sectional SEM images of solder bumps with an applied current of (a) no-current stressing at 125 ℃; (b) 1.68×10^4 A/cm^2 at 125 ℃ with the smaller void; (c) 1.68×10^4 A/cm^2 at 150 ℃ with the larger void at the cathode/substrate side. The IMC shape and thickness of each anode/chip side were different. The tilting effect was obvious.

On the contrary, electron flowed into the cathode/substrate side and out of the anode/chip side. The tilting effect is obviously shown in FIG. 7. The void in the cathode/substrate side enhanced the growth and clustering of IMC at the outgoing points of the anode/chip side along the electron flow path. FIG. 7(a) shows the cross-sectional SEM images of solder bumps at 125 ℃ without current stressing. The IMC shape and thickness at the cathode and anode were similar, which implies that no tilting effect occurred. In addition, the larger the void observed at the cathode/substrate side, the more severe were the tilting and clustering shape at the anode/chip side. The IMC layer at the anode/substrate side was much thicker with current than when no current was applied. The IMC layer thickness at the anode/substrate side of the cotton-like void failure mode was always thicker than that of the pancake-like void failure mode. This was due to the serious Joule heating that occurred in the cotton-like void failure mode which induced more Sn atoms to migrate from the cathode to the anode side to form Cu-Ni-Sn IMC. The high current density on the cathode/chip side implies more serious Joule heating, which subsequently accelerated the growth of the IMC at the anode/substrate side. FIG. 8 shows that the IMC layer thickness increased at the anode/substrate side when the applied current density was increased.

FIG. 8. IMC thickness with the applied current density at various electromigration failure modes at 150 ℃ for 450 h.

Conventionally, the growth rate of the IMC layer and the square root of time can be expressed as follows:

\[ d = d_0 + \sqrt{Dt} \]  

Where \( d \) is the thickness of IMC increase, \( d_0 \) is the initial thickness of the IMC layer, \( D \) is the diffusion coefficient of the IMC layer, and \( t \) is the heat treatment time. In this study, the IMC thickness with the applied current density at various electromigration failure modes was evaluated. There was a linear relationship between the growth of the IMC layer and the applied current density at anode/substrate side. Similarly, the growth of the IMC layer with a different applied density can be expressed as the function of diffusion coefficient of the IMC layer as follows:

\[ d = d_0 + f(D)J \]  

Where \( f(D) \) is function of diffusion coefficient, and \( J \) is the applied current density.

Conclusions

The electromigration characteristic of the SnAg3.0Cu0.5 flip chip solder bump was studied through the finite element analysis and was verified by experimental analysis. Under
current stressing, a void will be formed at the entry points of the cathode/chip side of the solder bump along the electron flow path. These simulation results agreed with the experimental finding. A dimensionless parameter current crowding ratio was proposed to closely observe the electromigration-induced void propagation. The current crowding phenomenon of the line-to-bump system will be decreased in the forepart of void propagation, and the current crowding level will be increased in the latter part of void propagation. Two different electromigration-induced flip chip failure modes were proposed in this study, and they were the pancake-like and cotton-like void failure modes. The cross-sectional SEM images of the solder bump showed that the cotton-like void formation was due to the bump where there exists a crack in cathode/chip side before or during the current stressing. The cotton-like void failure mode IMC layer at the anode/substrate side was always thicker than that of the cathode/chip side of the solder bump along the electron flow path under a higher current stressing condition. This study also found the linear relationship between the growth of the IMC layer and the applied current density at the anode/substrate side.

Acknowledgments

The authors would like to thank the National Science Council for funding this research under project number NSC94-2212-E-007-029. Moreover, the authors like to express their appreciation to Abel Tan for his great help in preparing the set-up of the equipment for analyses.

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