Monolithic Travelling-Wave Mach-Zehnder Transmitter with High-Swing Stacked CMOS Driver

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Abstract: We present a 20 Gb/s monolithically integrated transmitter with stacked CMOS driver and periodic-loaded PN-junction Mach-Zehnder modulator fabricated in IBM's sub-100nm technology node. Transmitter extinction ratios of 10 dB at 20 Gb/s are demonstrated.

OCIS codes: (130.4110) Modulators; (230.2090) Electro-optical devices; (230.3120) Integrated optics devices;

1. Introduction

Monolithic integration of silicon photonic transceivers in a standard complimentary metal-oxide-semiconductor (CMOS) foundry holds promise for dramatic unit cost reduction and enabling wide deployment of single-mode optical transceivers for short-reach interconnects [1]. Recently IBM announced its sub-100 nm CMOS-Integrated Nano-Photonics (CINP) technology node where CINP components, like WDM filters, germanium photodetectors, silicon modulators, optical switches, etc., are monolithically integrated with analog and mixed-signal circuits [2]. IBM's CINP technology integrates photonic components into the CMOS front end, thereby minimizing extra processing steps, additional required mask levels, and component parasitics. In addition, monolithic integration minimizes packaging and handling steps, and thus has the potential to reduce end product cost.

Here we report on a monolithically integrated stacked CMOS driver [3] and periodically loaded Mach-Zehnder modulator (MZM) manufactured in IBM's CMS90WG technology node. The monolithic stacked-driver/MZM transmitter (TX) shows open eyes out to 20 Gb/s operation with 10 dB extinction ratio (ER).

2. CMOS and Mach-Zehnder Modulator Design

The TX block diagram is shown in Fig. 1a. The electrical input has a 50Ω on-chip termination and a CML amplifier to boost weak input signals to CML levels, followed by a CML-to-CMOS converter. Cross-coupled CMOS inverters minimize timing error between the complementary signals. The front-end accepts single-ended or differential inputs. The level shifter [4] provides Lo (V_{SS} to V_{DD}) and Hi (V_{DD} to V_{DD2}) CMOS outputs, which are buffered by inverter chains to drive the output stage [5]. The output stage, Fig. 1b, uses cascoding to limit the static voltage across any device to V_{DD} while providing V_{SS} to V_{DD2} output swing [3,4]. Electrical testing at V_{DD}=1.5V, V_{DD2}=3V gave $2V_{pp}$ into 50Ω (25Ω output impedance), or $4V_{ppd}$ push-pull to 50Ω MZM electrodes. The CMOS driver circuits were designed for high-ER optical TX targeting short-reach optical interconnect applications up to 16 Gb/s (e.g. PCI Express 4.0, Fibre Channel, infiniband), and the measurements presented below show excellent performance out to 20 Gb/s.

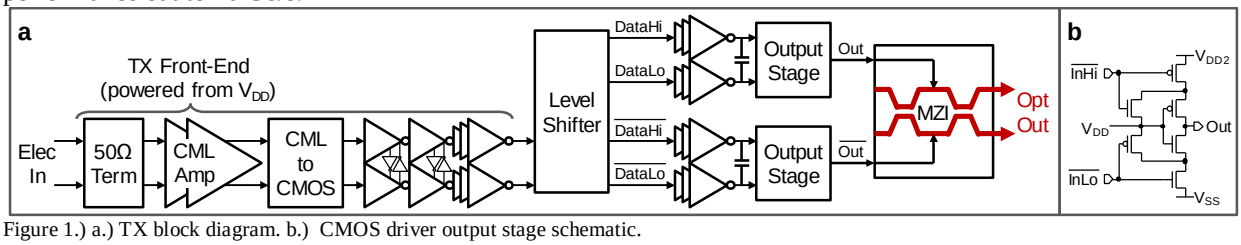

Figure 1.) a.) TX block diagram. b.) CMOS driver output stage schematic.

An image of the device is shown in Fig. 2a. The MZI has unloaded RF electrode segments to increase electrode line impedance. The unloaded RF segments are transmission line sections periodically inserted into the MZM electrode that are not connected to PN junctions. Figure 2b shows the loaded sections are the straight horizontal electrode segments highlighted by wide arrows, and the unloaded sections are the 180° turn segments denoted by the narrow white arrows. The MZM has ten 300 μm long electrode sections loaded with optical PN-junctions (3 mm total loaded electrode length) and nine 157 μm long unloaded electrode sections, for a total electrode length of 4.41

mm in each MZM arm. Since the unloaded electrode sections have low capacitance they do not contribute much to RF propagation loss. We calculate the effective line impedance from the combined loaded and unloaded sections to be ~45 Ω at 2 GHz and ~42 Ω at 18 GHz. The MZM has integrated terminating resistors that were nominally designed to have a 50 Ω termination resistance. However, due to a processing offset the fabricated devices showed a ~58 Ω resistance. The MZM also has 9 passive optical waveguide sections ~218 μm long (in proximity to the unloaded RF sections), summing to 1.967 mm of passive waveguide in each MZM arm.

The MZM is designed for ~1.3 μm light and has lateral PN junctions with ~150 nm thick SOI and 2 μm BOx. The MZM optical loss was estimated at ~6 dB, which includes losses from two thermally tunable MZM couplers at the device input and output. The MZM V_π*L product was measured to be 1.67 V-cm. Using the MZM V_π*L product, RF/optic interaction length, and output eye extinction ratio (ER) we calculate the V_{pp} drive on each MZM arm was ~1.7 V_{pp}, 15% less than standalone electrical measurements into 50 Ω.

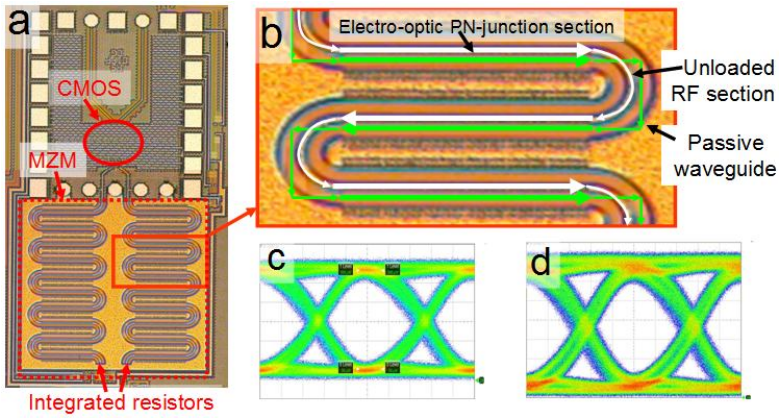

Figure 2.) a.) Image of monolithic TX with stacked CMOS drive and periodic loaded MZM. The MZM has 3 mm of electro-optic PN-junction on each arm giving a total push-pull RF/optic interaction length of 6 mm. b.) Magnified view of periodically loaded electrode in MZM, c.) 8.6 dB ER eye diagram from $3x10^{17}$ cm^{-3} p-doped PN-junction MZM. d.) 10.1 dB ER eye diagram from $7.5x10^{17}$ cm^{-3} p-doped PN-junction MZM. The TX in Fig. 2d gave 30% smaller optical modulation amplitude than that in Fig. 2c, note that the y-axis scales are different in 2c and 2d.

3. Device Response

Measurements were taken with probes that have both DC and high speed RF contacts. Figure 2c shows a 20 Gb/s eye diagram with an 8.6 dB ER from the monolithic TX in an MZM with n-doping simulated to be ~5×10^{17} cm^{-3} and p-doping ~3×10^{17} cm^{-3} in the RF/optic interaction region. Figure 2d shows a 10.1 dB ER from a modulator identical in design but with n-doping at ~5×10^{17} cm^{-3} and p-doping ~7.5×10^{17} cm^{-3} in the RF/optic interaction region. Even though a higher extinction ratio is seen in Fig. 2d, this TX gives a 30% (~1.5 dB) smaller optical modulation amplitude (OMA) than that obtained from the ~3×10^{17} cm^{-3} p-doped TX in Fig. 1b [6]. The CMOS driver consumed ~280 mW for 20 Gb/s operation, resulting in ~14 pJ/bit power consumption.

4. Conclusion

We have demonstrated a monolithic TX manufactured in the IBM CMS90WG technology node. While the transmitter driver circuit was designed for a 16 Gb/s data rate, our characterization showed open eyes up to 20 Gb/s, with a total TX power consumption of ~14 pJ/bit. Furthermore, we also note that while the CMOS TX driver was fabricated on a thick-BOX SOI substrate, the design was created using 90 nm bulk transistor models, prior to the availability of calibrated SOI CMOS models for CMS90WG technology. The resulting shift in expected transistor electrical parameters produced functional, but unoptimized driver circuits. New optical TXs designed with updated SOI transistor models are currently under fabrication, and are expected to further improve the TX performance. Discrete optical modulators designed in CMS90WG technology have been demonstrated to operate at data rates up to 25 Gb/s [7], and can be combined with appropriately designed TX circuits to produce 25 Gb/s transmitters [8].

5. References

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