Abstract

The high test power consumption, which can be several factors higher than the functional power consumption for which an integrated circuit (IC) is designed, may result in higher overall cost due to yield loss and potentially damaged ICs. As system-on-chips (SOCs) designed in modular fashion are becoming increasingly common, the testing can, in contrast to nonmodular SOCs, be performed in a modular manner. The key advantage is that modular test offers the possibility to plan the testing such that power consumption is controlled; modules are only activated when they are tested. This chapter contains an introduction to core-based testing, which is followed by a discussion on test power consumption and its modeling, and then the chapter discusses power-aware test planning for modular SOCs.