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Schottky Barrier Tunnel Field-Effect Transistor using Spacer Technique

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Abstract—In order to overcome small current drivability of a tunneling field-effect transistor (TFET), a TFET using Schottky barrier (SBTFET) is proposed. The proposed device has a metal source region unlike the conventional TFET. In addition, dopant segregation technology between the source and channel region is applied to reduce tunneling resistance. For TFET fabrication, spacer technique is adopted to enable self-aligned process because the SBTFET consists of source and drain with different types. Also the control device which has a doped source region is made to compare the electrical characteristics with those of the SBTFET. From the measured results, the SBTFET shows better on/off switching property than the control device. The observed drive current is larger than those of the previously reported TFET. Also, short-channel effects (SCEs) are investigated through the comparison of electrical characteristics between the long- and short-channel SBTFET .

Index Terms—Nickel silicide, dopant segregation, tunneling field-effect transistor, Schottky barrier, ambipolar behavior

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I. INTRODUCTION

As the complementary MOS (CMOS) devices are scaled down to 10 nm technology node, the subthrehold leakage current has been increased due to short-channel effects (SCEs). Also the subthreshold swing (SS) in MOSFET is fundamentally limited by thermionic emission of carriers (> 60 mV/dec). Thus, it is becoming more difficult to reduce power supply voltage. Recently, in order to solve the power dissipation problem, tunnel field-effect transistor (TFET) has been studied as a candidate for low operating power device [1-6]. TFET is known that the SS can be obtained below 60 mV/dec unlike MOSFET because carriers are injected by band-to-band tunneling. However, for real TFET, the SS of sub-60 mV/dec is not observed easily because of the increase of tunneling resistance by dopant diffusion by annealing, large band-gap, and trap-assisted tunneling (TAT) by defects. Also, silicon TFETs show small on-current (< 1 μm/μm) due to large tunneling resistance and ambipolar behavior caused by tunneling between the channel region and drain region. In addition, since TFET has an asymmetric source/drain doping type, it is difficult to fabricate short-channel TFET due to misalignment problem. Many research groups have concentrated on the improvement of on-current and SS properties by using high-κ material and band-gap engineering [7-9].

In this work, a TFET using Schottky barrier tunneling (SBTFET) is introduced to improve current drivability. The main difference between the SBTFET and conventional TFET is the metal source region resulting in Schottky barrier formation at the interface between the source and channel [10]. So it is expected that large on-

current is induced by smaller tunneling resistance. Also, in order to overcome the misalignment problem in short-channel TFET fabrication, the spacer technique is adopted for self-aligned doping process [11].

II. DEVICE OPERATION AND FABRICATION

The scheme of the SBTFET is described in Fig. 1(a). The source region of the SBTFET is defined using nickel silicide. In order to understand the principle of the SBTFET, the energy band diagrams are indicated as shown in Fig. 1(b). At OFF state, it is observed that the thermionic emission component injected over Schottky barrier contributes to the off-current in the SBTFET ($I_{OFF} = I_{thermionic}$). At ON state, the on-current consists of the thermionic emission and field-induced tunneling components from the source toward the channel region ($I_{ON} = I_{thermionic} + I_{tunneling}$). The Schottky barrier height (SBH) is determined by the workfunction difference between the metal source and channel region. For high current drivability, the SBH of the SBTFET needs to be lowered. However, the leakage current is supposed to increase because thermionic emission components over low SBH increase. While the SBTFET with high SBH can reduce the leakage current, tunneling components are suppressed due to widened Schottky barrier width, leading to small on-current. In this study, nickel silicide with mid-gap workfunction is used as the metal region of

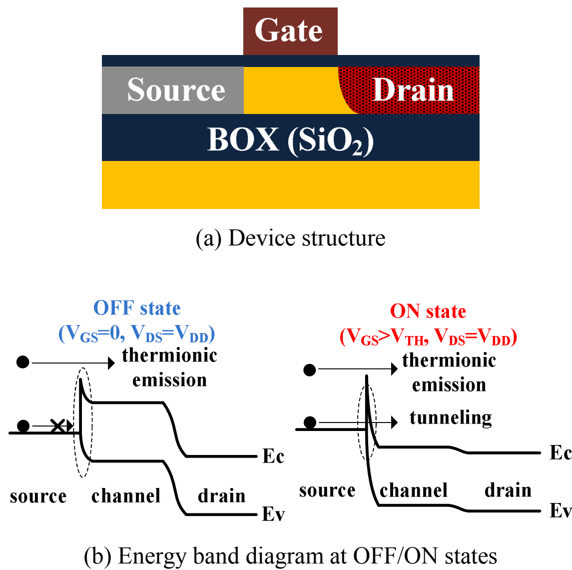


Fig. 1. (a) Device structure of the SBTFET, (b) energy band diagram when the device operates at OFF/ON states.

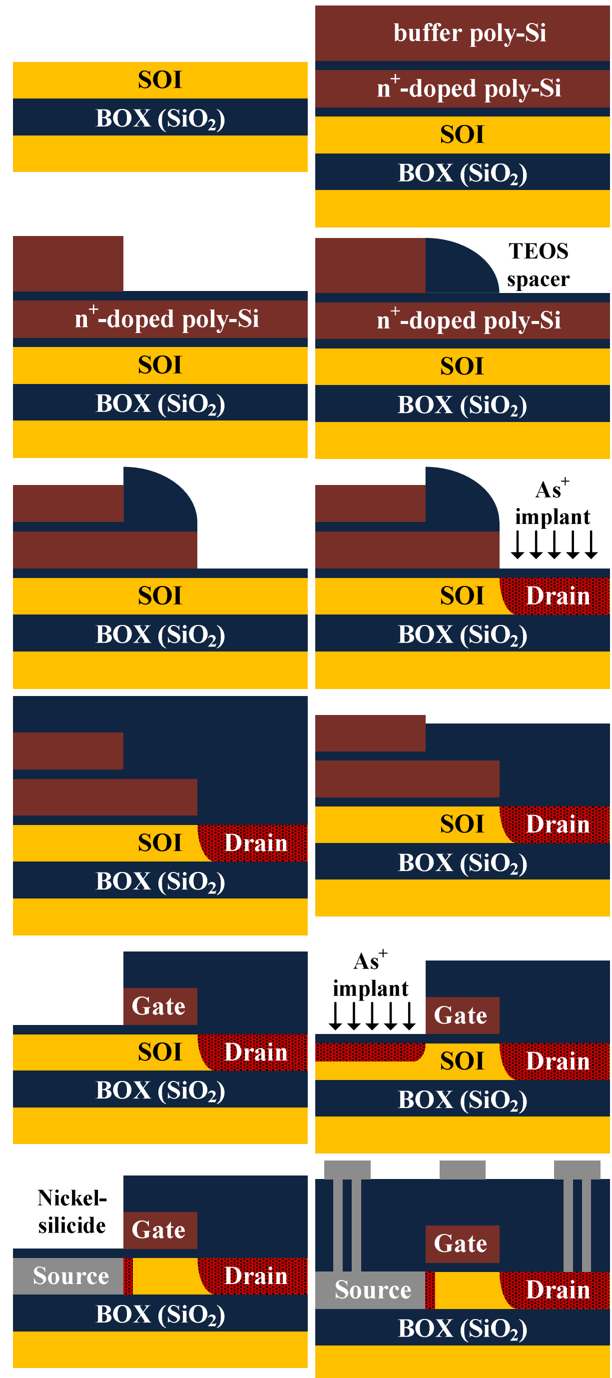


Fig. 2. Schematics of the process flow for the SBTFET using spacer technique.

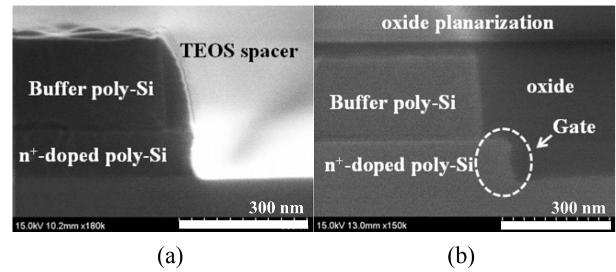
the SBTFET. Also, dopant segregation technique in the source region is applied for small tunneling resistance [12]. A schematic of the process flow for the SBTFET using spacer technique is shown in Fig. 2. After the (100) wafer preparation, SOI (Silicon On Insulator) thickness is thinned to 40 nm by oxidation process and active region is defined by photolithography process. Then, gate

oxide / gate n^+-doped poly-silicon / buffer oxide / poly-silicon (28Å / 1000Å / 300Å / 3000Å) are sequentially formed and the poly-silicon layer is anisotropically etched using a photoresist (PR) mask. In order to define the gate region, tetraethyl orthosilicate (TEOS) is isotropically deposited using PECVD and is etched using RIE. The TEOS spacer length is determined as the gate length. By using the TEOS spacer mask, the drain region can be defined (As^+, 2×10^{14} cm^{-2}, 10 keV). Next, HDPCVD oxide is deposited to protect the drain region and oxide CMP process is performed. Once the HDPCVD oxide on top of the poly-silicon is completely removed, poly-silicon / buffer oxide / gate n^+ poly-silicon are etched by using the remaining HDPCV oxide as a hard mask. Then, arsenic doping is performed for dopant segregation (As^+, 1×10^{14} cm^{-2}, 5 keV) and annealing process is conducted (950℃, 5 sec). For metal source region, after 15 nm nitride spacer formation, nickel is deposited (200Å) and RTP process is conducted (450℃, 60 sec). Residual nickel is stripped by SPM cleaning (H_2SO_4:H_2O_2 = 4:1, 120℃, 60 sec), and conventional back-end processes are performed.

The control devices using the same process method are fabricated to compare the electrical characteristics of the SBTFET and conventional TFET. The source region of the control device is formed by implantation process (BF_2^+, 6×10^{14} cm^{-2}, 10 keV). Furthermore, the SBTFET and control devices with a long channel by using gate photolithography process are fabricated to investigate SCEs. Fig. 3(a) shows the SEM image of the TEOS spacer for gate length definition. Also CMP process is successfully done for the formation of the metal source region as shown in Fig. 3(b). Fig. 4 shows the nickel silicide source and nitride spacer image after the source region formation. Through this process flow, the SBTFET and control device with a gate length of 100 nm can be successfully implemented. Also, the long-channel devices with a gate length of 0.5 μm is fabricated using photolithography.

III. Results and Discussion

The electrical characteristics of fabricated devices are analyzed using Agilent 4156C. First, the transfer characteristics of the SBTFET and control device with long channel (L_G = 0.5 μm) are investigated as shown in Fig. 5. For off-current properties, the control group has small leakage current by band-to-band tunneling. Also the SBTFET's leakage current level by thermionic components is similar to the control group. For on-current properties, in case of the SBTFET, it is found that the on/off current ratio and SS property are better than that of the control device due to small tunneling



(a) (b)

Fig. 3. SEM images of (a) the TEOS spacer, (b) oxide planarization after CMP process.

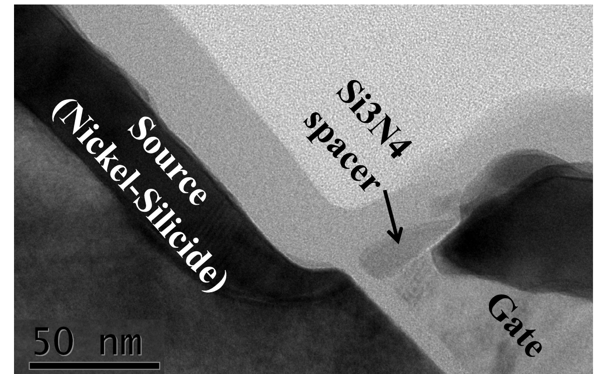


Fig. 4. TEM image of the source region after nitride spacer and nickel silicide process.

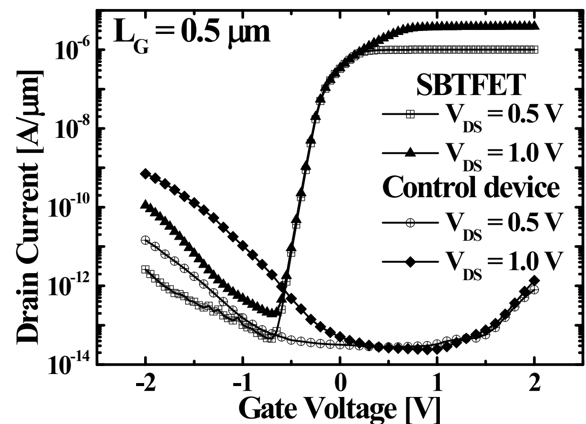


Fig. 5. The transfer characteristics of the SBTFET and the control device with gate length of 0.5 um.

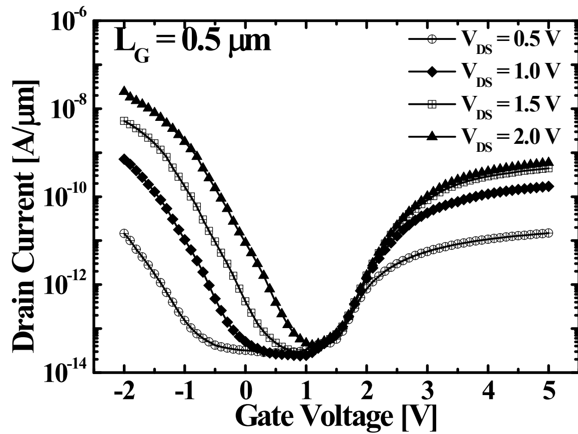
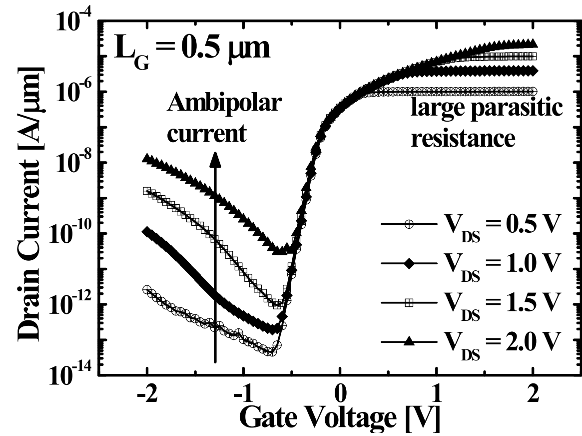


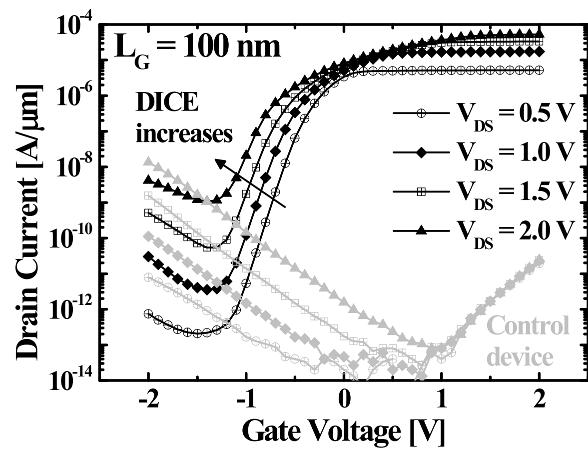
Fig. 6. Transfer characteristics of the control device with increasing drain voltage.

resistance. The extracted SS value is 68.1 mV/dec at drain voltage of 0.5 V and SS degradation is not observed with increasing drain voltage. However, drain current tends to saturate with increasing gate voltage. It is because the fabricated SBTFET has large parasitic resistance. In case of the control device, desirable switching can't be observed. Drive current is much smaller than ambipolar current and extremely high SS value is obtained. In order to investigate the reason of poor switching, the transfer characteristics of the control device are plotted for a wide range of gate voltage as shown in Fig. 6. For low forward voltage, switching operation hardly occurs. High gate voltage above 2 V is needed to operate the control device. For the reverse gate voltage range, ambipolar current significantly goes up with increasing drain voltage and is larger than the drive current. This result is caused by dopant diffusion difference. Boron dopants in the source region are easily diffused compared with heavy arsenic dopants in the drain region during thermal annealing process for dopant activation. As a result, tunneling resistance between the source and channel becomes larger resulting in poor SS and on-current properties.

Next, in order to investigate SCEs of the SBTFET, the transfer characteristics are plotted. In case of the SBTFET with a long-channel, SCEs are not seen and good current drivability as shown in Fig. 7(a). However, ambipolar current increases significantly as the drain bias increases, which is caused by tunneling current between the channel and the drain as the control device. In case of the short-channel SBTFET (L_G = 100 nm), the electrical characteristics are degraded compared with that of the



(a) L_G = 0.5 um



(b) L_G = 100 nm

Fig. 7. Transfer characteristics of the SBTFET with long- and short-channel.

long-channel SBTFET. Thus, the high SS value of 116 mV/dec is extracted. Especially, drain induced current enhancement (DICE) gets worse as the drain voltage is increased. It is because Schottky barrier width is modulated by the drain voltage regardless of the gate voltage. Thus, in order to reduce the SCEs and ambipolar behavior, additional techniques are needed such as underlapped drain region and long effective channel length [13]. However, although the short-channel SBTFET has SS degradation and DICE, the good switching behavior is still observed compared with the control device due to small tunneling resistance. The output characteristics of the SBTFET with L_G of 100 nm are also investigated as shown in Fig. 8. While the drive current is larger than that of the previously reported TFETs, the current drivability for the low drain voltage is weak due to tunneling resistance.

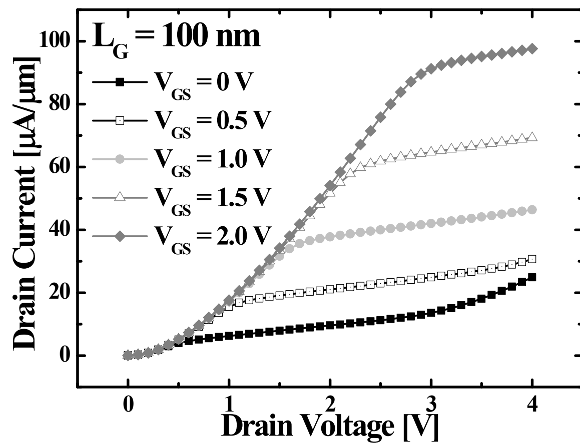


Fig. 8. Output characteristics of the SBTFET with gate length of 100 nm.

IV. CONCLUSION

In this study, the SBTFET is proposed to overcome the disadvantages of TFET. Also the proposed device with self-aligned source/drain region is firstly fabricated by using spacer technique. From the measured results, on/off switching property of the proposed device are improved compared with that of the control device. However, in terms of parasitic resistance, ambipolar current and SCEs, the improvement of the electrical characteristics is needed through additional process optimization.

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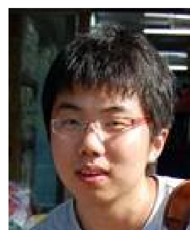

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