Prospects and Limitations of Organic Thin Film Transistors (OTFTs)

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Abstract. Organic Transistor (OT) modeling, fabrication and applicability has undergone remarkable progress during last ten years. Organic Thin Film Transistors (OTFTs) have received significant attention recently because of their considerable utility. They can be fabricated at lower temperature and significantly reduced cost as compared to Hydrogenated Amorphous Silicon Thin Film Transistors (a-Si: H TFTs). Fabrication of OTFTs at low temperature allows utilization of wide range of substrates, thereby permitting usage of organic transistors as future candidate for many low-cost electronics applications that require flexible polymeric substrates such as RFID tags, smart cards, electronic paper, and active matrix flat panel displays. This paper provides detailed insight of OTFTs, their operating principles, device materials and various structures such as Top Gate Top Contact (TGTC), Top Gate Bottom Contact (TGBC), Bottom Gate Top Contact (BGTC) and Bottom Gate Bottom Contact (BGBC). Although OTFTs find tremendous and widespread applications, but is marred by few limitations related to factors such as speed, compatibility, stability, degradability and variability. This paper comprehensively discusses the performance and limitations of OTFTs.

Keywords: Operating principle, Organic thin film transistor, Organic transistors and Pentacene.

1 Introduction

During the last few years, research in OTFTs is being actively pursued because of their potential for low cost fabrication of large area circuits. OTFTs possible applications range from Active-matrix displays, E-paper, E-book, Signage, Advertisement, Storage devices, Electronic display cards (Smart cards, Gate pass, and Game cards), Touch screen mobile phones, Automobile, Wearable cloths, RFID tags, Price/Inventory tags, Flexible integrated circuits to Sensors and other novel products [1-7]. Due to their unique material properties, organic semiconductors have several

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advantages over their inorganic counterparts. The most important advantage is in the processing techniques, where organic devices can be fabricated on large area [2], at much lower temperature and at considerably lower cost thereby allowing the use of flexible substrates [6, 7]. Therefore, researchers have actively considered fabricating OTFTs and other organic devices on a variety of unconventional substrates like glass, plastic [4], paper [5] and fibers. Furthermore, organic materials supports novel and unconventional fabrication techniques, such as spin coating process, nano imprinting techniques which enables rigorous downscaling of the devices to nano level size in a more cost effective way than for inorganic devices [7, 10, 12].

Performance of OTFTs can be expressed in terms of conventional parameters such as on-off current ratio (I_{ON}/I_{OFF}), field effect mobility (μ), threshold voltage (V_T) and transconductance (g_m). The performance of the best OTFTs now rivals that of commercial a-Si- H TFTs, which are commonly employed as the pixel switching elements in active matrix flat panel displays [8, 9]. A number of industrial laboratories are working hard to develop low-cost, large-area plastic electronics materials making use of TFTs and diodes based on organic semiconductors [9]. Inspite of impressive progress in their performance, a relevant physical description or model is still not available that can adequately predict or interpret observed phenomena of OTFTs [9, 10]. However, there are still many issues remaining with OTFTs that are to be resolved for their successful and reliable future use. Although, OTFT technology is on the verge of commercialization, but still faces a number of challenges that require fundamental understanding at the fabrication, materials chemistry and device physics to make significant progress [11-13].

This paper contains five sections. The present section 1 introduces the contents of the paper. Section 2 describes various top and bottom gate structures, material and fabrication of OTFTs. Compact model and operating principle are explained in section 3. Performance parameters of various structures are analyzed and discussed in section 4. Finally, section 5 discusses some of the limitations of OTFTs that needs to be overcome in future.

2 OTFT Structure, Material and Fabrication

An OTFT is a transistor made up of thin film current carrying organic semiconductor (OSC), an insulator layer and three electrodes. Two of the electrodes, source (S) and drain (D) are in direct contact with organic semiconductor and the third, gate (G) electrode is isolated from semiconductor by dielectric insulator. The structure of device is stated not only by its operating mode but also by issues and limitations arising from its fabrication process [7]. Firstly, the main difference between the geometry of conventional MOSFETs and OTFTs is that latter does not have a fourth terminal that is body, thus making these transistors free of body effect. Secondly, in MOSFETs the conducting channel is formed by an inversion layer while in OTFTs, it is because of accumulation layer [22]. Classification of different OTFTs structure based on top or bottom gate is shown in Fig.1.

The development of different structures had motivation to improve electrostatic control of gate (G) over organic conducting channel (such as pentacene) as well as to reduce contact resistances at source and drain regions [8]. Based upon the relative

position of S, D and G contacts with respect to OSC layer different structures can be made for OTFTs [12]. Certain merits and demerits are associated with each of the OTFT structures.

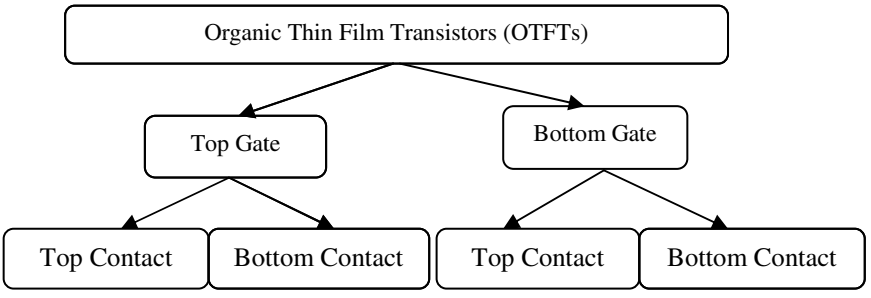


Fig. 1. Various structures of Organic Thin Film Transistors (OTFTs)

2.1 Top Gate Structures

The structure of top gate OTFT is like conventional MOSFET, where gate is placed on the top of organic semiconductor layer [7, 8]. Further it has two different configurations, i.e. top contact and bottom contact structures. These structures are based on relative position of contacts (S and D) with respect to semiconductor layer. In top contact structure, the contacts are deposited above OSC layer through shadow mask, where as in bottom contact structure, the contacts are placed below OSC layer using microlithography technique. Based on the placement of contacts, the two configurations of top gate structures are named as Top Gate Top Contact (TGTC) and Top Gate Bottom Contact (TGBC). As shown in Fig. 2 (a) for TGTC structure, gate is defined on the top of organic semiconductor layer and source and drain contacts are patterned between gate dielectric and organic semiconductor film. However, in TGBC structure source and drain contacts are patterned on a substrate rather than on an insulator layer or organic semiconductor layer as shown in Fig. 2 (b).The performance of top gate structure may get severely degraded when the underlying active organic semiconductor layer is affected during deposition of gate [12]. Thus top gate structures require precise and accurate fabrication procedure.

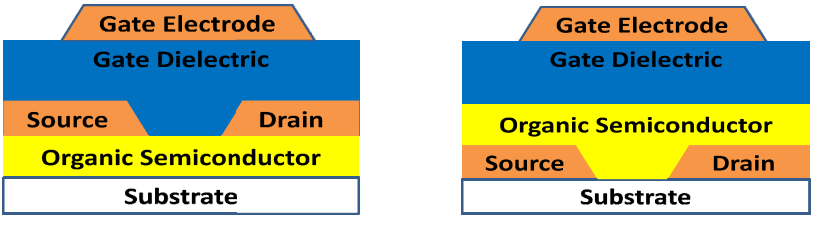
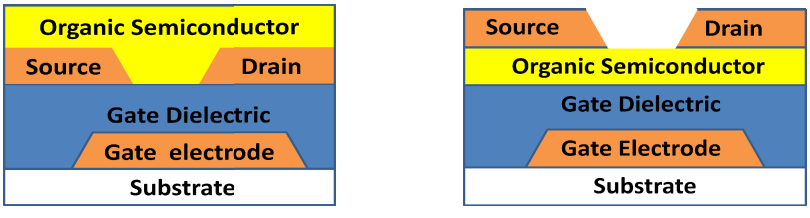


Fig. 2. Top gate OTFTs structures (a) Top Gate Top Contact (TGTC) structure (b) Top Gate Bottom Contact (TGBC) structure

2.2 Top Gate Structures

Bottom gate structures are built in majority for existing OTFTs since deposition of organic semiconductor on insulator is much easier than the reverse due to fragile nature of organic semiconductors. Furthermore, bottom gate structure can be categorized to two different configurations *viz.* Bottom Gate Bottom Contact (BGBC) and Bottom Gate Top Contact (BGTC).As shown in Fig. 3 (a) for BGBC structure, the gate is at the bottom, above which the insulator (dielectric) layer is deposited. S and D contacts are formed above the dielectric layer and finally organic semiconductor layer is deposited on the top of the structure [7]. BGBC structure is advantageous because the methods involving solvents and/or thermal treatments can be safely employed to prepare the gate dielectric and contacts without harming the semiconductor layer [8]. Moreover, bottom contact structures have an advantage of utilizing standard lithographic techniques straightforwardly for obtaining short channel length devices [12]. However, these devices usually suffer from higher contact resistances because of smaller effective area for charge carrier injection [22].



(a) (b)

Fig. 3. Bottom gate OTFTs structures (a) Bottom Gate Bottom Contact (BGBC) structure (a) Bottom Gate Top Contact (BGTC) structure

In BGTC structure, contacts on top are deposited through shadow mask where as for bottom gate formation microlithography technique is used [7]. The top contact OTFT fabricated using shadow mask technique results in relatively large channel length devices [10]. However, for same semiconductor and dielectric materials, the contact resistance and mobility are better in top contact devices. The better field effect mobility for BGTC OTFT is due to less contact resistance than that of BGBC [12]. OTFTs mobility in BGBC device structure is generally observed to be lower by two orders of magnitude than to BGTC device. The reasons for this difference is often explained by the large metal-semiconductor contact resistance due to interface contact barrier and irregular deposition or poor morphology of semiconductor film around the already patterned S and D contacts [8]. Organic semiconductor films grown on metal often have inferior properties as compared to those grown on a dielectric [11]. In BGTC, lower contact resistance and larger injection area enables higher currents for the same applied voltages in comparison to BGBC structure [21].

2.3 Organic Thin Film Transistor Materials

The important factors for high performance OTFTs are dielectric/semiconductor interface, metal/semiconductor interface, ordered molecular structure of active layer, efficient injection at contacts and stability. A wide variety of materials for all the layers of OTFT are explored in various combinations to optimize their performance. Organic materials offer strong assurance in terms of properties, processing and cost effectiveness.

2.3.1 Organic Semiconductor Thin Film

Organic semiconductor materials are divided in two groups such as polymers and small molecules. The mobility of polymers is lower than small molecules because of higher molecular weight [10]. To obtain higher mobility in OTFTs, active semiconductor layer should have large grain size. There are various polymers and small molecule semiconductor materials that can be used as active OSC material such as pentacene, poly (3-hexylthiophene) (P3HT) [14], poly (3-alkylthiophene) (P3AT) and poly (3-octylthiophene) (P3OT) [15]. Pentacene is the most extensively used small molecule material, because of its highest mobility among all organic semiconductor materials. Pentacene on SiO_2 has yielded higher carrier mobility. Pentacene has other advantages such as good chemical stability in adverse environmental conditions, very high mobility in thin film form and stable interface with commonly used electrode metals such as Al and Au [8, 22].

2.3.2 Electrodes

Electrodes can be fabricated using either inorganic or organic materials. The contact metal for S and D should have low interface barrier with active semiconductor layer so that large number of carriers can be injected. Moreover, these contacts should have small contact resistance [18, 19]. Prominent inorganic contact materials include aluminum (Al), gold (Au), titanium (Ti), copper (Cu), calcium (Ca), nickel (Ni), platinum (Pt), magnesium (Mg) and chromium (Cr) [8, 22]. New classes of organic materials known as conducting polymers are also available for S/D contacts. Poly-3, 4-ethylenedioxythiophene : styrene sulfonic acid (PEDOT: PSS), polyaniline doped with camphorsulphonic acid (PANI-CSA) [14] deposited by spin coating are commonly used conducting polymers for S/D electrodes. Among all inorganic contact materials, Au is the most commonly used contact metal because of its higher work function *i.e.* 5.1 eV, which enhances the injection of holes into active semiconductor layer. The material for gate electrode should have several characteristics, like good patterning capabilities, and good adhesion with substrate and gate dielectric. The gate metal work function should be comparable to active semiconductor layer to attain low threshold voltage. Such materials include heavily doped silicon, Al, Au, indium tin oxide (ITO) [12, 22].

2.3.3 Gate Dielectric

Nowadays, researchers are working to enhance the properties of dielectric materials, since, they are extremely crucial to achieve reliable and high-performance OTFTs.

Apart from compatibility with organic semiconductors, the dielectric materials should exhibit high insulation. High resistivity reduces the interface trap density between OSC and gate dielectric, which, in turn, prevents leakage between gate metal and OSC [14]. Further, the dielectric material should have high dielectric constant to ensure enough capacitance for channel current flow. This lowers the required drive voltage for a given channel current [12, 17]. Moreover, the thickness of gate dielectric layer is kept low to not only operate at low voltages, but also to reduce short channel effects in submicron devices. Besides this, the dielectric materials should have ability to form thin, pinhole-free films with high breakdown voltages and long-term stability [7-10]. These requirements are met by various dielectric materials such as SiO_2, Al_2O_3, polyvinyl phenol (PVP), propylene, poly (4-vinylphenol) (P4VP), poly-methyl methacrylate (PMMA) [16], barium zirconate titanate (BZT) and polyvinylidene fluoride (PVDF).

2.3.4 Substrate

Most OTFTs have been fabricated on heavily doped silicon substrate due to availability of good dielectric in the form of SiO_2 [16, 17]. Si is often used in electronics not only because of the intrinsic properties but also because of nearly ideal interface it forms with its thermally grown oxide [25]. Novel substrate materials on which working OTFTs have been fabricated include polyethylene naphthalate (PEN), poly-ethylenetherephthalate (PET), polyimide, and polyethylene, glass, plastic, paper and fibers [4-6]. These organic substrate materials have shown their remarkable performance in term of flexibility which motivates researchers for its utilization in design of flexible electronic devices and circuits.

2.4 OTFTs Fabrication

Performance of an OTFT strongly depends on the way it is fabricated. There are various fabrication approaches for OTFTs using different materials for substrates, electrodes, active semiconducting layers and gate insulators [8]. The devices are prepared either on top of highly n-doped silicon (Si) substrate or on a plastic foil. This section emphasizes on fabrication of bottom gate OTFTs with top and bottom contacts. Top and bottom contact are generally fabricated on a highly doped n-Si wafer, which acts as substrate as well as gate electrode [12]. A thermally grown SiO_2 on the Si substrate acts as gate insulator for both top and bottom contact devices. First step is thermal oxidation of Si that exposes wafer to an oxidizing environment of oxygen at an elevated temperature in quartz tube to grow SiO_2. Thereafter, substrates are cleaned by RCA (Radio Co-operation of America) method, followed by photolithography and lift-off process to pattern S and D electrodes [12]. Subsequently, pentacene is deposited as active semiconductor layer using spin coating technique. Finally, source, drain and gate contacts are made from gold. Major OTFT's fabrication process steps are depicted in Fig. 4. After fabrication of complete OTFT device, various characterization methods are applied to extract its electrical properties and parameters [18, 22].

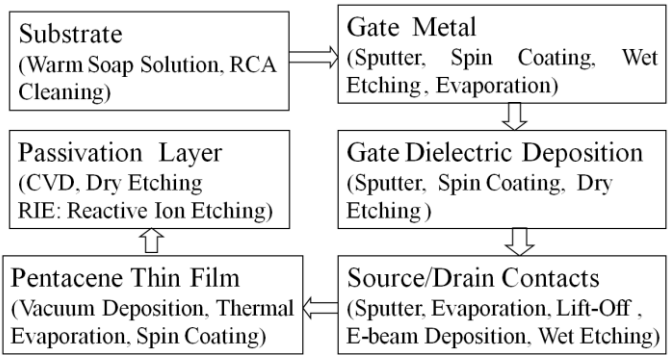


Fig. 4. Major steps used in fabrication of organic thin film transistors

3 OTFT Models and Operating Principle

Analytical models are often incorporated in simulations to forecast and optimize performance of organic integrated circuits. These models should be essentially upgradable, reducible, easily implementable and modifiable [13]. The model should also simultaneously allow for separation of characterization techniques. Researchers have recently proposed some analytical models which are discussed in following subsection along with their operating principle.

3.1 OTFTs Compact DC Models

The electrical characteristics of OTFTs are mostly similar to those of a-Si: H TFTs [24]. Some of the existing models of a-Si: H TFTs have been modified in order to represent the characteristics of OTFTs [6]. These OTFT models are referred to as dc compact models and behave similar to crystalline field-effect transistors (c-FETs) and a-Si: H TFTs [13]. Several models and features have been proposed to reflect one or the other specific charge transport mechanism in OTFTs. However, dc modeling involves the challenge of taking into account the variations in measurement results [13]. The electrical current-voltage characteristics of OTFTs are often incorrectly modeled similar to MOSFETs until the first dc compact model of OTFT was proposed by Xie *et al.* in 1992 [23]. This compact model for OTFT included both contact and leakage resistances. A generic analytical dc model, proposed by Marinov *et al.* [13], claims to be fully symmetrical, and valid for all regimes of TFT operation, *i.e.*, linear and saturation above threshold, subthreshold, and reverse biasing.

Although researchers have made serious efforts to describe the physical characteristics and properties of OTFTs by introducing analytical compact models [13, 15], but due to incomplete information about nature of carrier transport mechanism in organic semiconductors, these rare models are still far from representing OTFT compact dc model in usual circuit analysis. Furthermore, these

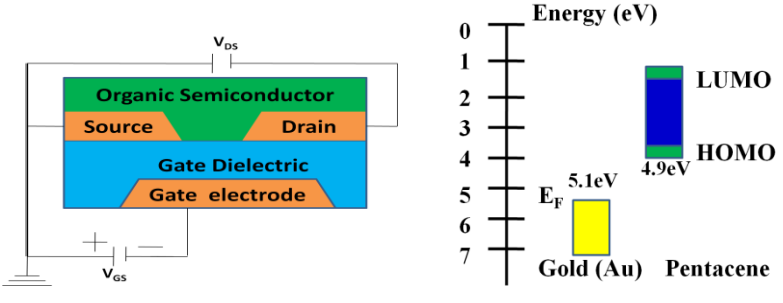
models are not fully suitable due to their incompleteness and/or their complexity, which leads to convergence issues and long computation time.

3.2 Operating Principle

The operating principle of OTFT in this paper is explained using the schematic diagram of BGBC structure, as shown in Fig. 5 (a). The device consists of pentacene organic semiconductor material with source/drain and gate electrodes made of Au and Al, respectively. The Fermi level of gold and the HOMO: LUMO (Highest Occupied Molecular Orbital: Lowest Unoccupied Molecular Orbital) levels of pentacene are shown in Fig. 5 (b).

Fundamentally, an OTFT operates like a capacitor. When voltage is applied between gate and source (V_{GS}), charge carriers get accumulated at insulator-OSC interface. For instance, when positive voltage is applied to the gate, negative charges are induced at the interface. However, the electron injection is poor in this scenario because the Fermi level of gold is far away from the LUMO level. Accordingly, no current passes through the channel. However, a small current exists, essentially, due to leakages through the insulating layer.

On the other hand, when negative gate voltage is applied, holes get injected from source to semiconductor. This charge forms conducting channel, since Fermi level of gold is now closer to HOMO level of pentacene, as depicted in Fig. 5 (b). Threshold voltage V_T describes activation potential for channel formation. On applying drain-source voltage (V_{DS}), current I_{DS} flow from source to drain.



(a) (b)

Fig. 5. (a) Schematic of BGBC structure operation, pentacene as active semiconductor layer, with S/D gold contact electrodes. (b) Energy band level of gold and pentacene interface.

Apart from voltages, critical device dimensional parameters that affect current flow include channel length L, width W, thickness of dielectric t_{ox} and organic semiconductor film thickness t_{osc}. Due to majority of holes in the conducting channel, pentacene is said to be a *p*-type semiconductor. Similarly, an organic semiconductor will be considered

n-type when S and D electrodes can inject electrons in its LUMO level. However, it is necessary to point out that this concept differs from that of doping in conventional semiconductors, which can be made either *n*-type or *p*-type.

4 Performance Analysis of OTFT

In general, OTFT performance is analyzed through its output and transfer characteristics. These characteristics are used to extract various performance parameters such as field effect mobility, on/off current ratio, threshold voltage, subthreshold slope and transconductance.

4.1 Characteristics of Different OTFT Structures

This section analyzes the functioning of various OTFT structures. For carrying out the analysis the parameter values for channel length (L), channel width (W), aluminum oxide (Al_2O_3) insulator thickness (t_{ox}), source/drain length (t_S/t_D), and pentacene active layer thickness (t_P) are taken as 10µm, 100µm, 5.7nm, 20nm and 30nm, respectively [7]. The gate electrode is considered to be made of aluminum with 20nm thickness. The properties of pentacene organic semiconductor material used in simulation include 2.2eV energy gap, 2.8eV electron affinity, electron density of state of 2.0 x 10^{21} per cm^3 in valance band, 1.7 x 10^{21} per cm^3 in conduction band and permittivity of 4.0 [12]. Top and bottom gate analyses have been performed for bottom and top contact OTFT structures using Silvaco ATLAS two-dimensional numerical device simulator setup. Out of these four structures, two structures are referred as top gate and the other two as bottom gate, as shown in Fig. 2 and Fig. 3, respectively. The mobility in OTFT structure is described using Poole-Frenkel model given by

$$\mu(E) = \mu_0 \, exp\left[-\frac{\Delta}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right] \tag{1}$$

where $\mu(E)$ is the field dependent mobility, μ_0 is the zero field mobility, E is the electric field, is the zero field activation energy, β is the electron Pool-Frenkel factor, γ is the fitting parameter, k is the Boltzmann constant and T is the temperature. Poole-Frenkel conduction is due to field enhanced thermal excitation of trapped charge carriers. The drain current reduces in the low field region, due to charge carriers being localized around the traps. This implies that the device drain current can be appreciably enhanced through release of these trapped charge carriers. Increase in the electric field is one of the ways to ensure such desirable phenomenon.

Various OTFT structures are simulated using organic TFT display module. The transistor sizes for all the proposed structures are kept same, for valid comparison among them. Simulation uses proper boundary condition and device physics to analyze the OTFT structures. The resulting output and transfer characteristic plots for TGTC, TGBC, BGBC and BGTC OTFTs structures are shown in Fig. 6 to Fig. 9, respectively.

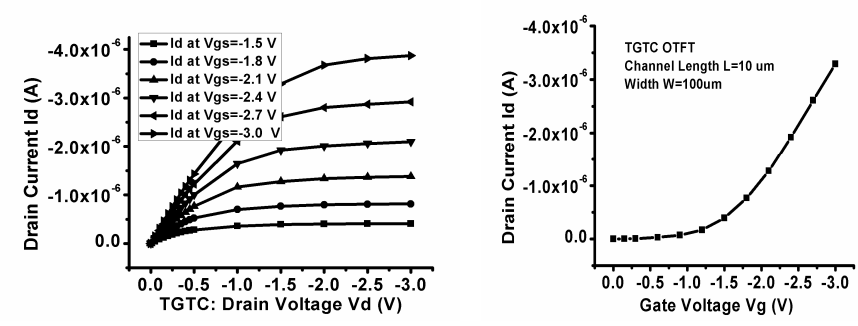


Fig. 6. Output and Transfer (at V_{ds} = - 1.5 V) characteristics of TGTC OTFT

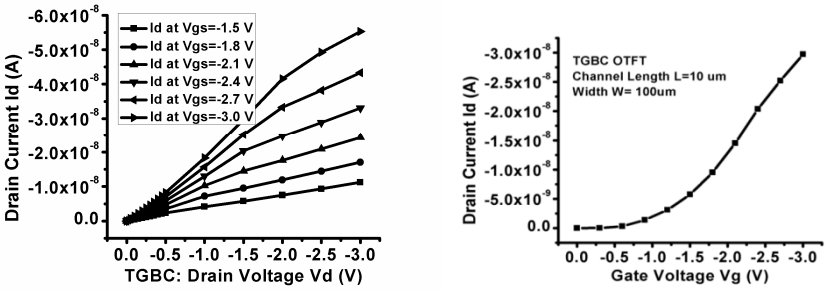


Fig. 7. Output and Transfer (at V_{ds} = -1.5 V) characteristics of TGBC OTFT

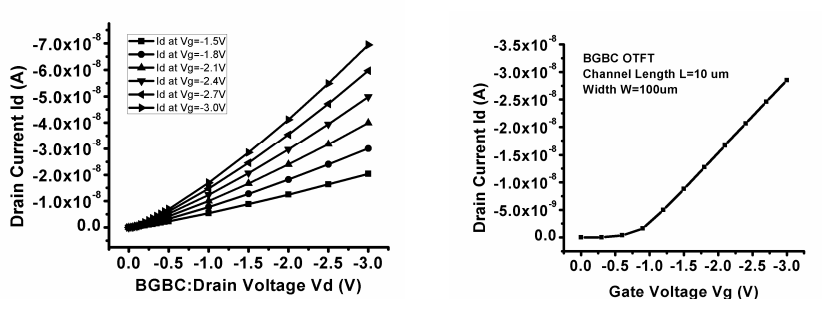


Fig. 8. Output and Transfer (at V_{ds} = - 1.5 V) characteristics of BGBC OTFT

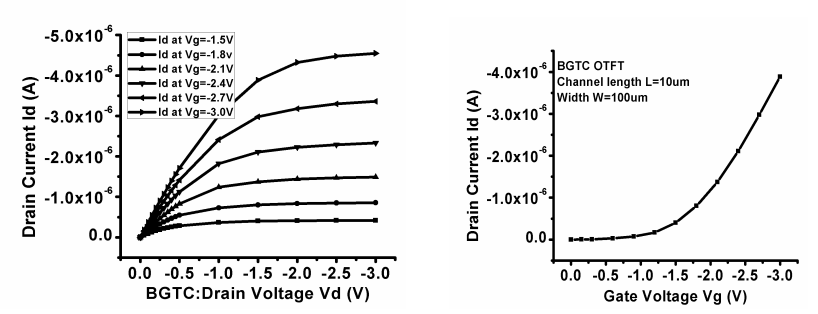


Fig. 9. Output and Transfer (at V_{ds} = -1.5 V) characteristics of BGTC OTFT

4.2 Performance Parameters

The performance parameters such as drive current, mobility, threshold voltage, subthreshold slope, transconductance, on/off current ratio are extracted from characteristic plots of different OTFT structures. The resulting parameter values are presented in Table 1.

Table 1. Extracted parameters for various OTFT structures

Parameters	TGBC	TGTC	BGTC	BGBC
Mobility (μ) cm^2/V.s	0.0016	0.2081	0.2512	0.0029
Threshold Voltage (V_T) V	-0.86	-0.97	-1.06	-0.63
On/Off Current Ratio (I_{ON}/I_{OFF})	10^6	10^5	10^5	10^6
Subthreshold Slope (SS) V/decade	0.163	0.119	0.130	0.147
Transconductance (g_m) S/m	0.019	2.30	3.00	0.013
Drive Current (I_{DSmax}) µA at $V_{GS} = V_{DS}$ = -3V	-0.055	-2.32	-4.60	-0.069

It is observed that OTFT structures with top contact demonstrate superior performance as compared to those with bottom contact. These improvements in performance are achieved in terms of mobility, transconductance and maximum drain current. Higher injection area and reduced drain and source contact resistances are main reasons for better behavior of top contact based OTFT architectures. Among all OTFT structures, BGTC structure exhibit best operating functionality in terms of all the afore-mentioned parameters.

4.2.1 Mobility

Mobility of organic semiconductor layer is receiving significant attention in order to improve transistor characteristics. In fact, reliable operation of transistor requires larger mobility [8, 22]. Earlier, OTFTs exhibited poor performance due to their low field effect mobility. This motivated most of the research efforts to improve mobility through changing processing conditions. Consequently, mobility of *p*-type OTFTs has

already exceeded 1cm^2/V.s for pentacene and 0.1cm^2/V.s for poly-3-hexythiophene (P3HT) [15]. Pentacene is the most widely used OSC for organic transistors due to its higher hole mobility. However, its electron mobility is substantially lower as compared to hole mobility. As a result, a significant effort is being devoted to improve its electron mobility [22], so as to realize complementary OTFT logic circuits using pentacene as active material.

The analysis in section 4.1 shows that a larger mobility is obtained for top contact rather than the bottom one. The results, tabulated in Table 1, indicate that TGBC and TGTC have much lower mobility than BGBC and BGTC structures, respectively. Moreover, simulation results indicate that device structure by itself is not the only factor that affects mobility devices. Other factors, which may be responsible for their performance, depend on the device fabrication process and material properties.

4.2.2 Threshold Voltage (V_T)

Threshold voltage is the minimum gate voltage at which an OTFT begins to conduct. In other words, it is the minimum gate voltage at which accumulation of holes takes place at the OTFT insulator-semiconductor interface. As indicated in table 1, threshold voltage (V_T) of TGBC, TGTC, BGTC and BGBC are -0.86V, -0.97V, -1.06V, and -0.63V, respectively, at gate and drain voltages of -3V each. Hence, the analysis reveals that bottom contacts show lower threshold voltages as compared to top contacts. Threshold voltage depends on dielectric capacitance and, hence, thickness of insulator layer. Dielectric thickness is smaller for bottom contact in comparison to top contact for constant dimensions of each layer of OTFT. This leads to lower threshold voltages for bottom contact structures.

4.2.3 On/Off Current Ratio (I_{ON}/I_{OFF})

I_{ON}/I_{OFF} is ratio of the current in the accumulation mode to the current in the depletion mode. I_{ON} is drain current above threshold voltage at which saturation takes place and I_{OFF} is the drain current below threshold voltage. The on/off current ratio of OTFTs are higher for thinner semiconducting layer. I_{ON}/I_{OFF} should be more than 10^6 for memory and display devices [8]. Short channel devices have higher on/off current ratio than long channel devices [22]. On/Off current ratio is evaluated from transfer characteristics of various OTFT structures.

The extracted on/off current ratios for TGBC, TGTC, BGTC and BGBC structures are 10^6, 10^5, 10^5 and 10^6, respectively. This shows that bottom contact devices exhibit higher on/off current ratio. The primary reason behind this is that the device exhibits negligible current at zero drive voltage. This also means that leakage current is extremely small for bottom contact devices thus making them suitable for memory and display applications.

4.2.4 Sub-threshold Slope (SS)

Sub-threshold slope is ratio of change in gate voltage to the change in drain current on log scale at constant drain voltage. Steeper curve correlates to better switching behavior of device.

$$SS = \frac{\partial V_G}{\partial log_{10}(I_{DS})} \tag{2}$$

Sub-threshold slope is evaluated using equation (2) from $log_{10}(I_{DS})$ versus V_{GS} curve. It is an important parameter that allows efficient usage of transistor as a switch. Sub threshold slope is a measure of switching behavior of OTFT. Table 1 indicates that for given dimensions the channel formation between source and drain contacts depends on the biasing voltages and, hence, switching behavior of a device. The simulated results of subthreshold slopes for TGBC, TGTC, BGTC and BGBC structures are 0.163, 0.119, 0.130, and 0.147V/decade, respectively. Therefore, bottom contact OTFTs demonstrates higher sub-threshold slopes as compared to top contacts with same gate structures. This can be attributed to different carrier injection density from the source electrode into the OSC thin film.

5 Limitations

Almost all electronic devices used in daily life are based on inorganic semiconductors, like, silicon, gallium arsenide, gallium nitride, indium phosphate, silicon-germanium, *etc*. Inorganic semiconductor based devices are dominant in electronic market because of their high operating speed, environmentally stable and everlasting performance. For instance, silicon based integrated circuits have been integral part of satellite communication systems for over last 40 years.

On the other hand, significant progress in organic semiconductors technology has provided designers with an alternative to inorganic materials. However, still numbers of challenges have to be met out in order to make organic material based devices, practically viable. Currently, organic devices show various constraints at fabrication, material and device physics level. Firstly, the organic semiconductor based devices possess complex structure. Besides this, they degrade with time and can deform easily. It is well-known that the characteristics of organic materials change with environmental conditions after long duration. Therefore, stability of these devices has to be worked out and modeled properly to better comprehend the process of degradation. Researchers agree that most of the instability comes from the chemical structure of the compound and, hence, are trying to find ways to synthesize more stable organic compounds.

Furthermore, OTFT current-voltage characteristics degrade at higher temperatures. In addition, the noise level increases considerably at low frequencies. Academia and industry throughout globe intend to develop organic semiconductor with high mobility and fast switching time. Rapid development of organic electronics with improvements in compatibility of organic transistors and micro-fluidics opens wide horizons for use of OTFTs in compact sensing systems or biochips. However, several issues are still open, particularly, those related to long-term stability and batch-to-batch, roll-to-roll or even device-to-device variability that will determine whether this technology will move beyond the laboratory stage. Currently, OTFTs are not suitable for very high switching speed applications due to low mobility. Consequently, high voltage and reverse recovery time are required to drive OTFTs devices.

6 Conclusions

Low cost and considerably lower temperature fabrication of flexible organic transistors make them suitable candidates for several futuristic low-cost, flexible devices and circuits. This has attracted researchers from all over the globe to the exciting domain of organic electronics. Consistent research work in organic devices has brought about steady improvement in the transistor's performance.

Many technical issues related to OTFT structures, materials, compact dc models, operating principle, fabrication and performance parameters have been discussed. Comparative analyses of various OTFT structures, *viz.* TGBC, TGTC, BGTC and BGBC, have been done based on simulated results. OTFT performance has been characterized in terms of field effect mobility, drive current, on/off current ratio, threshold voltage, sub-threshold slope and transconductance.

Observations reveal that OTFT structures with top contact exhibit superior performance as compared to those with bottom contact in terms of mobility, transconductance and maximum drive current. Moreover, BGTC structure exhibit best operating functionality among all OTFT structures. The analysis further indicates that not only device structure, but also, material properties and fabrication process affects device performance, particularly, operating speed and signal sensitivity.

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