Six-Level Single-Leg Flying Capacitor Converter Voltage Balancing Dynamics Analysis

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***Abstract*– Natural voltage balancing property is an attractive feature of a flying capacitor converter. In this paper, time domain approach based on stitching piece-wise analytical solutions for consecutive switching intervals is applied to a six-level single-leg flying capacitor converter. The small parameter approximation analysis yields physically meaningful, simple, and accurate expressions for average voltage balancing dynamics giving an in-depth insight into parameters and carrier frequency impact for carrier-based phase-shifted DC PWM.**

***Keywords*—Voltage Source Converter (VSC), High Voltage power converters, Multilevel converters, Pulse Width Modulation (PWM), Modulation strategy.**

I. INTRODUCTION

Multilevel converters are being progressively used for medium and high voltage / power applications [1, 2]. Flying Capacitor (FC) multilevel PWM converter may be an attractive choice due to its natural voltage balancing property.

It is recognized that FC converter voltage balancing process is driven by load current high order harmonics [3-7]. More specifically, the voltage balancing mechanism essence consists in capacitor excessive "voltage unbalance" energy dissipation by switching harmonics. Though it is a common practice to consider a primitive series LR-load (copper loss), the voltage balancing dynamics is accelerated by additional power loss mechanisms like PWM eddy current iron core loss, skin effect [7] and other.

FC converter analytical voltage balancing research mostly deals with an AC modulation [3-7]. As an FC converter may be well used for DC/DC power conversion [8], it is reasonable to get started with gaining an in-depth understanding of the average voltage balancing dynamics mechanisms for more simple DC PWM case.

The reported FC converter voltage balancing dynamics analysis methods are essentially based on frequency domain transformations. However, it seems somewhat unnatural to use "intermediate" heavy frequency domain methods for derivation of linear time invariant models for the purpose of time domain analysis. As a result, the reported voltage balancing analysis methods are rather algorithmic than true analytical and, therefore, don't give a thorough insight into voltage balancing process physical nature.

The alternative approach based on time domain “stitching” analytical transient solutions for consecutive PWM period switching intervals is more adequate for understanding voltage balancing mechanism [9]. A basic single-leg three-level FC converter study was carried out resulting in a simple accurate expression for a voltage balancing dynamics time constant that is valid under practical assumptions of inductance limited load ripple current and reasonably low capacitor ripple voltage [9]. In [10, 11] this approach was applied to four- and five-level single-leg converters.

While the approach [9-11] delivers simple transparent final expressions for voltage balancing time constants, frequencies, and capacitor voltage balancing dynamics, it involves complex mathematical transformations like matrix multiplications, series expansions, and polynomial roots calculations. These could hardly be executed manually and, therefore, require an extensive use of symbolic calculation tools (like Maple). The intermediate results are so bulky that it is quite difficult to communicate and publish them. And, finally, the derivation of simplified averaged voltage balancing dynamics equations that don't contain fast average load current dynamics in [9-11] is rather intuitive.

Simple "physical" approach to FC converter averaged voltage balancing dynamics analysis was suggested in [12]. First, non-damped solutions for zero loss are derived. Second, damping time constants are determined based on understanding of the fact that FC voltage balancing mechanism is driven by excessive capacitor "voltage unbalance" energy dissipation in converter load by switching voltage / current harmonics. In principle, all the required calculations can be carried out manually.

This simple technique makes essential use of the two "small parameter" assumptions:

1) inductance limited load ripple current;

2) relatively large capacitances so that FC average voltage does not change much on a single PWM period.

Using this technique, it is quite easy to reproduce averaged voltage balancing dynamics solutions for single-leg three-, four-, and five-level FC converters obtained in [9-11].

In this paper, time domain analysis is applied to a six-level single-leg FC converter that yields simple, comprehensive, physically meaningful solution for the averaged voltage balancing dynamics. The ratios of capacitances must be better fixed in advance (due to "the curse of dimensionality", for arbitrary capacitances the final formulas become too bulky).

For single-leg three-, four-, and five-level FC converters AC PWM solution was obtained from that for DC PWM by averaging on AC fundamental period. Unfortunately, this does not work for a single-leg six-level FC converter and, therefore, no comprehensive solution for AC PWM is suggested.

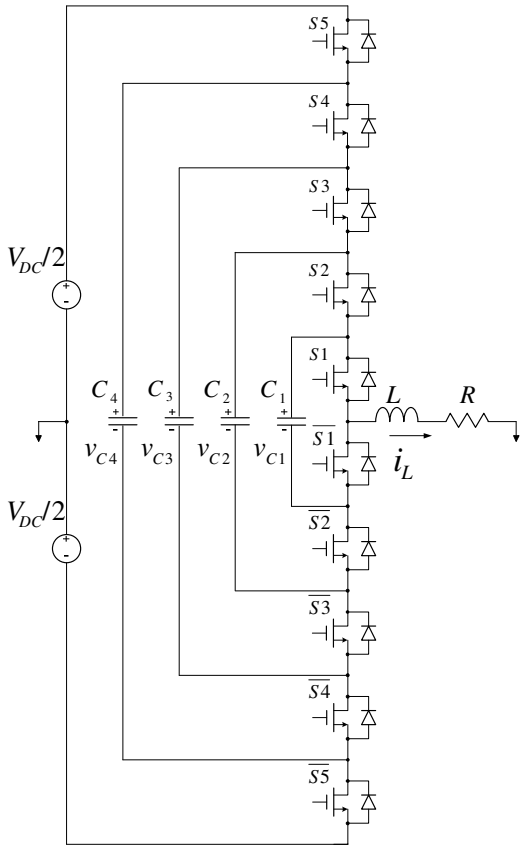

Fig. 1. Single-leg six-level FC converter with RL-load

II. Single-Leg Six-Level FC Converter Topology and Modulation Strategy

Single-leg six-level FC converter topology is shown in Fig.1. Consider positive normalized voltage commands $0<D<1$. Voltage command intervals $0<D<1/5$, $1/5<D<3/5$, $3/5<D<1$ must be considered on separate.

Phase-shifted carrier-based voltage modulation strategy for normalized voltage command $3/5<D<1$ is demonstrated in Fig.2. Voltage command V_{COM} is scanned by five triangular wave carrier signals to generate switching instants.

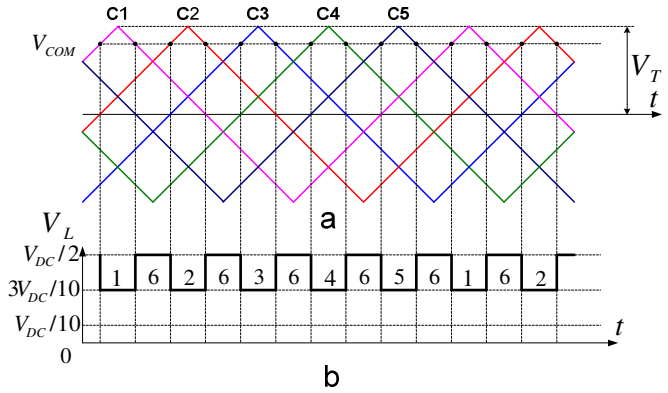

Fig. 2. Voltage modulation process (a) and output voltage waveform with switching states (b) for normalized voltage command $3/5<D<1$

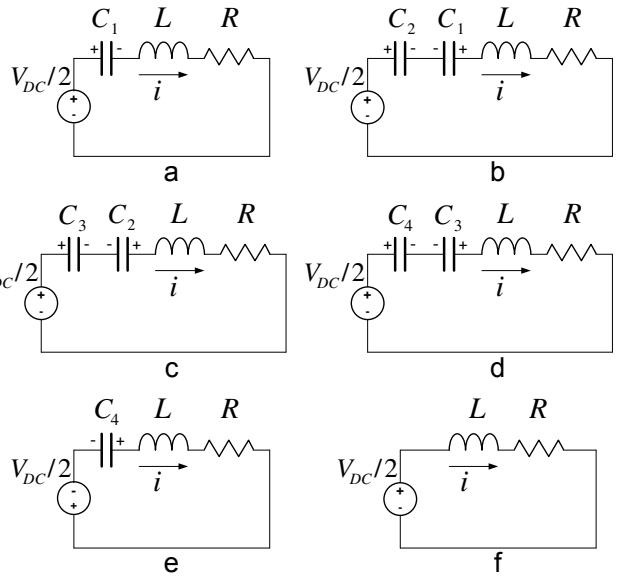

Fig. 3. FC converter topologies for $3/5<D<1$: a – 1, b – 2, c – 3, d – 4, e – 5, f – 6

The carrier signal *C1* (*C2; C3; C4*; *C5*) is responsible for generating the switching instants for the complementary switch pair $S1-\overline{S1}$ ($S2-\overline{S2}$; $S3-\overline{S3}$; $S4-\overline{S4}$, $S5-\overline{S5}$).

Fig.2,b shows converter switching states and output voltage waveform assuming ideal switches and the balanced capacitor voltages

$$v_1 = V_{DC}/5; \quad v_2 = 2V_{DC}/5; \\ v_3 = 3V_{DC}/5; \quad v_4 = 4V_{DC}/5. \tag{1}$$

A switching period is comprised of ten intervals. Interval 1, 2, 3, 4, 5 topologies generate the load voltage 3Vdc/10; five occasions of topology 6 – the load voltage of Vdc/2 (Fig.3). For topology 6, converter load is directly connected to the positive half of the power supply – all the "positive" switches *S1*, *S2*, *S3*, *S4* and *S5* are in conductance state and all the capacitors are disconnected.

Switching intervals duration

$$\Delta t_1 = \Delta t_2 = \Delta t_3 = \Delta t_4 = \Delta t_5 = (1-D)T_{PWM}/2, \tag{2}$$

where T_{PWM} - PWM period; $D = V_{COM}/V_T$ - normalized DC voltage command (Fig.2);

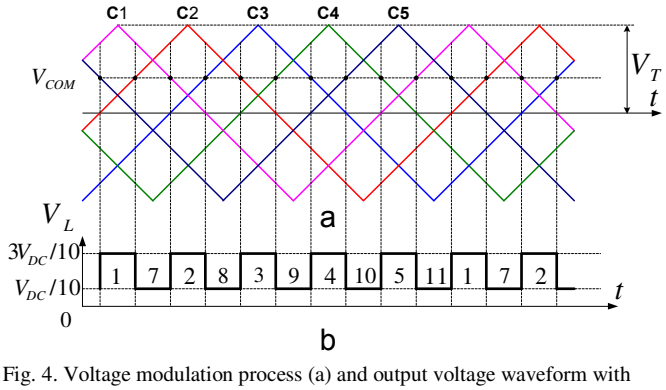

Fig. 4. Voltage modulation process (a) and output voltage waveform with switching states (b) for normalized voltage command $1/5<D<3/5$

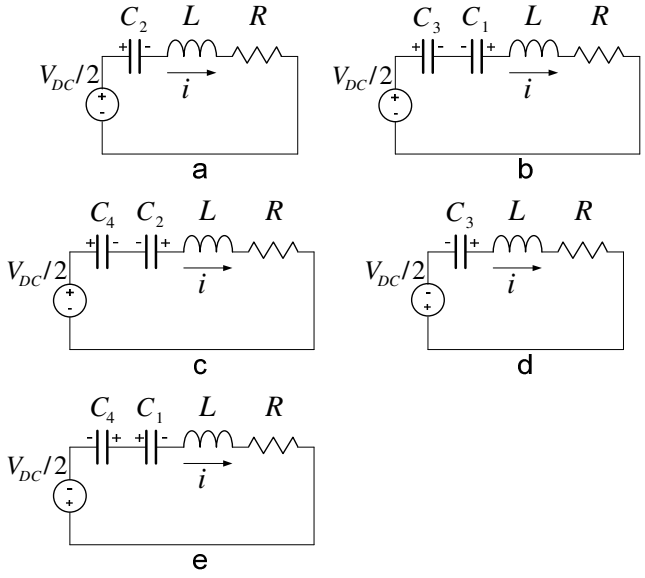

Fig. 5. FC converter Vdc/10 topologies: a – 7, b – 8, c – 9, d – 10, e – 11

$$\Delta t_6 = (D - 3/5)T_{PWM}/2. \quad (3)$$

Modulation strategy for *1/5<D<3/5* is illustrated by Fig.4. Five occasions of topology 6 (Fig.2) are replaced by five Vdc/10 output voltage topologies 7, 8, 9, 10, 11 (Fig.5).

Switching intervals duration for this case

$$\Delta t_1 = \Delta t_2 = \Delta t_3 = \Delta t_4 = \Delta t_5 = (D - 1/5)T_{PWM}/2, \quad (4)$$

$$\Delta t_7 = \Delta t_8 = \Delta t_9 = \Delta t_{10} = \Delta t_{11} = (3/5 - D)T_{PWM}/2. \quad (5)$$

Modulation strategy for *-1/5<D<1/5* is shown in Fig.6. Five Fig.6 topologies 12, 13, 14, 15, 16 that produce –Vdc/10 output voltage are presented in Fig.7.

Switching intervals duration for this case

$$\Delta t_7 = \Delta t_8 = \Delta t_9 = \Delta t_{10} = \Delta t_{11} = (1/5 + D)T_{PWM}/2, \quad (6)$$

$$\Delta t_{12} = \Delta t_{13} = \Delta t_{14} = \Delta t_{15} = \Delta t_{16} = (1/5 - D)T_{PWM}/2. \quad (7)$$

Phase-shifted carrier-based modulation strategy (Fig.2, Fig.4, Fig.6) provides optimal nearest level switching PWM voltage quality. While this strategy makes use of all possible 3Vdc/10 (-3Vdc/10) switching states (Fig.3) that is essential for natural voltage balancing, it employs only five Vdc/10 (-Vdc/10) topologies Fig.5 (Fig.7) and does not use other possible five states with three and four capacitors in series. This way, other

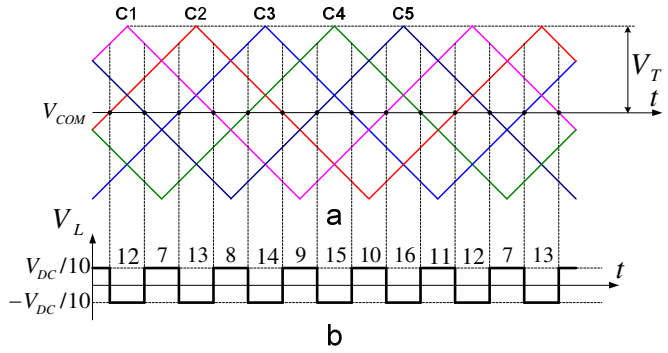

Fig. 6. Voltage modulation process (a) and output voltage waveform with switching states (b) for normalized voltage command *-1/5<D<1/5*

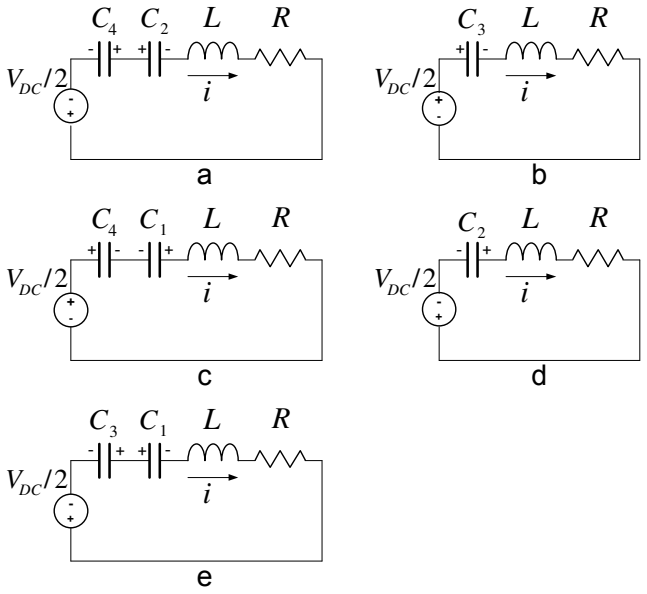

Fig. 7. FC converter -Vdc/10 topologies: a – 12, b – 13, c – 14, d – 15, e – 16

optimal voltage quality modulation strategies are possible that may provide better natural voltage balancing dynamics rate.

III. FC Converter Voltage Balancing Dynamics Modeling

For a given voltage command *D*, single-leg six-level FC converter is a fifth order linear switched system. On each switching interval, it is described by the state-space equation

$$X(t) = A_j(t)X(0) + B_j(t)V_{DC}/2; \quad (8)$$

$$X(t) = \left[i(t) \quad v_1(t) \quad v_2(t) \quad v_3(t) \quad v_4(t)\right]^T; j = 1,...,10.$$

The state-space matrices and vectors in (8) are obtained by analytically solving on the separate switching intervals the first and second order linear ordinary differential equations [9-11]. Though we assume oscillating step response of individual LCR-circuits (Fig.3, Fig.5, Fig.7), it does not limit the final results generality as long as small parameter assumptions hold.

For the intervals with two capacitors connected in series, the solution is first obtained for the second order circuit with an equivalent capacitance and initial voltage condition. Individual capacitor voltages are then found using the law of charge conservation.

For 3/5<*D*<1 voltage command interval, a discrete FC converter model for calculating the state-space variables at the switching instants becomes

$$\begin{aligned} &X(t_1) = A_1(\Delta t_1)X(0) + B_1(\Delta t_1)V_{DC}/2; \\ &X(t_2) = A_6(\Delta t_6)X(t_1) + B_6(\Delta t_6)V_{DC}/2; \\ &\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\ &X(t_{10}) = A_6(\Delta t_6)X(t_9) + B_6(\Delta t_6)V_{DC}/2; \\ &X(t_{11}) = A_1(\Delta t_1)X(t_{10}) + B_1(\Delta t_1)V_{DC}/2; \\ &\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \end{aligned} \quad (9)$$

where

$$t_1 = \Delta t_1;$$

$$t_2 = \Delta t_1 + \Delta t_6;$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (10)$$

$$t_{10} = \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5 + 5\Delta t_6 = T_{PWM};$$

$$t_{11} = T_{PWM} + \Delta t_1;$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

Example 1. Consider single-leg six-level FC converter: $V_{DC} = 50V$; $R = 1Ohm$; $L = 0.5mH$; $C_1 = C_2 = C_3 = C_4 = = C = 400uF$; $T_{PWM} = 560us$ $(1.8kHz)$.

Converter dynamics switched simulation results obtained by programming formulas (9), (10) are presented in Fig.8.

The average load current and capacitor voltages converge to

$$i(\infty) = V_{DC} D/(2R);$$

$$v_1(\infty) = V_{DC}/5; \quad v_2(\infty) = 2V_{DC}/5; \quad (11)$$

$$v_3(\infty) = 3V_{DC}/5; \quad v_3(\infty) = 4V_{DC}/5$$

for any set of initial conditions.

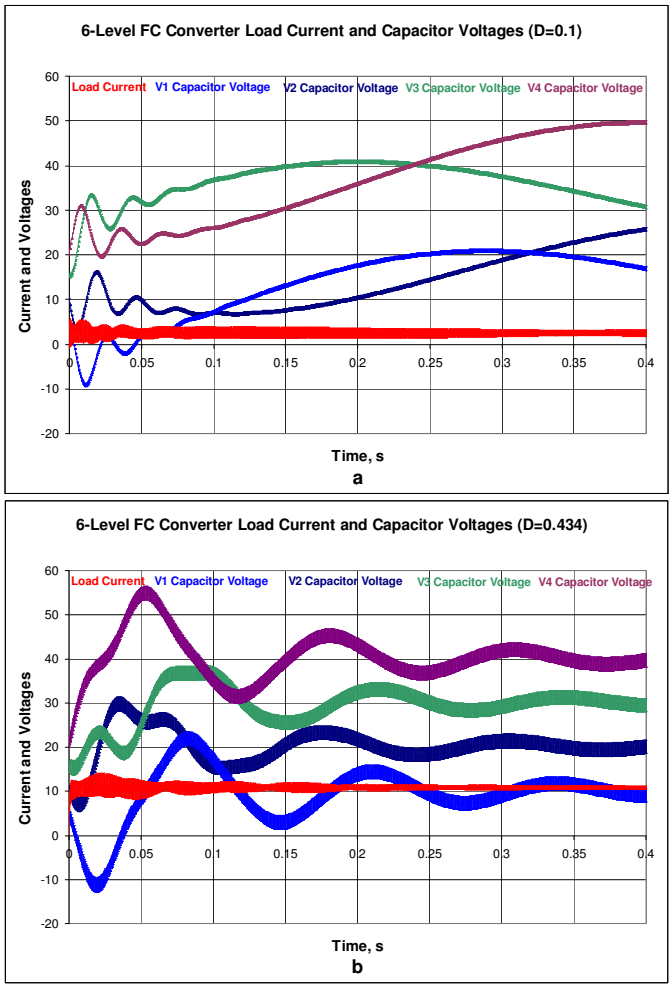

Fig. 8. FC converter current and capacitor voltages switched simulation for different voltage commands and initial conditions: a - *D*=0.1; b - *D*=0.434

Fig.8 shows that load current settles very fast. Capacitor voltages response is comprised of high frequency component with relatively strong damping and dominating low frequency component with relatively weak damping.

In the examples throughout this paper, the switches are assumed ideal with reverse voltage blocking capability. This is not correct for the real life switches with anti-parallel diodes. As the natural voltage balance condition $v_1 < v_2 < v_3 < v_4$ tends to be violated due to unbalanced initial conditions and oscillating response, the anti-parallel diodes come into play and the linear model is no more valid due to non-linear clamping effects. However, if the capacitor voltages are balanced and the DC bus disturbance is moderate, then the above condition is never violated and the linear model is valid for the real life switches [7].

IV. FC Converter Voltage Balancing Dynamics for DC Modulation

Suppose that the interval 1 initial conditions are substituted, along with the interval 1 duration, into the interval 1 dynamic solution. This gives initial conditions for the next interval 6. By substituting them with the interval 6 duration into the interval 6 dynamic solution, initial conditions for the interval 2 are obtained. Carrying out the same procedure for the rest of PWM subintervals 2-6-3-6-4-6-5-6 completes a PWM period and a linear difference vector equation for *3/5<D<1* is obtained in the form

$$X(t + T_{PWM}) = A(D)X(t) + B(D)V_{DC}/2, \quad (12)$$

where

$$A(D) = A_6 A_5 A_6 A_4 A_6 A_3 A_6 A_2 A_6 A_1;$$

$$B(D) = A_6(A_5(A_6(A_4(A_6(A_3(A_6(A_2(A_6B_1 + B_6) + B_2) + \quad (13)$$

$$+ B_6) + B_3) + B_6) + B_4) + B_6) + B_5) + B_6.$$

While calculating matrix A and vector B in (12), the switching interval 1 was selected the first one (Fig.2). It can be shown that the other nine possibilities to get started will produce different system matrices but the same transient behavior (the same eigenvalues).

A similar procedure may be carried out for *1/5<D<3/5* and *0<D<1/5*.

Assuming system (12) stability, a steady state solution may be found as

$$X(\infty) = (I - A(D))^{-1} B(D)V_{DC}/2, \quad (14)$$

I - unity matrix.

Generally speaking, the solution (14) is a function of the normalized voltage command D and also depends on the selected intervals order 1-6-2-6-3-6-4-6-5-6, 6-2-6-3-6-4-6-5-6-1, 2-6-3-6-4-6-5-6-1-6, ... However, for a good practical converter load current and capacitor voltage ripples should be low enough and solution (14) is supposed to be close to (11) for any of the ten possible interval orders.

Using "on average" derivatives approximation

$$\frac{di}{dt} \approx \frac{i(t+T_{PWM})-i(t)}{T_{PWM}}; \quad \frac{dv}{dt} \approx \frac{v(t+T_{PWM})-v(t)}{T_{PWM}}, \qquad (15)$$

from (12) the FC converter "averaged" voltage balancing dynamics continuous time model in the form of differential equation becomes

$$\frac{dX}{dt} = \frac{1}{T_{PWM}}\big(A(D)-I\big)X + \frac{1}{T_{PWM}}B(D)V_{DC}/2. \qquad (16)$$

An accurate solution and switched simulation will show five times switching frequency ripples in load current and capacitor voltages that are filtered out in the averaged models (12), (16).

FC converter averaged voltage balancing dynamics analysis methodology [9-11] comprises the following steps. First, we obtain the characteristic polynomial of matrix *A(D)* (13)

$$P(\lambda) = \lambda^5 + b_4\lambda^4 + b_3\lambda^3 + b_2\lambda^2 + b_1\lambda + b_0. \qquad (17)$$

As the matrix *A(D)* is about multiplying 10 5x5 matrices, this could hardly be done manually and requires an assistance of some symbolic calculations tool.

Second, each coefficient of (17) is expanded into power series of a small parameter (multiplied by some function of *D*)

$$\beta = \omega_1 T_{PWM} << 1, \qquad (18)$$

where $\omega_1 = \sqrt{\omega_{10}^2 - \alpha^2}$; $\omega_{10}^2 = 1/(LC_1)$, $\alpha = R/(2L)$.

The small parameter assumption is valid for practical converters that have low ripple current (inductance dominated load) and low ripple voltage (reasonably large capacitance).

Though oscillating step response of all required LCR-circuits is assumed (relatively small capacitance), the results are general and hold for relatively large capacitances $C > 4L/R^2$ as well though, most likely, this is not a practical FC converter case.

The selection of the series expansion maximum power for the coefficients (17) is dictated by the accuracy considerations for the polynomial roots with a modulus close to unity.

Third, the roots of (17) with the series expanded coefficients are found analytically in the form of series expansion. For the small parameter approximation (18), it may be shown that there is always one real root and two pairs of complex conjugate roots.

The above calculations must be performed on separate for *3/5<D<1*, *1/5<D<3/5* and *0<D<1/5*.

The real root is positive

$$0 < \lambda < 1$$

and delivers the averaged continuous system time constant

$$T(D) = -T_{PWM}/\ln(\lambda) = L/R \qquad (19)$$

that is actually load current (fast) time constant that does not depend on the normalized voltage command *D* because load voltage averaged on a PWM period practically does not depend on the individual capacitor voltages [9-11].

Each complex roots pair of characteristic equation (17)

$$\lambda^{(1,2)} = m\exp(\pm j\theta), 0 < m \le 1 \qquad (20)$$

generates equivalent continuous system voltage balancing angular frequency and damping time constant

$$\omega = \theta/T_{PWM};$$
$$T_P = -T_{PWM}/\ln(m). \qquad (21)$$

Considering arbitrary capacitances makes voltage balancing frequency and especially time constant expressions too bulky. Therefore, it is suggested to select fixed capacitances ratios. Below four equal capacitances $C_1 = C_2 = C_3 = C_4 = C$ are assumed for the sake of simplicity. However, there is any no problem to consider different capacitance ratios, for example, $C_1 = 2C_2 = 3C_3 = 4C_4 = C$.

Voltage balancing angular frequencies and time constants amount to:

for *0<D<1/5* –

$$\omega_{1,2} = \frac{T_{PWM}\sqrt{3750D^4 - 900D^2 + 150 \pm 10\sqrt{E}}}{8LC}; \qquad (22)$$

$$E = (625D^4 - 190D^2 + 17)(125D^4 + 10D^2 + 13),$$

$$T_{1,2} = \frac{1500L^2C\sqrt{E}}{RT_{PWM}^2 W_{1,2}};$$

$$W_{1,2} = 3750D^6 + 1350D^4 - 1190D^2 + 154 \pm H; \qquad (23)$$

$$H = \sqrt{E}(11 - 15D^2),$$

for *1/5<D<3/5* –

$$\omega_{1,2} = \frac{T_{PWM}\sqrt{F \pm 10\sqrt{10G}}}{200LC};$$

$$F = 1875D^4 - 3000D^3 + 1650D^2 - 600D + 195; \qquad (24)$$

$$G = (25D^4 - 30D^3 + 4D^2 + 2D + 1)\times$$
$$\times(125D^4 - 300D^3 + 290D^2 - 140D + 29),$$

$$T_{1,2} = \frac{60000L^2C\sqrt{P}}{RT_{PWM}^2 Q_{1,2}};$$

$$P = (25D^4 - 30D^3 + 4D^2 + 2D + 1)\times$$
$$\times(125D^4 - 300D^3 + 290D^2 - 140D + 29); \qquad (25)$$

$$Q_{1,2} = \pm\sqrt{10}(31250D^7 - 98125D^6 + 113250D^5 -$$
$$- 49225D^4 - 4650D^3 + 8585D^2 - 330D - 627) -$$
$$- \sqrt{P}(600D^2 - 440),$$

for *3/5<D<1* –

$$\omega_{1,2} = \frac{(1-D)^2 T_{PWM}}{16LC}\left(\sqrt{5} \pm 1\right), \qquad (26)$$

$$T_{1,2} = \frac{3000L^2C}{RT_{PWM}^2(1-D)^2(125D - 5 \pm 12\sqrt{5})}. \qquad (27)$$

Two oscillation frequencies and two time constants (22)-(27) are piecewise analytical functions of *D* continuous with their first derivatives at the stitching points *D=1/5* and *D=3/5*. Their graphs are presented in Fig.9.

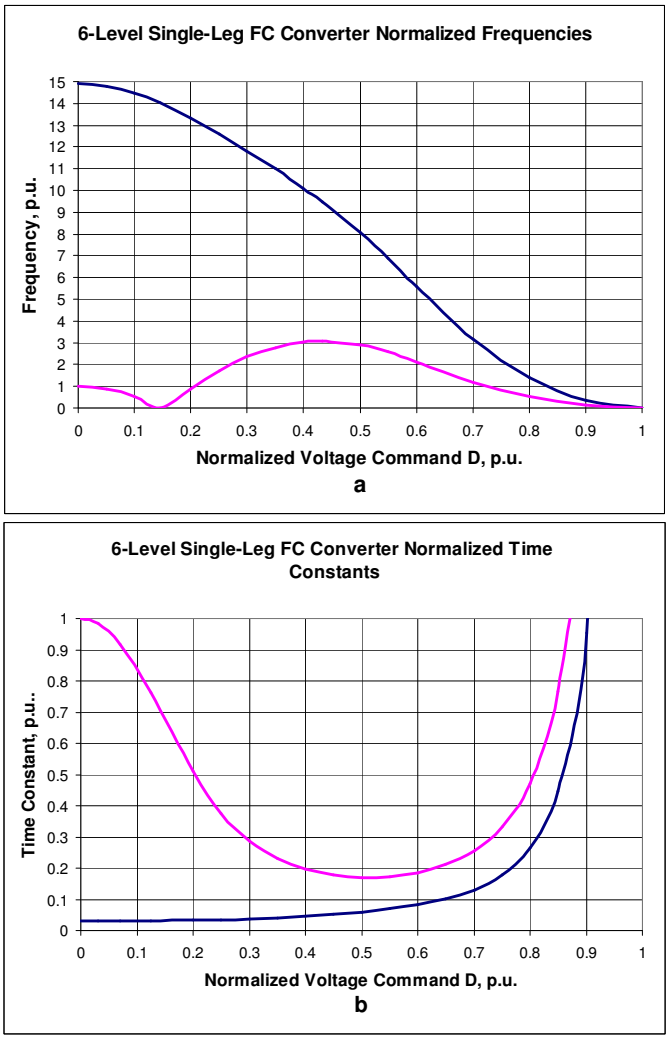

Fig. 9. FC converter voltage balancing dynamics frequencies (a) and time constants (b) for equal capacitances

While the high frequency is decreasing monotonically in D, the low frequency equals zero for $D=0.145$ and has maximum for $D=0.434$ (Fig.8,b).

The high frequency related time constant is increasing monotonically while the low frequency time constant has minimum for $D=0.5$. Note relatively poor voltage balancing rate for $D=0$ and small D. This may hopefully be improved by better modulation strategy without compromising optimal voltage quality (see discussion in Section II).

V. Voltage Balancing Dynamics Solutions

Simple physical approach to FC converter averaged voltage balancing dynamics analysis [12] makes it possible to obtain non-damped linear time-invariant differential equations zero load resistance and zero DC bus voltage

$$X'(t) = A(D)X(t), \quad X(0) = X_0; \qquad X(t) = \left[v_1(t) \quad v_2(t) \quad v_3(t) \quad v_4(t)\right]^T. \tag{28}$$

Calculation of state-space matrices for different voltage command intervals yields

for $3/5<D<1$ –

$$A(D) = \frac{(1-D)^2 T_{PWM}}{8L}\begin{bmatrix} 0 & \frac{1}{C_1} & 0 & 0 \\ -\frac{1}{C_2} & 0 & \frac{1}{C_2} & 0 \\ 0 & -\frac{1}{C_3} & 0 & \frac{1}{C_3} \\ 0 & 0 & -\frac{1}{C_4} & 0 \end{bmatrix}; \tag{29}$$

for $1/5<D<3/5$ –

$$A(D) = \frac{T_{PWM}}{8L}\begin{bmatrix} 0 & \frac{a(D)}{C_1} & \frac{b(D)}{C_1} & -\frac{b(D)}{C_1} \\ -\frac{a(D)}{C_2} & 0 & \frac{a(D)}{C_2} & \frac{b(D)}{C_2} \\ -\frac{b(D)}{C_3} & -\frac{a(D)}{C_3} & 0 & \frac{a(D)}{C_3} \\ \frac{b(D)}{C_4} & -\frac{b(D)}{C_4} & -\frac{a(D)}{C_4} & 0 \end{bmatrix}, \tag{30}$$

where

$$a(D) = (-25D^2 + 10D + 7)/25; \qquad b(D) = (3/5 - D)^2, \tag{31}$$

for $0<D<1/5$ – the same structure matrix (30) with

$$a(D) = 8/25; \qquad b(D) = (6 - 50D^2)/25. \tag{32}$$

Matrix $A(D)$ elements defined by (29)-(32) are continuous with their first derivatives in stitching points $D=1/5$ and $D=3/5$.

Matrices (29), (30) are skew symmetric and have biquadratic characteristic equations. Two pairs of conjugate imaginary eigenvalues define two oscillation frequencies that, for equal capacitances, coincide with (22), (24), (26).

Once oscillation frequencies are found, it is possible to write down solutions of homogeneous non-damped equations (28) with (29)-(32)

$$v_i(t) = s_{1i}\sin\omega_1 t + c_{1i}\cos\omega_1 t + s_{2i}\sin\omega_2 t + c_{2i}\cos\omega_2 t; \quad i = 1...4. \tag{33}$$

For $3/5<D<1$, matrix (29) is sparse two-diagonal and its dependence on D is "scalar". Therefore, coefficients in (32) depend on initial voltage conditions only while the dependence on D is in oscillation frequencies similar to what is observed for single-leg three-, four-, and five-level FC converters [9-11].

For $0<D<1/5$ and $1/5<D<3/5$, state matrices (30) with (31), (32) are dense with different element dependences on D. As a result, coefficients in (33) depend both on initial conditions and on normalized voltage command D that is a consequence of complexity increase with level count rise to six.

After non-damped homogeneous solutions (33) are found using linear differential equations theory, it is easy to obtain capacitor voltage balancing dynamics solutions by accounting

for damping time constants (23), (25), (27) and non-zero DC bus voltage.

To incorporate a non-zero DC bus voltage (forced solution) into (32), one has to add the balanced capacitor voltage values (1) and to replace the initial conditions according to

$$v_1(0) \to v_1(0) - V_{DC}/5; \quad v_2(0) \to v_2(0) - 2V_{DC}/5; \\ v_3(0) \to v_3(0) - 3V_{DC}/5; \quad v_4(0) \to v_4(0) - 4V_{DC}/5. \tag{34}$$

The final expressions are a little bit bulky and, therefore, are not presented here. Their comparison with accurate switched simulation results (Fig.10) shows good practical accuracy of approximate averaged voltage balancing dynamics solutions.

Due to the carrier signals order *C1; C2; C3; C4*; *C5* phase-shifted PWM strategy (Fig.2, 4, 6) may be referred to as "lead" one. Alternatively, PWM with reverse order *C5; C4; C3; C2*; *C1* may be considered as "lag" strategy.

As may be easily observed, the lag PWM strategy generates inverse switching states order with respect to the lead one. Lag PWM voltage balancing dynamics solution may be formally obtained from that for lead modulation by changing to the opposite the signs of sinusoidal terms in (33) [10, 11].

VI. FC Converter Voltage Balancing Dynamics Analysis for AC Modulation

For AC PWM, the FC dynamics models become linear time-variable. For three-, four-, and five-level single-leg converters voltage balancing dynamics solutions for AC PWM were obtained from those for DC PWM by averaging oscillation frequencies and inverse time constants on AC fundamental period [9-11]. An explanation may be that this is possible due to "scalar" type dependence of non-damped equations on D similar to (28), (29). In six-level FC converter case, the situation is more complicated because for *0<D<1/5* and *1/5<D<3/5* non-damped equation matrix (30) has different element dependences on *D*.

Intuitively, the right thing to do in this situation is to average original DC PWM equations rather than their solutions.

For AC PWM with a modulation index *M*, *0<M<1*, an instantaneous voltage command is

$$D(t) = M \sin(\omega_f t). \tag{35}$$

Assuming relatively high AC fundamental frequency, original DC PWM non-damped equations (28)-(32) may be averaged for *0<M<1* accounting for matrix elements symmetric, even behavior for *0<D<1* and *-1<D<0* (for negative *D*, it must be replaced by its modulus |*D*|).

The averaged vector equation for AC PWM then becomes

$$X'(t) = A(M)X(t), \quad X(0) = X_0; \\ X(t) = \left[v_1(t) \quad v_2(t) \quad v_3(t) \quad v_4(t)\right]^T, \tag{36}$$

where

$$A(M) = \frac{T_{PWM}}{8L}\begin{bmatrix} 0 & \frac{a(M)}{C_1} & \frac{b(M)}{C_1} & -\frac{b(M)}{C_1} \\ -\frac{a(M)}{C_2} & 0 & \frac{a(M)}{C_2} & \frac{b(M)}{C_2} \\ -\frac{b(M)}{C_3} & -\frac{a(M)}{C_3} & 0 & \frac{a(M)}{C_3} \\ \frac{b(M)}{C_4} & -\frac{b(M)}{C_4} & -\frac{a(M)}{C_4} & 0 \end{bmatrix}. \tag{37}$$

For *0<M<1/5*, by averaging (32)

$$a(M) = 8/25; \\ b(M) = (6 - 50D^2)/25. \tag{38}$$

For *1/5<M<1*, the expressions for coefficients become more cumbersome and are not presented here.

Similar to DC PWM, oscillation frequencies for AC PWM are found by calculating the roots of characteristic polynomial of matrix (37).

Voltage balancing oscillation frequencies for AC PWM are shown in Fig.11. Note that the low frequency becomes zero for *M* slightly larger than *0.2*.

AC PWM voltage balancing dynamics switched simulation results are presented in Fig.12. Comparison of Fig.12, a and Fig.12, b confirms that voltage balancing process for AC PWM is practically not affected by (relatively high) AC fundamental frequency [9-11].

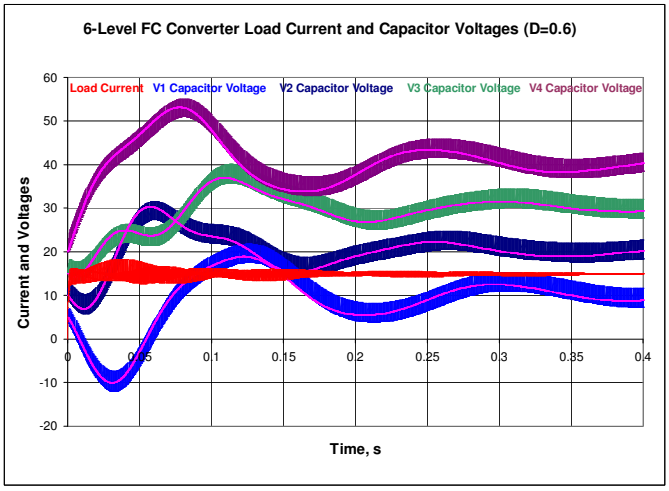

Fig. 10. FC converter switched simulation results comparison with analytical voltage balancing dynamics approximation (pink lines) - *D*=0.6

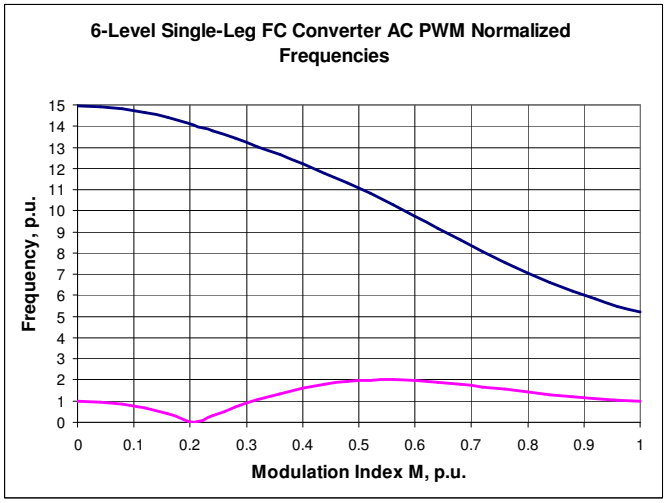

Fig. 11. FC converter voltage balancing dynamics frequencies for AC PWM

Fig.12, c confirms that for modulation index *M=0.2* the low oscillation frequency is very close to zero.

The authors have to admit that so far they don't have a comprehensive solution for AC PWM time constants and voltage balancing dynamics.

VII. Conclusion

This paper investigated into natural voltage balancing dynamics for a six-level single-leg FC converter with carrier-based phase-shifted modulation. Using time domain averaging and small parameter approximation, derived are simple, accurate, and physically meaningful expressions for voltage balancing frequencies and time constants and capacitor voltage balancing dynamics for DC PWM. The obtained solutions clearly reveal the dependences on inductive load parameters, carrier frequency, voltage command, lead / lag PWM strategy.

For AC PWM, the analysis ended up with voltage balancing dynamics oscillations frequencies. Switched simulations confirm that AC fundamental frequency has no impact on averaged natural voltage balancing dynamics. Strict AC PWM analysis including time constants and voltage balancing dynamics solution is a challenging topic for future research. Another future research topic is investigation into modulation strategies different from phase-shifted PWM that may deliver faster voltage balancing dynamics, especially, for small normalized DC voltage commands (modulation indices).

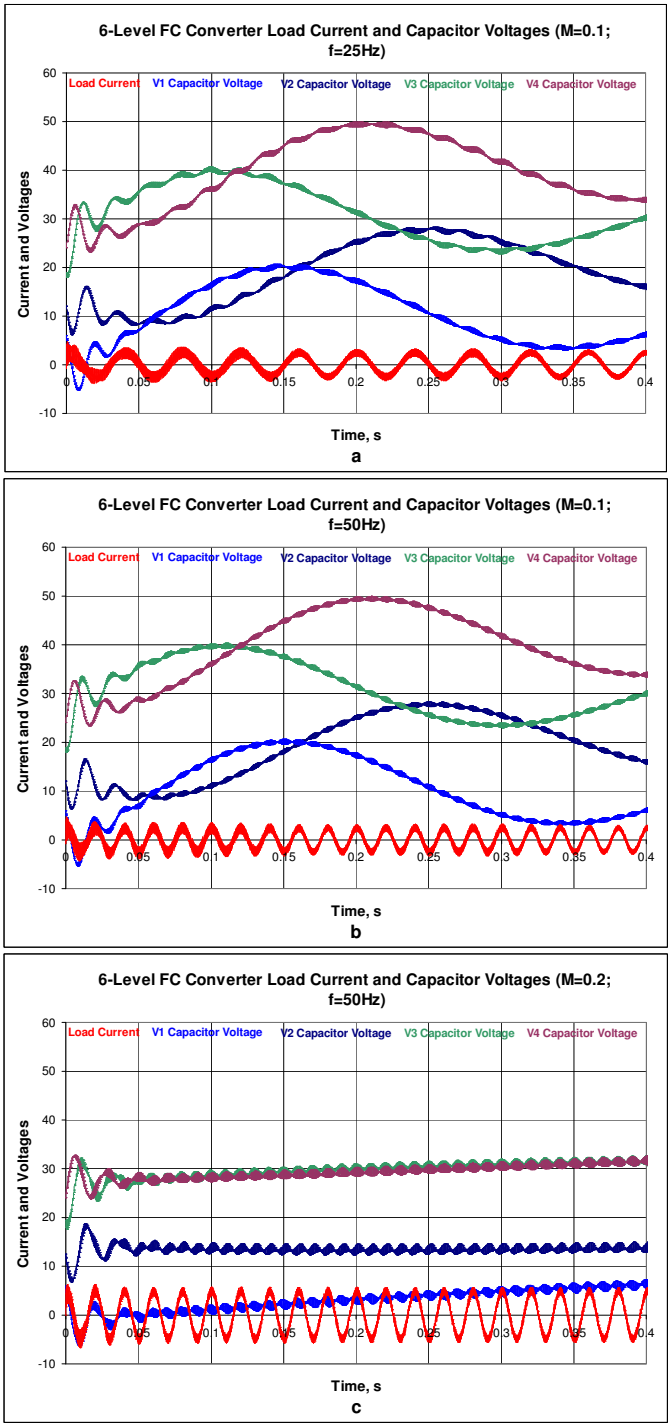

Fig. 12. FC converter current and capacitor voltages simulation for AC PWM: a - *M*=0.1, 25Hz; b – M=0.1, 50Hz; c – M=0.2, 50Hz

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