High Aspect Ratio TSV Copper Filling with Different Seed Layers

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Abstract

The paper addresses the through silicon via (TSV) filling using electrochemical deposition (ECD) of copper. The impact of seed layer nature on filling ratio and void formation will be discussed with respect to via diameter and via depth. Based on the Spherolyte Cu200 the electrolyte for the copper electrochemical deposition was modified for good filling behavior. Thermomechanical modeling and simulation was performed for reliability assessment.

Introduction

3D integration is a fast growing field that encompasses different types of technologies. One of the most promising technologies is the through silicon via (TSV) technology for interconnecting stacked devices on wafer level to perform high density interconnects with a good electrical performance and a small form factor. Beside the formation of TSVs in the front-end process or back-end of line (BEOL), there is also a post front-end integration process for completely processed and tested CMOS device wafers. Such a process is used in Fraunhofer´s VSI approach described in [1,2]. The via filling processes basically deal with chemical vapor deposition (CVD) processes of tungsten or copper or electrochemical deposition (ECD) of copper. Future trends for stacked devices require copper filled TSV for optimized electrical performance. One of the specific characteristics of CVD processes are via dimensions, e.g. via diameter and via depth. The CVD processes is well suited for small sized vias (diameter: 3 µm to 5 µm) with a high aspect ratio (HAR) up to 20 which results in typical via depths in the range of 20 µm to 50 µm. Via sizes larger then 5 µm diameter and via depths acceding 20 µm are preferably filled by a copper electro-depo-sition process.

Cost of ownership is the most important criterion for increasing TSV application in 3D device stacking. Reliability yield and particular void free filling is a major issue besides filling speed. Here, the nature and quality of the seed layer and electrolyte chemistry act as key contributors. Fraunhofer IZM's and Atotech's Wafer Technology Division teamed up to investigate the impact of seed layer to the TSV filling process in detail.

Post Front-end TSV Process flow

An ECD TSV filling process, based on Atotech's SPHEROLYTE Cu 200 product family was integrated into the Fraunhofer IZM post front-end 3D TSV process. The generic process flow is briefly described based on the realization of a silicon interposer with TSV [5].

First, the high aspect ratio vias are formed by RIE (Figure 1a) using a so called Bosch-Process [3, 4] with a photo resist mask. For sidewall insolation of the vias a thermal oxidation can be performed or a CVD oxide [1, 2] is used. For the seed and barrier layer deposition CVD of W or Cu, but also sputtering processes, are applicable (Figure 1b). The filling of the vias is done by ECD of copper on the seed layer (Figure 1c). During the ECD, copper will be also deposited on the wafer surface. This layer can be used as pad- or wiring layer for the redistribution. The RDL formation uses standard build-up thin film processes with copper electroplating into photoresist openings followed by seed layer etching and polymer passivation (Figure 1d).

The interposer wafer is transferred on a temporary handling substrate by temporary additive bonding followed by a thinning sequence from the silicon back side (Figure 1e). The bottom side of the thinned interposer wafer is passivated and the IO terminals will be formed by passivation opening and thin film deposition (Figure 1f).

The interposer wafer is transferred from the top handling substrate to a bottom temporary handling substrate (Figure 1g) and is now ready for assembly (Figure 1h).

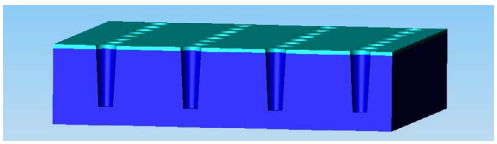


Figure 1a: Via Etching (RIE)

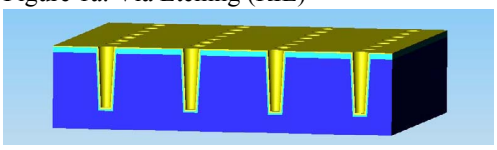


Figure 1b: Sidewall passivation and barrier seed layer deposition

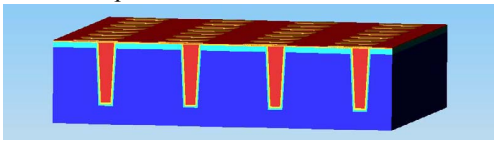


Figure 1c: Via Filling by ECD

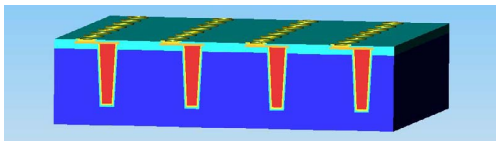


Figure 1d: RDL and IO pad preparation

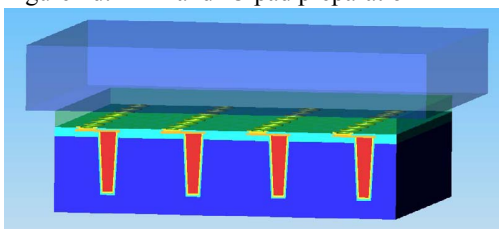


Figure 1e: Transfer to handling substrate

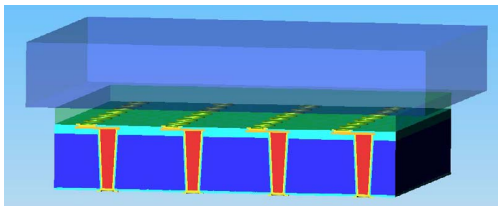


Figure 1f: Thinning and back side IO pad

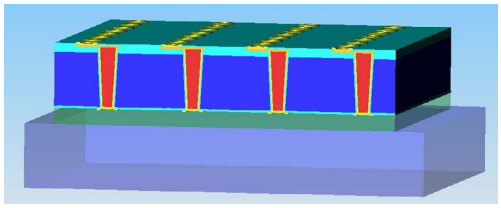


Figure 1g: Wafer transfer

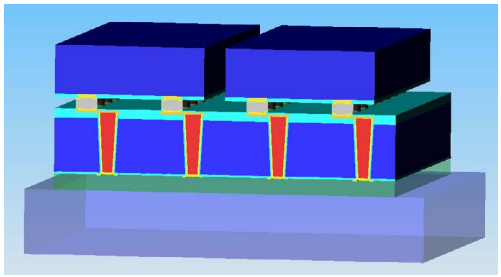


Figure 1h: Wafer level assembly

Figure 1a-h: Generic process flow for silicon interposer with Through Silicon Vias

Experimental TSV Filling Process Setup

The TSV manufacturing process has to be cost effective and CMOS compatible and comprise a void-free metal filling step. On one hand, the via filling depth is limited to a specific aspect ratio depending on the filling process, on the other hand, process filling time is shorter for smaller vias. But a certain via depth is needed defined by the functionality of the devices or further process integration steps, e.g. assembly/stacking. CVD processes allow higher aspect ratios but are limited in the deposited layer thickness and take place at higher temperature. Electrochemical Cu filling of vias with diameters >15 µm and depths up to >50 µm can be implemented as a cost effective low temperature process.

In this context and considering the economic point of view, the specific goal of the experiments was to find out, for which via dimensions (diameter and depth) sputtering is a suitable seed layer deposition process. So besides the different via dimensions, different seed layer processes were subjects of the investigations. As sputtered seed layer a standard adhesion and seed layer of TiW/ Cu was chosen. This process is characterized and successfully implemented in Fraunhofer IZMs leadfree solder CuSn/ SnAg micro-bumping and thin film Cu redistribution (RDL) process. For direct comparison with this TiW/ Cu seed layer at higher aspect ratios a Cu-CVD layer was chosen. As W-CVD is an established process for via filling in the VSI process [1], it was included into the comparison for seed layer deposition and via filling process. An attractive process in this specific case is also the combination of the CVD tungsten and sputtering of titanium/ tungsten-copper as seed layer followed by Cu electrodeposition for the small size vias in the range of 4 µm to 15 µm.

For the evaluation of the different seed layers two different test masks for 200 mm wafer have been used for the via formation. The first one (mask 1), which was used for most seed layers, comprises circular openings of 3, 5, 6, 11, 16, and 35 µm. The vias etched with this mask result in a varying depth between 42 µm for the 3 µm openings and 77 µm for the 35 µm openings. The second one (mask 2), which was only used for the combined W-CVD/Cu-PVD seed layer, comprises square openings of 5, 15, and 20 µm. The vias etched with this mask had a varying depth between 58 µm for the 5 µm openings and 94 µm for the 20 µm openings. For the passivation a thermal oxide was chosen.

The via/mask dimensions used for the plating are summarized in Table 1.

Via opening diameter (mask size)	Via opening diameter after etching	Via depth after etching (mask 1)	Via depth after etching (mask 2)
35	35	77	
20			94
16 (15)	18	67	(83)
11	12	63	
6	8	60	
5	6	52	58
3	4	42	

Table 1: mask size, via opening and depth after etching

Results and Discussion

ECD Cu Deposition with Spherolyte CupraBase 50 CT

The filling of the high aspect ratio TSV with electrolytic copper is a challenging process step. A perfect fill is required since incorporated seems or voids would ultimately cause interconnect failures and reliability issues. Furthermore, with respect to process integration, throughput and productivity, the “overburden”- the amount of copper which is deposited on the wafer top - as well as the process/plating time have to be minimized. [6]

To achieve a defect-free via fill, the copper deposition rate at the via bottom has to be higher than at its top and aperture area. Primary and tertiary current distribution do counteract this “super-conformal” or “bottom-up” growth, on the other hand suitable electrolyte additive chemistries and/or pulse reverse plating current profiles do promote a void-less fill.

Additives in sulphuric acid based copper electrolytes, which are commonly used for copper depositions for electronic applications, are organic components which impact the copper deposition kinetic, thereby acting as suppressors or anti-suppressors/accelerators. They are effective within the copper - electrolyte interface and their concentrations on the copper surface are related to mass transport, adsorption kinetic and consumption on the copper cathode.

Polyether-type additives or so called carriers, such as polyethylene glycol (PEG), do adsorb (together with chloride) on the entire cathode surface leading to a strong polarisation/suppression of the copper deposition reaction.

Thiols or brighteners like bis (3-sulfopropyl)-disulfide (SPS) displace or lift carrier-type suppressors thereby having a de-polarising/ accelerating effect on the copper deposition.

Molecular and polymer amine and heterocyclic compounds, the so called levelers, such as Janus Green B do adsorb preferentially on surface protrusions due to mass transport and electrostatic attraction effects leading to a selective surface suppression. The positively charged (protonated) levelers can inactivate the negatively charged brighteners (sulfonic acid group) whereby ion pairing interactions are postulated.

An appropriate additive selection in nature and concentration is necessary to achieve the required “bottom-up” fill. Thereby, especially the adjustment of the leveler components is essential as shown in the example in Figure 2.

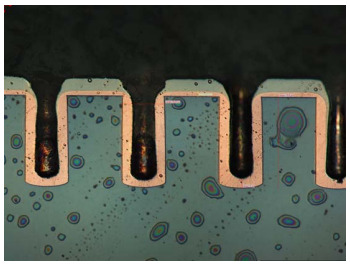
Here, vias with an opening of 35 µm in diameter and a depth of 70 µm are partially filled in order to evaluate the filling behavior. The Spherolyte Cu200 additive system was used whereby the concentration of the leveler component was increased in the short test series. In all experiments the same DC plating current profile was applied.

Without the leveler (see Figure 2a), a (sub-) conformal growth is seen which, most probably, would lead to void formation during filling. A pronounced “bottom-up” fill combined with a good suppression at the via entrance is observed after adding the leveling compound (Figure 2b). The via will be filled without defects. Further (over-)dosing of the leveler shifts the suppression too far towards the via bottom (see Figure 2c).

Appropriate pulse, especially pulse reverse current profiles can improve the via filling significantly. Thereby, the pronounced dissolution rates at the high current density areas at the via entrances during the anodic pulse are utilized to improve the “bottom-up” fill. The optimal pulse parameters depend on via geometry and electrolyte composition.

In all experiments described within this paper DC current profiles were used, whereby the plating current was increased stepwise during the plating process with the ongoing filling process.

a)



b)

c)

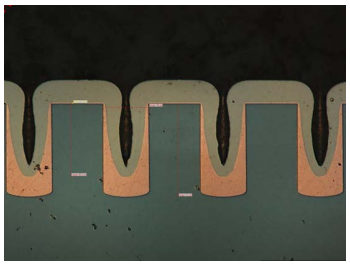


Figure 2: Microsection showing partially filled 35 µm x 70 µm via holes. A Spherolyte Cu200 additive system based copper electrolyte was used; the plating current profile was similar in all experiments. The concentration of the leveler component was increased from a) 0 ml/l and b) 5 ml/l to c) 10 ml/l. (Ni is plated on top of the Cu for preparation reasons)

ECD with CVD Copper Seed Layer

In the following examples of Cu via filling on CVD copper seed layer for different via sizes (see Table 1) are shown. For the 4 µm-vias (Figure 3a) bottom voids were observed, probably due to discontinuities in the seed layer on the via bottom. This effect is basically not typical and can by avoid by process optimization for small sized vias. The via test samples carried different via sizes which results in not optimized process conditions for the seed layer deposition. The upper 39 µm of the vias are successfully filled.

The 8 µm-vias (Figure 3b) are completely filled but show some seam voids which indicates that the additive composition of the electrolyte in this case is not optimal as its adjustment depends on the via dimensions.

The 18 µm and 35 µm-vias (Figure 3c - d) were filled void free, whereby the 35 µm-vias were filled only up to ~85 %, after 150 minutes. But the copper profile indicates that further plating would continue filling successfully. This process is time limited. For a complete via filling of 35 µm

via /77 µm depth a plating time of around 165 minutes is required for the used chemistry.

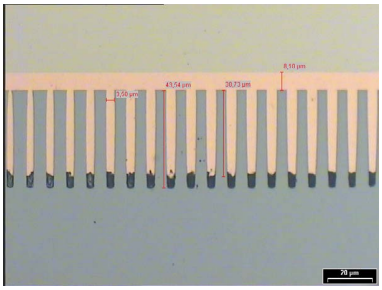


Figure 3a: 4 µm with Cu CVD

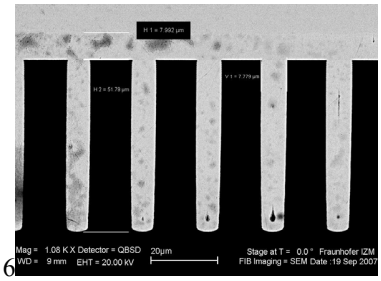


Figure 3b: 8 µm with Cu CVD

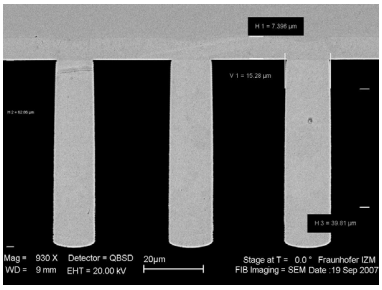


Figure 3c: 18 µm with Cu CVD

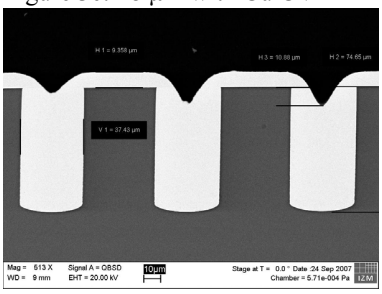


Figure 3d: 35 µm /77 µm with Cu CVD

Figure 3a-d:Via filling of different sizes with Cu-CVD seed layer

ECD with CVD Tungsten Seed Layer

In the following cross sections (Figure 4a – d) of vias filled with ECD Cu on CVD tungsten seed layer the filling process started in principle for all via diameters at the via bottom. However, for the smallest via diameter (Figure 4a) a relevant number of vias was found which have been filled only partially. The defects though look atypical as one finds vias, which have almost not been filled at all; others are filled at the bottom but not in the middle. Further a quite rough Cu film on the upper surface of the wafer was found. All these elements indicate that the pre-treatment of the tungsten seed layer for Cu ECD is critical and not suited to activate the surface to a sufficient extent for starting the Cu deposition everywhere at the same time. This applies especially for small via diameters. Basically the pre-treatment of tungsten seed layer for Cu deposition is crucial. So an additional Cu layers was deposited using the standard TW/Cu sputter process. These results are discussed later on in this paper.

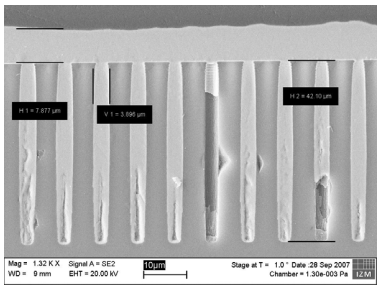


Figure 4a: 4 µm with W CVD

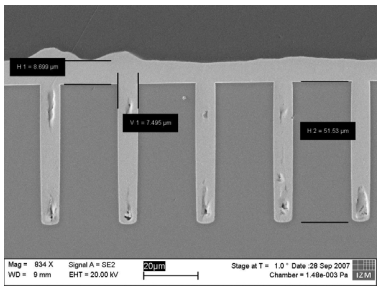


Figure 4b: 8µm with W CVD

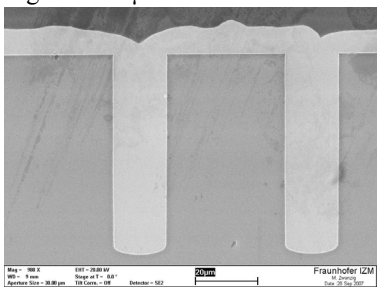


Figure 4c: 18 µm with W CVD

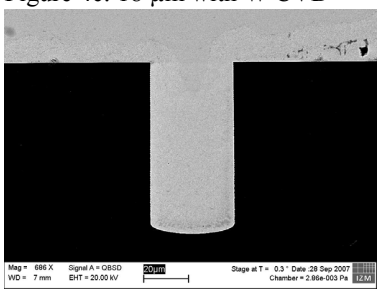


Figure 4d: 35 µm with W CVD

ECD with sputtered TiW / Cu Seed Layer

The chosen sputtered seed layer TiW/Cu based on the proven concept of the sequential sputtering of TiW (200 nm) and Cu (500 nm) is used as a seed layer for ECD micro-

bumping process as well. This layer provides good adhesion and barrier properties. Based on the sputtering principle and equipment, the process is limited to a certain via size and aspect ratio. For small via sizes Cu will not be deposited on the via bottom. So increasing via filling depth from 20 µm for 4µm vias to around 38 µm for 8 µm and complete filling of 65 µm depth via with a diameter of 18 µm (see Figure 5a – d) were found.

The filling of 18 µm and 35 µm-vias (Figure 5e– f) is almost perfect. Longer deposition time in Figure 5f would lead to a complete filling. It can be deduced that the sputter process does not yield a good enough seed layer in the bottom region of extreme high aspect ratio vias. So our standard TiW/Cu plating base is well suited as seed layer for the ECD Cu via filling for via diameters larger than 18 µm (depth about 70 µm) or an aspect ratio smaller than 4 (see Figure 6). Further investigations will be performed to identify the maximum aspect ratio for 18 µm via sizes. It is expected to achieve a ASR of > 6. Figure 6 summarizes the Cu-ECD filling degree vs. via size.

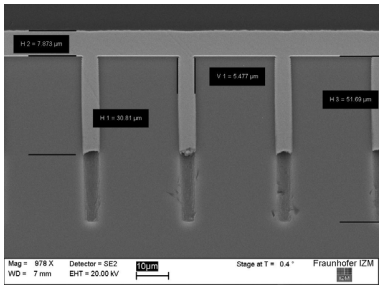


Figure 5a: 4 µm via size

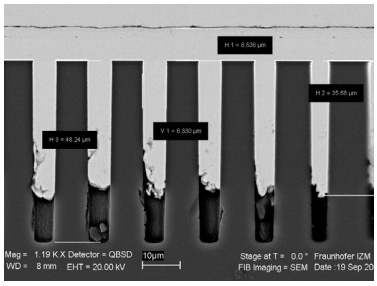


Figure 5b: 6 µm via size

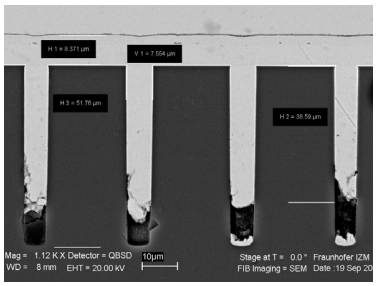


Figure 5c: 8 µm via size

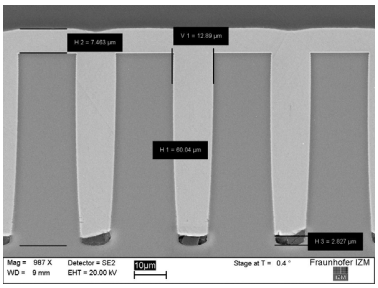


Figure 5d: 12 µm via size

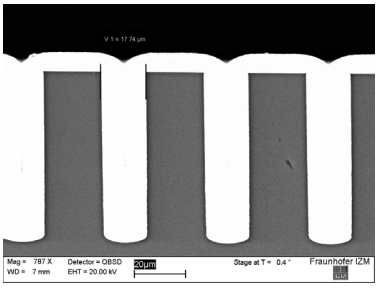


Figure 5e: 18 µm via size

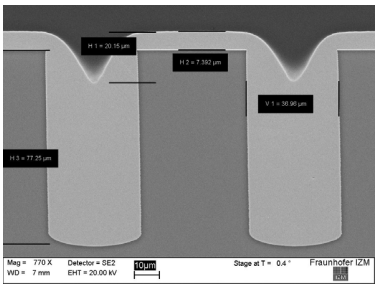


Figure 5f: 35 µm via size

Figure 5: Cu ECD Via Filling with sputt. TiW/Cu seed layer

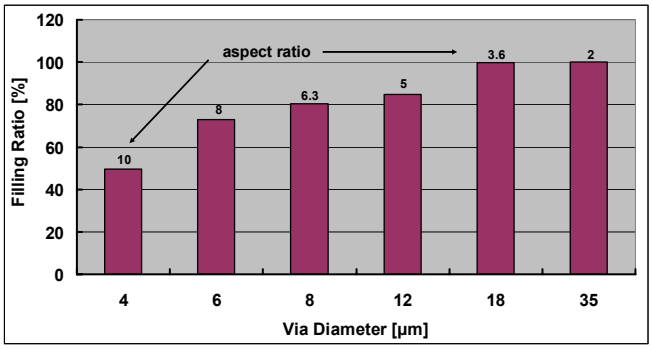


Figure 6: Via filling ratio in dependence of via diameter and via depth (aspect ratio) for sputtered TiW/Cu seed layer

ECD with CVD Tungsten and sputtered TiW/Cu Seed Layer

As on the CVD tungsten layer an inhomogeneous starting behaviour of the Cu electrolyte was observed although the via filling was good in principle, it was proceeded as follows.

To improve the starting behaviour of the CVD tungsten seed layer, a sputtered TiW/Cu seed layer was superimposed. Figure 7a – c show for via diameters from 5 µm to 20 µm and via depth from 58 µm to 94µm, respectively, the best filling results for small and larger via diameter of the investigated seed layers. So this seed layer combination avoids the filling gap (bottom voids) of small via size with only sputtered TiW/Cu seed layer. Figure 8 shows a detail of a via bottom of a 20 µm via filling.

Figure 9 summarizes the via filling results for the different seed layers. Cu-ECD with CVD seed layers show good filling also for small via sizes up to 4 µm. A filling degree of close to 100 % could be achieved. This is influenced by process conditions for the bottom seed layer deposition (Cu-CVD) as well as by the wetting pre-condition of the tungsten seed layer.

With sputtered seed layers for small via sizes only a 50% filling could be achieved which corresponds for 4 µm via diameter to a depth of around 39 µm.

For the combined seed layer process (CVD W + sputt. TiW/Cu) a filling degree of 100 % could be achieved for all via sizes. The via depth in the test trials is considerably larger (58 to 94 µm) than for the other samples at comparable via diameters.

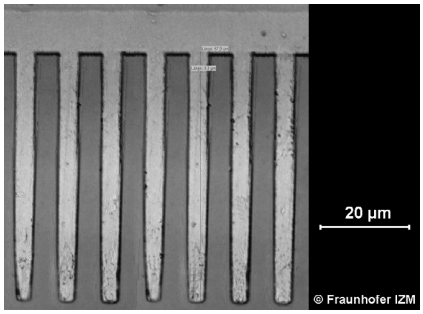


Figure 7a: 5 µm with therm. Ox., CVD W; sputt. TiWN/Cu

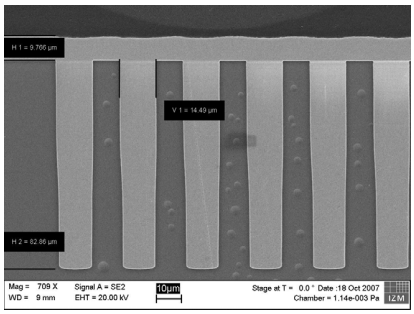


Figure 7b: 15 µm (83 µm) with CVD W; sputt. TiWN/Cu

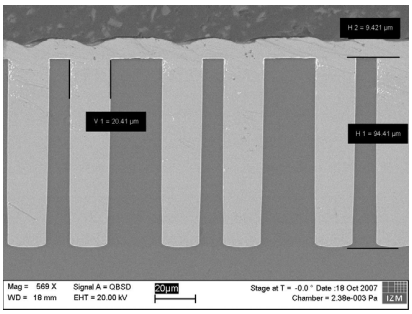


Figure 7c: 20 µm via size. (94 depth)(CVD-W+sputt. TIW/Cu

Figure 7: best filling results for small and larger via diameter of the investigated seed layers

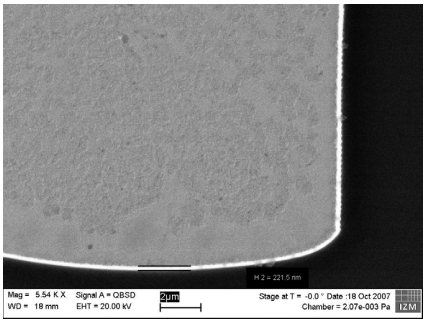


Figure 8: cross section of bottom of a 20µm via

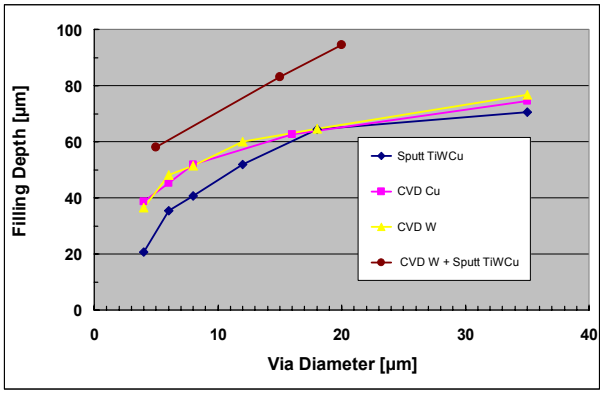


Figure 9: Filling depth in function of via diameter and different seed layers

Modelling and Simulation

To give a forecast about thermo-mechanical stress and first reliability estimations Finite Element (FE) simulations have been performed. Materials were characterized in their elasto-plastic mechanical properties by nano-indentation and successive parameter extraction by FE-simulation [7]. These properties are needed to evaluate a possible damage behaviour during processing, assembly (soldering) and successive thermal cycling for later use within the framework of e.g. a Coffin-Manson damage model [8]. Hereby, a calculated physical quantity to describe inelastic mechanical deformation would be used, as e.g. a dissipated energy or plastic strain [9]. For a parametric simulation, a 2D FE-model of rotational symmetry has been created which allows quick alteration of geometrical, material- or process-related

parameters for the through silicon via (TSV) as depicted in figure 10.

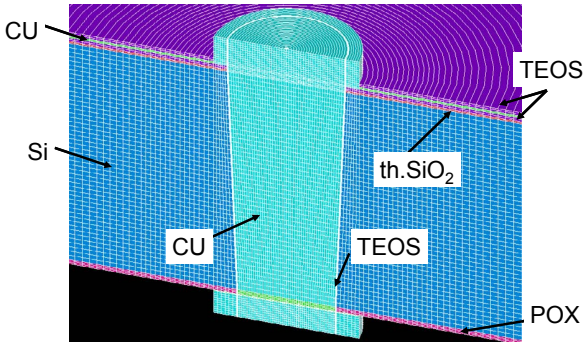


Figure 10: 2D FE Model of TSV (rotational symmetry)

The model has been created in a fashion that allows successive addition or subtraction of elements in order to simulate the individual process steps like addition of an oxide layer or etching of a via. The elements are then brought to life at the respective process temperature to get the correct thermal strain.

For material data used for the simulations please refer to [7] or [2]. As material properties are assumed to be time-independent for the temperatures involved, the simulation is tracked by steps only. The process steps are followed by three solder reflows and three thermal cycles in order to check their influence of stress or plastic strain. Then, the following parameters have been used in the simulation for parametric runs (Table 2):

Configuration	Abbreviation	A: Si Thickness	B: Oxide Dep. Temp
Standard Base Variant	Std	d = 50 µm Si	T = 400 °C (CVD)
Thick Silicon	Tck	d = 150 µm Si	T = 400 °C (CVD)
Low Temperature	LoT	d = 50 µm Si	T = 250 °C (Poly)

Table 2: text matrix with varied parameters A and B

The idea is to check for different geometry (thicker chip) and different oxide deposition processes which differ in temperature.

After FE runs, some regions of interest could be identified. From Figure 11, where plastic strain and stress are given (as possible failure criterion) for two load steps, it is instructive to look at the top, the centre and the bottom of the via. This is analogous to the results found for a tungsten filled TSV as described earlier in [2].

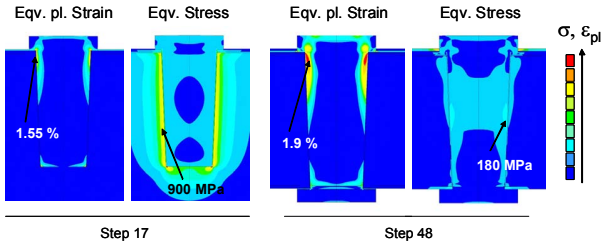


Figure11: Situation after load step 17 (TSV filling, maximum stress) and 48 (thermal cycling, maximum strain) for the base variant

As can be observed, the maximum plastic strain evolves near the top of the via during processing, climbes up to a constant value after thermal cycling not to accumulate any more from that point on. Maximum stresses in the copper stay near the yield stress of 180 MPa in the centre of the TSV. This is in accordance with the expected large CTE mismatch between the silicon and the copper. The maximum non-singular stress is found in the adjacent silicon, whereas the stress maximum at the top of the via is an artefact (stress singularity at corner).

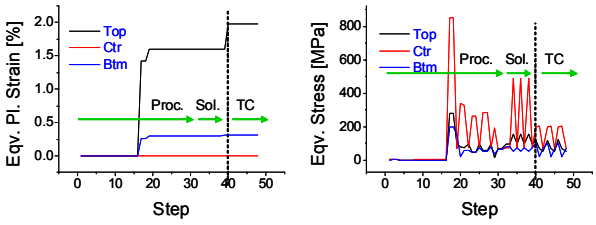


Figure 12: Equivalent accumulated plastic strain and stress at different locations of the via during processing (Proc.), three reflows (Sol) and thermal cycling (TC within T = -40..125 °C) for base variant

As can be seen from Figure 12, the plastic strain does not accumulate during thermal cycling. This means that some large plastic deformation induced damage is not to be expected, which should prolongue via lifetime. Hightest nonsingular values of stress, however, are recorded in the silicon adjacent to the TSV due to a very high compressive force after filling of the TSV and heating up (step 17). This could be harmful during processing. Soldering and thermal cycling do not cause again any comparable loading on the silicon. In Figure 13 the results of the parameter study with respect to processing conditions and geometry can be seen.

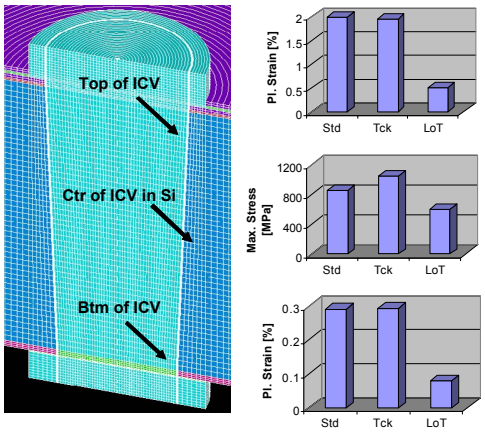


Figure 13: Resulting maximum values as obtained by parametric study. Strains are given after thermal cycling, stresses are given after via filling for the base variant, the thick silicon and the low-T process

So simulation indicates a strong dependence on process temperature, whereas reflow soldering and thermal cycling are less important for both, stress and strain. Their value can be decreased at the important locations by a low temperature process, which is in such a respect advantageous. The thickness of the via has no significant influence on the strains at the top and bottom of the via as this is a local effect.

Conclusions

A TSV low cost process can be realized if a low cost via filling process is on hand. Electrochemical deposition of copper is one of the preferred candidates to perform cost efficient via filling for different via sizes in a typical range of larger than 4 µm until 35 µm diameter. Four different seed layers: CVD-Cu, CVD-W, sputtered TiW/Cu, CVD-W / sputtered TiW/Cu were evaluated and compared in terms on via filling characteristics.

Using an optimized electrolyte for Cu electrodeposition and TiW/Cu seed layer shows that vias exceeding 18 µm diameter can be filled up to a depth in the range of 70 µm. Small via sizes (e.g. 4 µm) can only be filled until a depth of around 20 µm using a sputtered seed layer. To achieve a higher filling ratio for smaller via diameters CVD seed layers have to employed. Depending on the established process infrastructure a combined CVD and sputtering process such as CVD-W and sputtered TiW/Cu can be a good alternative process to fulfill the requirements of via filling in the requested range from 4 µm to 35 µm diameter and via depths until 94 µm which fits into most applications.

To evaluate the stress and strain fields during processing, assembly and thermal cycling FE-simulations have been carried out. It was found that process temperature has a significant effect on stresses in the silicon at the centre of the via which could be harmful in terms of damage. In this respect, using not a CVD oxide process but a low temperature polymer dielectric would reduce stress in the silicon. As the plastic strain does not accumulate during thermal cycling, a long lifetime could be expected during operation. However, to extend the given scheme for obtaining a statement about damage and lifetime, some experimental data is needed for comparison.

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