Design of a High Performance CMOS Operational Amplifier Using DTMOS Technique

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Abstract—In this paper a high performance CMOS operational amplifier (op amp) using dynamic threshold voltage MOSFET (DTMOS) technique is presented. A two stage operational amplifier is designed and simulated using 0.18 µm CMOS technology. The performed simulation results show an input-referred noise of 490.82 nV/√Hz at 100 Hz, and a power consumption of 38.53 µW under 5 pF loads. The dc open loop gain is 96.15 dB, a phase margin of 59.2° and a unity gain-bandwidth (UGB) of 28.18 MHz while operating at 1 V supply voltage. The Op Amp has a CMRR of 153.9 dB and PSRR of 107.1 dB.

Keywords-CMOS; Operational amplifier; op amp; DTMOS; Low-voltage low-power.

I. INTRODUCTION

In the past few years with the rapid growth of market for portable devices such as cell phones, portable computers and medical electronic implant devices, design of analog integrated circuits at low-voltages with high performance has become an extremely important issue. Reduction of threshold voltage is necessary for low voltage operation, so various techniques have been proposed for low-voltage low-power analog integrated circuits design.

A MOSFET can be operated at a lower voltage by forward biasing the source-bulk junction (forward body-bias). This approach has been used to design a low-voltage low-power CMOS operational amplifier, but with increasing forward body-bias, the leakage current increases significantly. The DTMOS technique in 1994 (Assaderaghi et al, 1994) is proposed to overcome the drawback in a forward-biased MOSFET [1]-[3]. This technique can be used in connection with the back-gate forward-bias technique in designing low-voltage low-power analog, digital and mixed signal CMOS integrated circuits.

Several papers have been focused on design of CMOS operational amplifier and operational transconductance amplifier (OTA) based on DTMOS technique. In [4]-[7] the authors presented a novel class AB op amp for low-voltage (1 V) applications. In [8] the authors proposed an ultra-low-voltage ultra-low-power operational transconductance for biomedical applications. In [9] the authors presented a 0.8 V class-AB linear OTA for high-frequency applications. In [10] a novel input stage for low-voltage low-power and low-noise operational amplifier has been described.

The organization of this paper is as follows. In Section II, the DTMOS technique is presented. The structure of proposed op amp is described in Section III. The simulations results are provided in Section IV and finally the conclusion is given.

II. DTMOS TECHNIQUE

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low-voltage is the threshold voltage. DTMOS technique is the best idea for reduction threshold voltage. In DTMOS technique, the bulk is tied to its own gate as shown in Fig. 1.

![Dynamic threshold MOSFET device](image)

The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{th}$) according to below equation [12]:

$$V_{th} = V_{th0} + \lambda \left( \sqrt{2\varphi_f - V_{BS}} - \sqrt{2\varphi_f} \right)$$

(1)

Where $V_{BS}$ is the source-bulk voltage, $V_{th0}$ the threshold voltage for $V_{BS} = 0$. $\lambda$ is body effect factor with an
approximate value between 0.3 to 0.4 $\sqrt{V}$, and $\varphi_f$ is Fermi potential with a typical value in the range of 0.3-0.4 V [12].

III. DESIGN LOW-VOLTAGE LOW-POWER OP AMP

Fig. 2 shows the schematic of a two stage low-voltage operational amplifier based on DTMOS technique.

![Schematic of the proposed DTMOS op amp circuit.](image)

This structure combines a fully differential pair with a current source load and a differential pair with a current mirror load. We used DTMOS transistors pairs (M1, M2 M5 and M6) in both differential pair. The active current source M3 and M4 can source the maximum current for the input pair to reduce thermal noise. The current mirror M7 and M8 combine with the transconductance of the input pair to define the DC gain. A cascode stage, M5 and M6 can increase the bandwidth and gain of the amplifier. The common source configuration is chosen for the output stage of the operational amplifier. Such a stage can provide about 20-30 dB of gain. A Miller compensation scheme is chosen to achieve desirable phase margin.

A. DC Gain

The small-signal DC gain of the proposed op amp is given by:

$$A_v = (g_{m2} + g_{mb2}) \ast \ldots \ast \left(\frac{g_{m6} + g_{mb6}}{r_{o6}(r_{o2} || r_{o6})} \parallel r_{o6} \right) \ast \ldots \ast \left(\frac{g_{m5}r_{o5} \parallel r_{o10}}{g_{ms}}\right) \ast \ldots \ast (2)$$

While the transconductance $g_{mb}$ can be calculated as given in (3), [12]:

$$g_{mb} = \frac{\lambda}{2 \sqrt{2p_f + V_{sb}}} g_m = \eta g_m \tag{3}$$

The transconductance $g_{mb}$ varies from 20% to 30% of $g_m$ for the same transistor in a CMOS process [8].

B. AC Analysis

Small-signal analysis of the circuit in Fig. 2, results in the following equation (ignoring some smaller parameters such as $C_1$ and $C_2$):

$$V_{out} = \ldots = \left(\frac{g_{m2} + g_{mb2}}{g_{m9}}\right)g_{m9}R_2R_3C_c - s(g_{m2}R_2R_3C_c \left(1 - g_{m9}C_c\right))$$

$$\frac{1}{1 + sR_cC_c + R_3C_c + g_{m9}R_2R_3C_c + s^2R_3C_cC_3} \tag{4}$$

Where

$$C_1 = C_{gd2} + C_{gd2} + C_{gd4} + C_{gd4} + C_{gd6} + C_{gd6} \tag{5}$$

$$C_2 = C_{gd6} + C_{gd6} + C_{gd8} + C_{gd8} + C_{gd9} + C_{gd9} \tag{6}$$

$$C_3 = C_{load} + C_{gd9} + C_{gd10} + C_{gd10}$$

$$R_1 = r_{o2} || r_{o4} \tag{7}$$

$$R_2 = r_{o8} \parallel \left[r_{o6}(1 + (g_{m6} + g_{mb6})(r_{o2} || r_{o4}))\right] \tag{8}$$

$$R_3 = r_{o9} \parallel r_{o10} \tag{9}$$

$C_c$ and $R_c$ are the compensation capacitor and zero-nulling resistor respectively.

With the supposition that the second pole is far larger than the dominant pole, the dominant pole of equation (4) can be approximated by:

$$P_1 \approx -\frac{1}{g_{m9}R_2R_3C_c} \tag{10}$$

and the second dominant pole is:

$$P_2 \approx -\frac{g_{m9}R_2}{R_cC_c} \tag{11}$$

Also the zero is:

$$Z = \frac{g_{m9}}{(1 - g_{m9}R_c)C_c} \tag{12}$$

For unity gain-bandwidth stability, the magnitude of the second dominant pole should be greater than the UGB, therefore:

$$C_c > \left(\frac{g_{m2} + g_{mb2}}{g_{m9}R_2}\right)R_cC_3 \tag{13}$$

According to Equations (7) and (8), we can find that $R_c$ can control the zero and second dominant pole positions and therefore change the phase margin. If $R_c$ is chosen close to $1/g_{m9}$, then $P_2$ is maximized and stability is achieved with a minimum $C_c$.

C. Noise analysis

The input-referred noise (includes thermal noise and flicker noise) of the proposed op amp is described as:

$$V_n^2(f) = \frac{2}{C_{ox}}\left[\frac{K_{fn}}{W_2L_2f} + \frac{4KT_\gamma}{g_{m4} + g_{m6} + g_{mb2}} \right] + \ldots \left[\frac{K_{fp}}{W_4L_4f} + \frac{4KT_\gamma}{g_{m4} + g_{m6} + g_{mb2}} \right] + \ldots \left[\frac{K_{fp}}{W_6L_6f} + \frac{4KT_\gamma}{g_{m8} + g_{m6} + g_{mb2}} \right] + \ldots \left[\frac{K_{fp}}{W_8L_8f} + \frac{4KT_\gamma}{g_{m8} + g_{m6} + g_{mb2}} \right] \tag{14}$$

Where $C_{ox}$ is capacitance per unit area of the gate oxide, $W$ and $L$ are the channel width and length respectively, $K_{fn}$ is NMOS flicker noise coefficient, $K_{fp}$ is PMOS flicker noise coefficient, $k$ is the Boltzmann constant and $T$ is the absolute temperature. The derived coefficient $\gamma$ is equal 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFETs. It also varies to some extent with the drain-source voltage [12]. The noise contribution of cascode stage M5, M6, output stage M9, M10 and current bias transistor M0 is negligible.

IV. SIMULATION RESULTS

The proposed op amp has been simulated with HSPICE in a 0.18 $\mu$m CMOS standard technology under 5pF load.
The simulated AC results and noise performance are shown in Fig. 3 and Fig. 4, respectively. These Figures show the DC gain of the design is 96.15 dB with unity gain-bandwidth up to 28.18 MHz. The phase margin is 59.2°. The input-referred noise is 490.82 nV/√Hz at 100 Hz and 11.36 nV/√Hz at 1 MHz.

Table I shows a comparison with other low-voltage operational amplifiers. To evaluate this work a figure of merit (FoM) is defined as [8]:

$$\text{FoM} = \frac{\text{Gain} \times \text{UGB}}{\text{Power supply} \times \text{Power consumption}}$$  \hspace{1cm} (11)

V. CONCLUSION

A new 1 V low-voltage low-power CMOS operational amplifier was proposed in this paper. The proposed op amp utilizes DTMOS technique. The simulation results show that the DC gain of the presented amplifier is equal to 96.15 dB while achieving unity gain bandwidth of 28.18 MHz and phase margin 59.2°. The total power consumption of the op amp is 38.53 µW. Also this op amp has a CMRR of 153.9 dB and PSRR of 107.1 dB. The designed op amp is robust against temperature and voltage supply variation.

REFERENCES


TABLE I. COMPARISON BETWEEN OPERATIONAL AMPLIFIER

<table>
<thead>
<tr>
<th></th>
<th>Proposed op amp</th>
<th>[5]</th>
<th>[8]</th>
<th>[13]</th>
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<tr>
<td>Technology (µm)</td>
<td>0.18</td>
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<td>Gain (dB)</td>
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<td>Phase margin</td>
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<td>62°</td>
<td>66°</td>
<td>45°</td>
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<td>UGB (MHz)</td>
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<td>2.73</td>
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<td>CMRR (dB)</td>
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<td>PSRR (dB)</td>
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<td>N/A</td>
<td>88 @ 10 kHz</td>
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<tr>
<td>Slew Rate (V/µs)</td>
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<td>Output voltage swing (V)</td>
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<td>0.8</td>
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<td>Input-referred noise (nV/√Hz)</td>
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<td>10 @ 10 mHz</td>
<td>408 @ 10 kHz</td>
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<td>5</td>
<td>5, 10 kΩ</td>
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<td>20</td>
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<td>FOM (dB MHz/V.µW)</td>
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