A 3μW Fully-Differential RF Envelope Detector for Ultra-Low Power Receivers


* ULP Wireless, Holst Centre imec, Eindhoven, The Netherlands
** Mixed-signal Microelectronics, Faculty of Electrical Engineering, Eindhoven University of Technology, The Netherlands

Abstract—A fully differential envelope detector (ED) operating at 2.4GHz is designed in 90nm CMOS technology. The new design uses the common-gate topology to deal with large common-mode input signals through first-order current cancellation. Thereby, a fully differential ultra-low power super-regenerative front-end is enabled. It has a measured output voltage swing of 2.8-127mV and achieves 19.6dB output SNR at sensitivity input level. The circuit consumes 3μW from a 1.2V power supply.

I. INTRODUCTION

Wireless body area networks (WBANs) are networks used for communication among sensor nodes operating on, in or around the body. WBANs enable monitoring of vital body parameters and movements. The key characteristic of WBAN sensors is their autonomous operation. For true energy autonomy, the total power consumption of a sensor should be minimized. The low complexity of super-regenerative (SR) receivers using on-off keying (OOK) modulation enables ultra-low power consumption [1].

Fig. 1(a) shows a super-regenerative RF front-end architecture [1]. The receiver operates in the 2.4GHz ISM band and achieves a data rate of 5Mbps at a sensitivity of -75dBm. It consists of a low-noise amplifier (LNA), a voltage-controlled oscillator (VCO), a differential to single-ended converter (DSC) and a single-ended envelope detector (ED).

The VCO bias current is periodically quenched at baseband frequency, i.e. 5MHz, to achieve maximum sensitivity and selectivity. Due to the quenching, a low frequency common-mode (CM) signal is generated. Fig. 2 illustrates the oscillator output signals. The CM signal is up to 50mV in amplitude, while the RF amplitude ranges between 25-200mV. When insufficiently suppressed, the CM signal may transfer to the ED output and the baseband information can be lost.

To avoid this problem, the DSC in Fig. 1(a) suppresses the common-mode signal, but at the cost of unnecessary power consumption. Furthermore, the advantages of a differential chain, i.e. better noise rejection and distortion performance, are lost. A fully differential ED is desired, so that the converter can be omitted from the receiver chain, as shown in Fig 1(b).

This paper presents a novel fully differential ED, which suppresses the undesired low frequency common-mode inputs through filtering and first-order current cancellation. Hereby, the front-end power consumption can be decreased and a fully differential receiver chain can be realized.

The organization of this paper is as follows. Section II explores envelope detector topologies and presents the proposed circuit. Section III presents simulation and measurement results. Finally, conclusions are drawn in section IV.

II. ENVELOPE DETECTOR TOPOLOGIES

A. Prior-art: (partly) single-ended circuits

Fig. 3 shows two (partly) single-ended envelope detector topologies. Both circuits exploit the exponential transfer which the MOS transistor exhibits when biased in weak inversion, in combination with a low-pass filter to obtain the baseband information from the RF carrier.
The circuit in Fig. 3(a) is the widely used, conventional single-ended common drain ED [2,3]. A replica circuit may be added to produce a DC-reference to obtain a pseudo-differential output. Similarly, a single-ended envelope detector using the common source topology has also been reported [4]. The circuit in Fig. 3(b) has a differential input, but does not provide a differential output [2]. Due to the squaring nature of the transfer function, both positive and negative RF inputs realize equal output amplitude.

In any of these circuits, signal components below the cut-off frequency of the output low-pass filter experience the linear (first-order) transfer. In other words, the circuit does not act as a rectifier for these frequencies, but rather as a regular amplifier. For this reason, the low frequency quenching input would transfer directly to the baseband output.

B. Proposed common gate differential circuit

Fig. 4 shows the proposed circuit. The nonlinear I-V characteristics of NMOS transistors N1,2 and PMOS transistors P1,2 are used to down-convert the RF signal to baseband. A low-pass filter, formed by C2 and R2 with cut-off frequency $f_{LPF}$, is placed on each output node to filter out high-frequency components produced by the nonlinear transfer function of the transistors. At each input node, AC coupling capacitor $C_{CP}$ and the input impedance of the NMOS and PMOS transistors form a high-pass filter (HPF) to suppress low frequency input signals below cut-off frequency $f_{HPF}$, thereby rejecting CM input signals arising from the quenched operation.

The current reference circuit in Fig. 4 is constructed by stacking two transistors B1 and B2 that form current mirrors with N1,2 and P1,2, thus fixing the DC voltages on their gate and source nodes, such that $I_Q = I_{REF}$.

The pair of NMOS transistors N1,2 is biased in weak inversion. The common gate topology is used, i.e. the signal is applied to the source node and the output is taken from the drain nodes. For simplicity we assume here that the common-mode $v_{cm}$ is zero. The drain current equation for N1 is given by [6]

$$I_{d,N1} = I_Q e^{v_c/V_T} \left( e^{v_c/V_T} - 1 \right) - e^{v_n/V_T} \rightarrow I_Q e^{v_c/V_T}, \quad (1)$$

where $I_Q$ denotes the quiescent current, $V_T$ the thermal voltage ($kT/q$) and $V_n$ the threshold voltage and $n$ corrects the slope of the transfer function for losses due to capacitive division.

In contrast to (1), both common drain and common source topologies would produce a small-signal current given by

$$I_d = I_Q e^{v_c/V_T}. \quad (2)$$

Comparing (1) and (2), the advantage of the common gate topology becomes clear. If inputs are applied to the source node, no capacitive division with the gate oxide capacitance occurs. As a result, $n$ is not present in the small-signal current. Modern processes typically have $n > 1.5$. As a result, common source and drain topologies achieve less efficient nonlinear transfer.

A proposed common gate differential circuit

In Fig. 4, the relatively low input impedance of the transistor linear trans $R \rightarrow 1Ω$-selected is on each output node to filter out high-frequency components produced by the nonlinear transfer function of the transistors. At each input node, AC coupling capacitor $C_{CP}$ and the input impedance of the NMOS and PMOS transistors form a high-pass filter (HPF) to suppress low frequency input signals below cut-off frequency $f_{HPF}$, thereby rejecting CM input signals arising from the quenched operation.

The current reference circuit in Fig. 4 is constructed by stacking two transistors B1 and B2 that form current mirrors with N1,2 and P1,2, thus fixing the DC voltages on their gate and source nodes, such that $I_Q = I_{REF}$.

The pair of NMOS transistors N1,2 is biased in weak inversion. The common gate topology is used, i.e. the signal is applied to the source node and the output is taken from the drain nodes. For simplicity we assume here that the common-mode $v_{cm}$ is zero. The drain current equation for N1 is given by [6]

$$I_{d,N1} = I_Q e^{v_c/V_T} \left( e^{v_c/V_T} - 1 \right) - e^{v_n/V_T} \rightarrow I_Q e^{v_c/V_T}, \quad (1)$$

where $I_Q$ denotes the quiescent current, $V_T$ the thermal voltage ($kT/q$) and $V_n$ the threshold voltage and $n$ corrects the slope of the transfer function for losses due to capacitive division.

In contrast to (1), both common drain and common source topologies would produce a small-signal current given by

$$I_d = I_Q e^{v_c/V_T}. \quad (2)$$

Comparing (1) and (2), the advantage of the common gate topology becomes clear. If inputs are applied to the source node, no capacitive division with the gate oxide capacitance occurs. As a result, $n$ is not present in the small-signal current. Modern processes typically have $n > 1.5$. As a result, common source and drain topologies achieve less efficient nonlinear transfer.

A similar analysis can be done for the PMOS transistor. In this case, a positive voltage drop occurs with respect to the bias point.

![Figure 4. The schematic of the proposed fully differential common gate ED.](image-url)
The resulting differential output voltage amplitude is then given by
\[ v_{od} = v_0^+ - v_0^- = \frac{I_Q R_L A^2}{4 V_T^2}, \] (5)
so that the output voltage directly relates to the RF input amplitude \( A \) and thus the OOK modulated baseband data.

C. Envelope detector conversion gain

An important property for EDs is the conversion gain, which represents the down-conversion efficiency through the gain from RF to baseband frequencies. Using (5) as a starting point, correction constants are used to model three important effects, which have to be taken into account during design:

- \( a_{od} \) corrects for model mismatch related to the assumption that the transconductance \( g_m \) in weak inversion is asymptotic, i.e. \( g_m = I_Q V_T \), while this is not necessarily true near true inversion [6].
- \( a_C \) denotes the losses due to capacitive division between the coupling capacitance and parasitics at the source node, i.e. \( a_C = C_{CP} / (C_{CP} + C_{PD}) \).
- \( a_L \) denotes the resistive division of \( R_L \) with the parallel output impedance of the MOS transistor, \( 1/g_{ds} \), and the input impedance of the baseband stages, \( R_{BB} \).

Using (5), the conversion gain for the proposed ED is
\[ k_{\text{conv}}(A) = \frac{|v_{od}|}{|v_{id}|} \bigg|_{f = f_{FB}} = \frac{|v_{od}|}{A} = \frac{I_Q a_L R_L a_C^2 A}{4 V_T^2}, \] (6)
where \( f_{FB} \) denotes the baseband frequency of the OOK modulated input signal.

\( V_T \) and \( A \) can not be influenced by ED circuit design, so the maximum achievable conversion gain is limited by \( I_Q \) and \( R_L \). Since the transistors operate in weak inversion, the drain-source voltage must remain larger than \( 3V_T \) for channel saturation [6]. Kirchhoff’s voltage law dictates a constraint for the voltage headroom between \( V_{DD} \) and moderate inversion, given by
\[ V_{DD} - |v_{id}| / 2 - 2V_{DSatmin} / 2 = -2V_D / 2 - k_{\text{conv}} |v_{id}| = 0. \] (7)

Adding the compensation constants \( a_{od}, a_C \) and \( a_L \) to (7), the limitation posed on the maximum value of the voltage across the load resistance \( V_D = I_Q R_L \) is derived as
\[ \left( I_Q R_L \right)_{\text{max}} = \frac{V_{DD} - \alpha_C |v_{id}|_{\text{max}} / 2 + 6V_T}{4 + \alpha_{od} a_C a_L^2 |v_{id}|_{\text{max}}^2 / 4 V_T^2}, \] (8)
predicting that large \( |v_{id}| \) or large \( I_Q R_L \) results in compression of the conversion gain. During design a maximum input amplitude of 200mV was assumed. In order to achieve the highest gain while operating as much in weak inversion as possible, we selected \( I_Q = 850\text{nA} \) and \( R_L = 180\text{k}\Omega \). According to (7), the resulting \( |v_{id}|_{\text{max}} \approx 170\text{mV} \), so compression is expected at input amplitudes above this maximum.

D. Low frequency common mode suppression

When the ED is used in a fully-differential chain of a ultra-low power receiver, e.g. a super regenerative receiver [1], low-frequency common-mode inputs need to be suppressed.

As can be seen from (3), the first-order currents cause most problems. Any low-frequency input is not filtered by the output filter and transfers directly to the output nodes. However, the first-order currents in each transistor branch flow in the opposite direction. The resulting voltages are ideally equal and have 180 degree phase difference. In other words, the resulting output signal should not contain any differential component.

In practice, the NMOS and PMOS transistors need unequal sizes to produce equal \( g_m \). As a result, a differential mode output results from the common mode input, which impedes with the baseband signal. Simulation shows that first-order current cancellation achieves around 17dB common-mode to differential-mode suppression, which is insufficient. For further CM suppression, a high-pass filter on each separate input node (Fig. 4) filters the unwanted signal with cut-off frequency
\[ f_{HPF}^{-1} = \frac{1}{2\pi C_{CP} \left| Z_{in}\right|} = \frac{1}{2\pi C_{CP} (1/g_{mN} / / 1 / g_{mP})}. \] (9)

This first-order high-pass filter is designed to suppress the 5MHz common-mode signal by another 30dB before the signal enters the ED circuit, effectively solving the CM problems.

Table I summarizes the final component values used.

<table>
<thead>
<tr>
<th>TABLE I. FINAL COMPONENT VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Components</strong></td>
</tr>
<tr>
<td>P1,P2,B1</td>
</tr>
<tr>
<td>N1,N2,B2</td>
</tr>
<tr>
<td>R1, Raffect</td>
</tr>
<tr>
<td>C3, CCP, C5</td>
</tr>
</tbody>
</table>

III. IMPLEMENTATION RESULTS

The fully differential ED has been fabricated in a 90nm CMOS technology. In- and output buffers are included on the chip to model the reference system presented in Fig. 1(b) [1]. The chip photographs is shown in Fig. 5. The inset photograph shows the ED circuit only in a close-up. The circuit occupies 0.018 mm² of chip area, excluding buffers and bond-pads. The chip is bonded inside a QFN56 air-cavity package for testing. The packaged chip is placed on a custom designed FR4 PCB.
An off-chip reference current is generated so $I_D = 850\,\text{nA}$ within +/-5nA uncertainty. In simulation, this bias current setting has shown to provide the desired noise and gain performance. Also, $I_D$ is simulated to only vary with 7.9% for 20% PVT spread. The current reference is thus assumed robust.

### Measurement results

Fig. 6 shows calculated, simulated and measured conversion gain. The conversion gain is mapped on linearly scaled axes to clearly show that the gain increases linearly with input amplitude, as predicted by (6). However, the conversion gain is compressed above 135mV of amplitude. Since the final circuit uses relatively small-sized transistors which operate near moderate inversion, $V_{DS_{min}} = 3V_T$ is probably underestimated in (8) [6]. As a result, compression occurs at lower input amplitudes than predicted.

In OOK operation, the SNR at the ADC should be at least 12dB to achieve $10^{-3}$ BER. In ED-based receivers, the noise at baseband frequencies at the ED output can be attributed mainly to the ED transistors, where flicker noise is dominant. The noise mixed from RF to baseband frequencies is negligible [3].

The signal power levels and the noise power levels at the output of the circuit have been measured to determine the output SNR. Fig. 7 shows simulated and measured output SNR. The measured output SNR ranges from 19.6-53.0dB for an ED input amplitude range of 25-200mV, which is the VCO output amplitude range. Hence, $10^{-3}$ BER is achieved if baseband stages do not add over 7.6dB NF, which is trivial to achieve.

Finally, the measured common mode input to differential mode output suppression is 46.3dB. A 5MHz, 50mV amplitude common mode input results in 243μV at the ED output, which is 21dB below the 2.8mV minimal down-converted RF signal amplitude. Thus, the differential amplitude resulting from common-mode inputs is below the noise floor.

Table II summarizes the measured circuit specifications.

| Table II: Summarized Measured Circuit Specifications |
|-----------------------------------|-------|--------|
| **Circuit specifications at $I_D = 850\,\text{nA}$** | **Value** | **Unit** |
| Power consumption ($V_{DD}(I_{Nrz} + 2I_D)$) | 3.0 | μW |
| Differential output amplitude (min-max) | 2.8-127 | mV |
| Output SNR (min-max) | 19.6-53.0 | dB |
| Diff. output ampl. at max. (50mV) CM input ampl. | 243 | μV |
| Common-mode to differential mode suppression | 46.3 | dB |

**B. Comparisons with previous work**

One fully differential ED has been reported [5]. Here, both a current reference and several voltage references are required to fix the quiescent conditions. The common source topology is used, which we have previously shown to be less power efficient than the common gate topology. Unfortunately, gain and SNR performance is not specified for the ED. Furthermore, several mV of common-mode distortion are still perceivable.

Compared to a previous single-ended implementation [1], the proposed circuit has a similar conversion gain and output SNR performance. However, the ED power consumption is decreased by more than 50%, from 8.4μW to 3μW.

Finally, since the presented circuit is inherently differential, the DSC in the RF front-end from [1] can be omitted. This will save 20% on the 500μW total power budget published in [1].

**IV. CONCLUSIONS**

A fully differential common gate envelope detector has been designed in 90nm CMOS. The circuit is designed to operate in a fully differential 2.4GHz super-regenerative front-end.

The presented ED performs first-order current cancellation and uses a high-pass filter to suppress the unwanted common-mode signal present because of VCO quenching.

Since the presented ED is inherently differential, no DSC is required. In this way, up to 20% on the 500μW total front-end power budget may be saved. The circuit consumes only 3.0μW from a 1.2V supply. The SNR at the output of the envelope detector is measured to be 19.6dB for sensitivity input levels, so that $10^{-3}$ BER is easily achieved using OOK operation.

**REFERENCES**


