A LOW POWER REVERSIBLE BRAUN ARRAY MULTIPLIER ARCHITECTURE USING KTR GATE

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Abstract---The current digital era is more tempted towards the Reversible logic design because of its low power consumption. Multiplication is the basic building block for several DSP processors, Image processing etc. In Digital Signal Processors the computing complexities of algorithms used have been gradually increased. In order to achieve the high execution Speed, Parallel array Multipliers are used. A typical implementation of such an array multiplier is Braun Design. The proposed low power Reversible Braun array multiplier is designed using the full adder which can be implemented using the Proposed new KTR Gate. The Outputs are verified using the Verilog HDL Code in Modelsim Software.

Key words: Reversible Multiplier, Braun array, KTR gate.

1. Introduction

This section provides the reason and the definition of Reversible logic, and some key features of the proposed work.

1. a .Reversible Logic

It is well known that Moore's law will stop to function sooner and something dramatic will therefore have to happen in microelectronics in near future. With much faster and more complex digital systems being built, power consumption of CMOS circuits has become a major concern. Landauer [1] proved that power loss is an integral feature of irreversible circuits that have information loss irrespective of the technology the circuit is implemented in. Also, Bennett [2] showed that in order to keep a circuit from dissipating any power, it had to be composed of reversible gates. Reversible are circuits (gates) that have the same number of inputs and outputs and there is a one- to-one mapping between vectors of inputs and outputs. Thus the vector of input states can be always uniquely
reconstructed from the vector of output states. Because truly low power circuits cannot be built without the concepts of reversible logic, various technologies and circuits for reversible logic are recently being studied [2].

1. b. Proposed Contribution

In this paper, the focus is on the application of proposed reversible KTR gate and its implementation for designing novel reversible Braun Array Multiplier .The partial products can be generated in parallel using Fredkin gates and thereafter the addition can be done using the full adders designed from newly proposed KTR gate. A 4x4 architecture of the proposed reversible Braun Array Multiplier is also designed. It has been proved that the proposed multiplier architecture using the proposed KTR gate is better than the existing ones in literature, in terms of number of reversible gates employed. The reversible circuits designed and proposed in this paper form the basis of the ALU of a primitive quantum CPU.

2. The New Proposal of Gate and Full Adder

2. a. KTR Gate

The inputs and the outputs of the proposed 4*4 reversible KTR Gate are A,B,C,D and P,Q,R,S respectively.

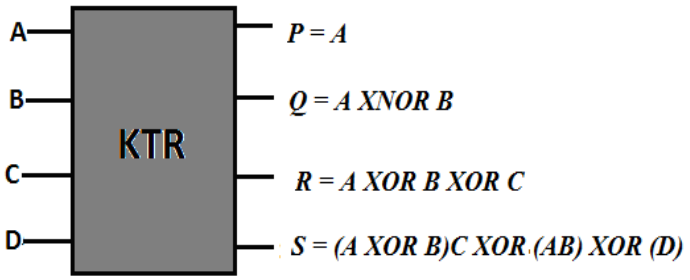

Figure 1. Proposed KTR Gate

The simple block diagram of the proposed KTR Gate is shown in the figure 1.

2. b. Full Adder Circuit using the Proposed KTR Gate

The proposed Reversible KTR Gate acts as Full adder to exhibit the Sum and Carry when the input D is Supplied as '0'

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as shown in the figure 2.On Implementing the Proposed KTR gate as a full adder we have 2 garbage outputs. Sum and Carry are taken in the output C and D respectively.

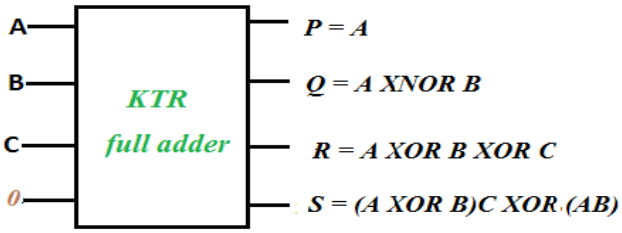


Figure 2.Full adder using KTR Gate

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	1	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	1
0	1	1	1	0	0	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

Table 1.Truth Table of the Proposed KTR Gate

The Truth Table for the proposed KTR gate is given by Table-1. From the truth table it is clearly inferred that the proposed KTR Gate is perfectly reversible as it is one to one mapping.

A number of reversible full adders were proposed already. Table -2 gives a comparison between the existing full adder circuits and the proposed one using the KTR Gate.[3]

Composition	Gates	Optical Cost	Delay
Toffli + Feynman	16+3	54	13Δ
TNOR + Feynman	16+3	38	8Δ
TNOR + Toffli	8+6	34	13Δ
NR Gate	2	8	4Δ
KTR Gate	1	3	-

Table 2.Comparison between Adders

3. Braun Array Multiplier

Braun Multiplier in standard form has (n-1) Carry Save Adder stages for generating partial products and one Ripple Carry Adder stage which give final 4 MSB Product Bits. [4].

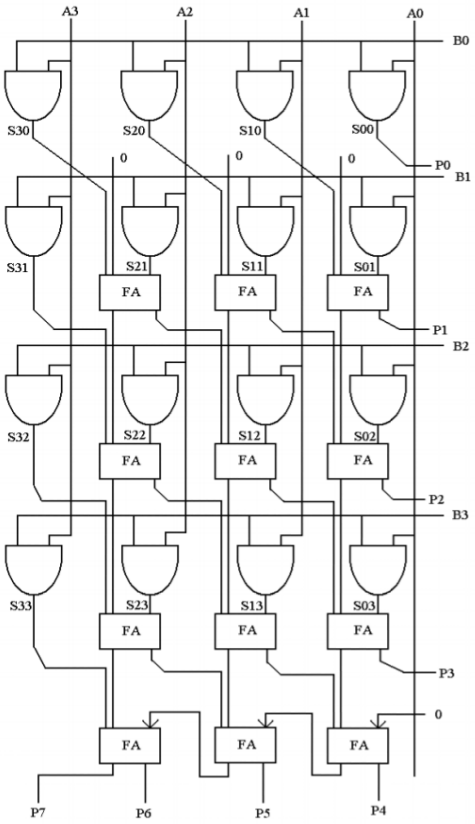


Fig 3: Braun Array Structure

3. a. Carry Save Adder

Carry save adder is a digital adder which is used to compute sum of three or more n-bit binary numbers. Carry save adder is same as a full adder. It generates two outputs of equal dimensions as the inputs.

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation.

The basic idea is that three numbers can be reduced to 2, in a (3:2) compressor, by doing the addition while keeping the carries and the sum separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs.

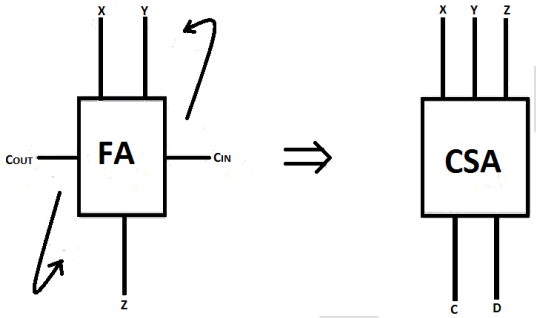


Fig 4: The carry save adder block is the same circuit as the full adder.

The sum and carry can then be recombined in a normal addition to form the correct result. It is only the final recombination of the final carry and sum that requires a carry propagating addition.

3.b Ripple Carry Adder

A simple ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Figure 5 shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. The main drawback of this adder is that the total propagation delay, T is directly proportional to the total number of stages of Ripple Carry Adder. If the total no. of stages are N and propagation delay of each stage is tp, then total propagation delay of ripple carry adder will be T= N x tp.

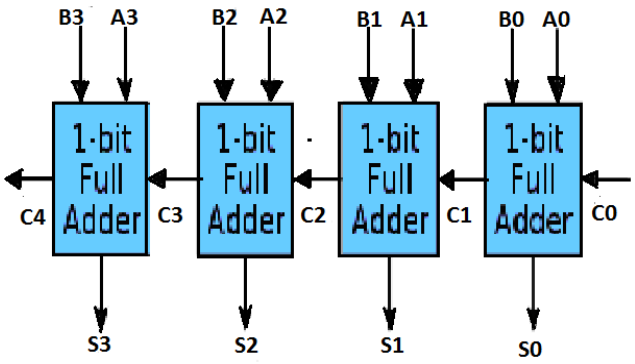


Fig 5: 4-Bit Ripple Carry Adder

4. The Proposed Novel Reversible Braun Array Multiplier Architecture using the proposed KTR GATE

The parallel generation of the products are obtained using the Fredkin gates [5]. Figure 6 represents the parallel generation of the products using the Fredkin Gate. The proposed reversible 4 bit Braun array multiplier needs 12 adders to be executed. All the partial products are computed in parallel, then collected through the cascaded array of carry save adders. At the bottom of the array, an adder is used to convert the carry save form to the required form. Here in the proposed architecture KTR 1 to 9 acts as an carry save adders and KTR 10,11,12 acts as an ripple carry Adders (Carry of the 1st adder is given as the input to the Next Adder). Figure 7 represents the Proposed 4x4 Novel Reversible Braun Array Multiplier

X3	X2	X1	X0	
X3.Y0=d	X2.Y0=c	X1.Y0=b	X0.Y0=a	Y0
h	g	f	e	Y1
l	k	j	i	Y2
p	o	n	m	Y3

Fig 6: The parallel generation of the products

Computation time is fixed by the depth of the array and by the carry propogation characteristics of the adder. Notice that multiplier is suited only for the positive operands. The efficiency of the proposed reversible Braun array multiplier greatly depends on the choice of the reversible parallel adder. The efficient parallel adders proposed here will significantly

improve the multiplier efficiency as it has less delay we also can reduce the power consumption by running less number of adders and switching off those adders which are not in use. The multiplier is most optimized compared to its existing reversible counterpart in literature [6]. The proposed 4x4 bit multiplier is designed with bare minimum of 28 reversible gates while its existing counterpart in [6] has 28 reversible gates.

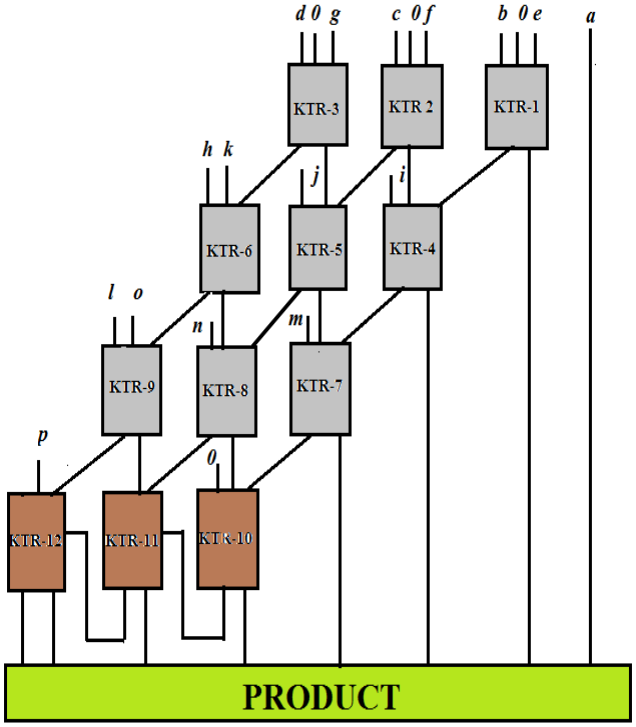


Figure 7. Proposed 4 x4 Novel Reversible Braun Array Multiplier

The results can be generalized for NXN bits. The numbers of garbage outputs are nearly same for both the multiplier. Table 2 shows the comparison efficiency of the reversible multipliers.

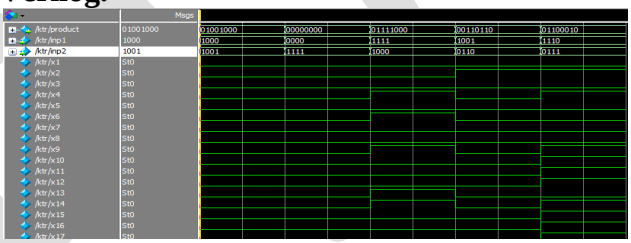
5. Comparison table between Existing Multiplier and the Proposed Braun Array Multiplier

Here in this Section, We just compare the No .of gates used and the Overall Speed of the Ordinary Multiplier and the Braun Array Multiplier. This comparison is given in the table 3.

Multipliers Design	No. of Gates	Parallel Adder Dependency	Overall Speed
Existing Circuit[6]	**40**	No	Low
Proposed Braun Array Multiplier	**28**	Yes	High

Table 3.Comparison Table

6. Simulation Output of Proposed KTR Gate By Verilog.



7. Conclusion

The proposed Reversible Braun Array Multiplier using newly proposed KTR Gate has an advantage of acquiring high speed as it is a parallel multiplier. Braun Array Multiplier also have a disadvantage that it can be implemented only for signed components. This can be overcome by using Baugh Wooley Multiplier which is the future scope of this research article.

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