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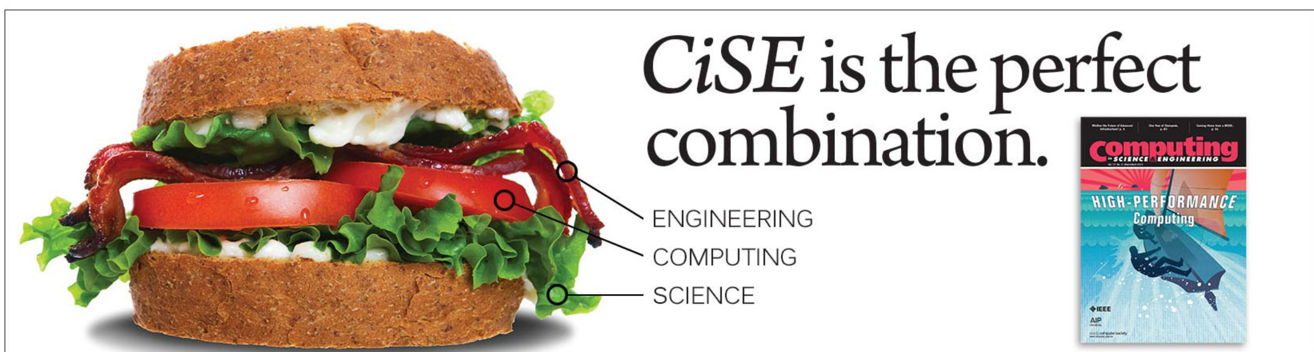

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Growth of antiphase-domain-free GaP on Si substrates by metalorganic chemical vapor deposition using an *in situ* AsH_3 surface preparation

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Antiphase-domain (APD) free GaP films were grown on Si(100) substrates prepared by annealing under dilute AsH_3 *in situ* in an MOCVD reactor. LEED and AES surface analysis of Si(100) surfaces prepared by this treatment show that AsH_3 etching quickly removes O and C contaminants at a relatively low temperature (690–740 °C), and creates a single-domain "A-type" As/Si surface reconstruction. The resulting GaP epilayers grown at the same temperature are APD-free, and could thereby serve as templates for direct growth of III-V semiconductors on Si. This single chamber process has a low thermal budget, and can enable heteroepitaxial integration of III-Vs and Si at an industrial scale. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4929714]

The heteroepitaxial growth of III-V semiconductors on Si substrates is an enabling technology for lowering the cost of high-efficiency multijunction photovoltaics and optoelectronic devices.[1] The nucleation and growth of GaP on Si can serve as a seed layer for the growth of other III-V materials because GaP and Si have a relatively small lattice mismatch (0.37% at 300 K). Although the integration of GaP and Si has been a topic of research for decades, this technology has not yet been widely adopted in industry, unlike the analogous growth of GaAs on Ge.[2] There are several challenges that must be overcome to produce high-quality material from III-V on Si heteroepitaxy; namely, the lattice mismatch, the thermal expansion mismatch, and the formation of antiphase domains (APDs) due to the growth of polar III-V materials on non-polar Si substrates.

Most recent GaP/Si work has been performed by first growing a homoepitaxial Si buffer layer and annealing under H_2. This creates a double atomic step reconstruction that avoids the formation of APDs by enabling the nucleation on different terraces to grow in registry, without the formation of P-P or Ga-Ga bonds that can lower the material quality of the III-V semiconductor.[3,4] This approach has been successful for the growth of GaP on Si by both metalorganic chemical vapor deposition (MOCVD)[3,4] and molecular beam epitaxy (MBE).[5] Low defect density III-V on Si growth has also been previously demonstrated by thermal cycling to decrease the density of threading dislocations.[6] While these processes are successful at a laboratory scale, the high temperatures and times required for annealing and to grow the Si buffer may not be industrially feasible and have been shown to have detrimental effects on the bulk properties of the Si substrate, which is a problem for the development of solar cells or other devices where the Si semiconductor is electronically active.[7]

Here, we investigate an alternative approach that is much simpler and, due to a lower thermal budget, potentially less damaging to the underlying Si devices. In this approach, Si surfaces are prepared *in situ* by etching with AsH_3 in the MOCVD reactor used to grow GaP. Prior work has shown that annealing Si under AsH_3 in an MOCVD reactor can etch the Si surface to produce a flat 2-domain $(2 \times 1)/(1 \times 2)$ reconstructed surface and remove carbon and oxygen.[8,9] Detailed studies of the As/Si(100) surface carried out in MBE systems have shown that a variety of step topologies can be obtained under different As deposition conditions.[10,11] APD-free GaP/Si growth has been demonstrated after AsH_3 annealing,[12,13] but this result was never correlated with the state of the pre-nucleation As/Si surface. Using Auger electron spectroscopy (AES), we show that a brief AsH_3 exposure at temperatures between 690 and 740 °C removes surface C and O contamination from Si surfaces that have been chemically cleaned prior to growth, and establishes a double-stepped (1×2) surface. Reflectance difference spectrometry (RDS) enables *in situ* monitoring to precisely determine at what point this surface has been established and GaP nucleation can begin. LEED images indicate that subsequently grown GaP follows the stacking sequence established by this surface, producing GaP(100) with a (111)B offcut. Transmission electron microscopy (TEM) and other characterization techniques confirm that the resulting GaP is APD-free and the crystalline quality of both the GaP and the GaP/Si interface are excellent. The ability to grow high-quality GaP using a fast AsH_3 pretreatment at a relatively low temperature in a single chamber with no Si regrowth makes this process the most industrially relevant candidate for the direct heteroepitaxy of III-V semiconductors on Si substrates.

All growth in this work was performed in a low pressure (50 Torr) MOCVD system attached directly to an ultrahigh-vacuum (UHV) surface analysis chamber, which allows the Si surface to be studied without exposure to atmospheric conditions. Si(100) substrates (1 cm × 1 cm or 2 cm × 2 cm) with an offcut of 2°, 4°, or 6° toward [111] were cleaned with a 2:1:10 mixture of ammonium hydroxide, hydrogen peroxide, and de-ionized water (DI H_2O) at room temperature, rinsed in DI H_2O, and then etched with 10% HF for 30 s

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prior to loading into the MOCVD reactor.[14] The AsH_3 etching process was performed by annealing under low AsH_3 partial pressures (0.029–0.71 Torr) diluted in 50 Torr of purified H_2 (total flow rate of 3.5 lpm) for 2–10 min. The samples were rapidly heated to temperatures between 780 and 800 °C under AsH_3 (temperature measured by a calibrated pyrometer at the back of the graphite sample chuck), then immediately cooled to the annealing/growth temperature for 2 min (see temperature profile in Fig. 2(b)). As/Si(100) samples that underwent surface analysis were cooled to 300 °C under the same AsH_3 partial pressure and then immediately transferred to an UHV surface analysis chamber where AES and low-energy electron diffraction (LEED) were used to characterize the composition and structure of the surface.

For GaP growth, PH_3 and triethylgallium (TEG) were used as precursors under a high V/III ratio (V/III = 3000–5600) with a PH_3 partial pressure of 5.5–5.8 Torr. GaP growth was carried out at substrate temperatures of 690–740 °C. After growth, GaP samples were cooled under PH_3 to 300 °C and then under H_2 before being transferred out of the reactor. During both etching and GaP growth, the surfaces of the samples were monitored using RDS at 3.25 and 3.5 eV.[15] Atomic force microscopy (AFM) images were collected using a Veeco D3100 operated in tapping mode. Cross-section and plan-view samples for TEM analysis were prepared using standard mechanical polishing and dimpling techniques. Final thinning to electron transparency was performed using low kV Ar^+ ion milling with the samples continuously rotated and cooled using a liquid nitrogen cold stage. The samples were examined in a FEI G2 30 Super Twin TEM operated at 200 kV to avoid beam damage to the Si. For plan-view specimens, the samples were ion milled from the Si substrate side only with the GaP surface protected using a glass cover slip to prevent re-deposition of ion milled material. A Panalytical X-Pert Pro diffractometer was used to obtain high-resolution XRD reciprocal space maps of the (004) and (224)GI planes of the GaP/Si films.

AES analysis of samples in different stages of processing (as received, after wet cleaning and HF, and after the AsH_3 treatment) is shown in Figure 1. These data demonstrate that the AsH_3 treatment is more effective at removing C and O contaminants from the surface than wet chemical cleaning (2:1:10) alone, and any remaining C or O is below the detection limit of the AES system (∼3%–5% coverage). The etching of Si, C, and O from the surface is attributed to the presence of H from dissociated AsH_3, and As then chemically passivates dangling bonds on the Si surface, preventing other materials from sticking to the Si.[14] Exposure to high flow rates of AsH_3 is known to induce faceting/roughness of Si surfaces (and also Ge surfaces, to a lesser extent).[8,16] However, AFM scans (25 μm^2) of samples that underwent the low AsH_3 partial pressure process had only slightly increased roughness (R_q = 0.11 nm vs. 0.09 nm for an un-etched sample from the same wafer). Increasing the time of the AsH_3 process resulted in increased surface roughness (R_q = 0.47 nm for a 10 min AsH_3 pretreatment). This indicates the importance of the AsH_3 annealing time, as extended exposure can detrimentally roughen the Si surface.

In situ RDS greatly facilitated the development of this process by providing real-time information about the

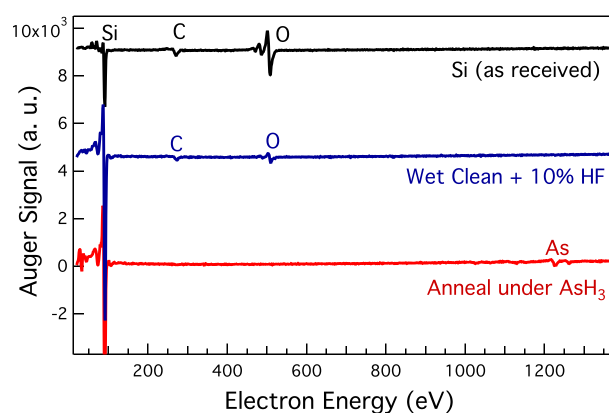

FIG. 1. AES data for Si surfaces at different stages of processing which show that AsH_3 effectively removes C and O, while wet cleaning processes do not: (black) as-received Si with native oxide, (blue) HF-dipped Si surface, and (red) As/Si(100) surface prepared by exposing Si to AsH_3 for 2 min at 740 °C.

existence and average direction of the surface dimers. This technique measures the difference in reflection between two orthogonal directions of a beam of polarized light incident on the sample.[17,18] Figure 2(a) shows energy scans taken on an Si substrate before, during, and after the AsH_3 process. Samples that have only been subjected to a wet chemical clean have no clear RDS signature, as the dihydride Si surface has no Si–Si dimers. Dimerized As/Si samples have RDS spectra peaks with energies at 3.35 and 3.85 eV, and the direction and amplitude of these peaks correlates with the average direction of the As–As dimers on this surface. Although the magnitude and position of these peaks changes with sample temperature, a time dependent ΔR/R at specific wavelengths provides a signature peak-splitting that correlates with the removal of residual oxide from the surface and formation of a single domain surface (Fig. 2(b)).

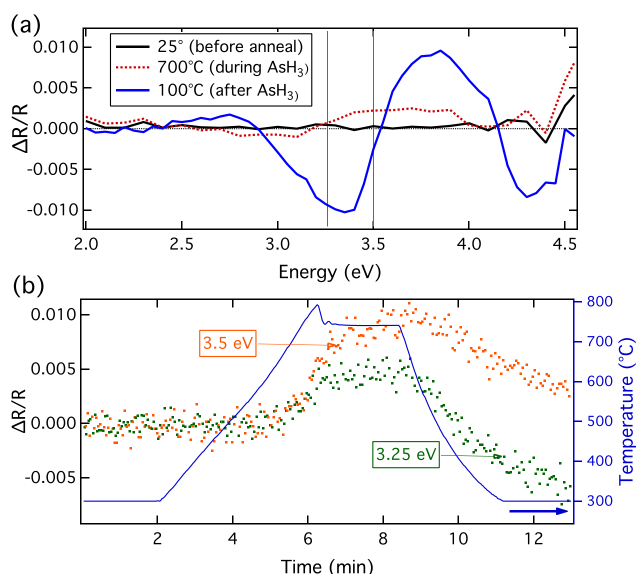

FIG. 2. (a) Representative RDS energy scans before (black), during (red-dashed), and after AsH_3 treatment (blue). Vertical lines indicate the energies monitored during pretreatment and GaP growth. (b) RDS time scan data (green, orange) and pyrometer temperature data (blue) during the AsH_3 treatment process. The energy dependent signal can be used to monitor the formation of the desired As/Si surface.

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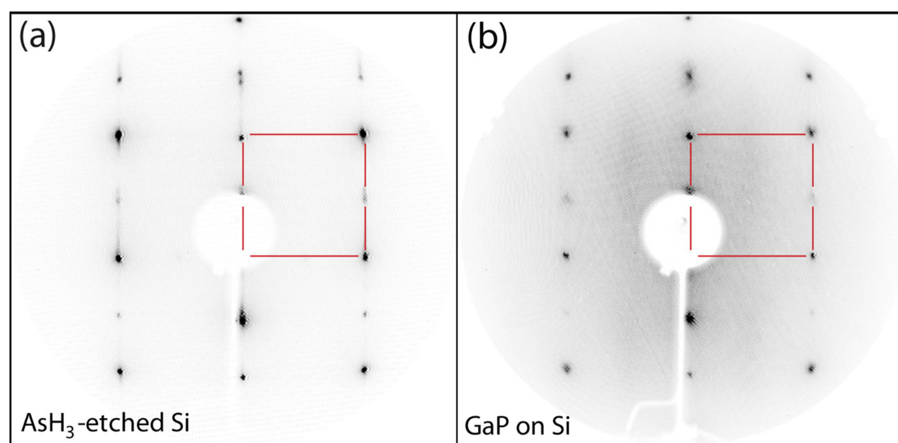

FIG. 3. (a) LEED pattern of As/Si(100) offcut 4°-[111] taken at 65 eV immediately after annealing under AsH_3 which indicates a single-domain surface [PD299]. (b) LEED of GaP/Si taken at 65 eV after annealing under PH_3 for 10 min at 700 °C [PD305].

Figure 3(a) shows the LEED pattern of an As/Si(100) surface miscut 4°-[111] after it was annealed under AsH_3 for 2 min, then cooled under flowing AsH_3 and transferred to the analysis chamber as described earlier. The absence of diffraction spots perpendicular to the direction of step-splitting indicates that this is a single domain (1×2), "A-type," or "D_A" surface.[19] The same AsH_3 treatment produced single-domain surfaces on Si with 2°-[111] and 6°-[111] offcuts (not shown). Continued exposure to AsH_3 can produce a two-domain surface, demonstrating the sensitivity to process parameters and the value of *in situ* monitoring with RDS.

The MOCVD reactor used for this work is not opened to the atmosphere between runs. This reduces its exposure to contaminants from the surroundings, but means that the reactor history can be more important than for a reactor that can be cleaned before every run. The most significant background species is As_x, which provides enough As to create As/Si surfaces with structures very different from clean As-free surfaces.[8] After the reactor is opened to the environment, or has been sitting idle for multiple days, a small amount of (2×1) character is sometimes detected by LEED. However, single domain (1×2) surface reconstructions have been obtained after reactor coat runs containing Ga, As, P, and In (as well as trace dopants). This suggests that uncontrolled extrinsic contaminants in the reactor that are below the detection limit of AES may affect the step topology of the resulting surfaces.

GaP films were grown on these surfaces by immediately switching from flowing AsH_3 to flowing TEGa and PH_3 once the (1×2) As/Si surface had been established. The growth rate of GaP was 5–6 nm min^{-1}. The V/III ratio was varied, but did not produce a noticeable change in film morphology for ratios >3000, similar to prior reports.[20] No APDs or other nucleation-related defects were observed by TEM (as discussed below). At the edges of the $(2 \times 2$ cm) samples, the growth of triangular (100) facets that pointed "downhill," or toward [111], were regularly observed. The majority of films grown remained smooth during the growth process with an RMS roughness of ∼5 nm for 90–100 nm thick films. However, for some growths, after ∼15 nm of growth, the surface of some GaP films began to show triangular faceting over large areas, observable as a sharp change in the RDS signal. The mechanism for the formation of these facets is still under investigation, but may be due to extrinsic contaminants from the reactor, as discussed above. Figure 4 shows the (224) GI reciprocal space map of a 75 nm thick GaP/Si film. Although the GaP/Si film (75 nm) is over the modeled critical thickness, XRD showed no significant relaxation within the detection limits.[21] The reciprocal space map of the (004) plane showed that negligible epilayer tilt and Pendellösung fringes were observed, which indicate planar epilayer interfaces.

Figure 3(b) shows the LEED pattern for the same 75 nm GaP film after it was unloaded from the reactor, and subsequently re-annealed under PH_3 for 10 min at 700 °C before surface analysis. This P-terminated GaP surface has dimer rows that are parallel to the step edges, indicating that the alternating sequence of Ga and P(100) layers in the GaP film continues the registry established by the As layer on the Si surface. This is consistent with other studies in which the orientation of dimers on the Si surface establishes the orientation of the subsequently grown GaP.[22] It has yet to be determined whether the As layer is displaced by the Ga and P precursors, or remains present at the Si/GaP interface.

Cross sectional TEM (Fig. 5(a)) and *ex situ* scanning AES of very thin GaP nucleation layers indicate that there is a continuous GaP film at the surface at nucleation. HRTEM images of the GaP/Si interface were taken both parallel and perpendicular to the direction of the wafer offcut and confirm a relatively flat interface (Fig. 5(b)). Unlike prior reports of

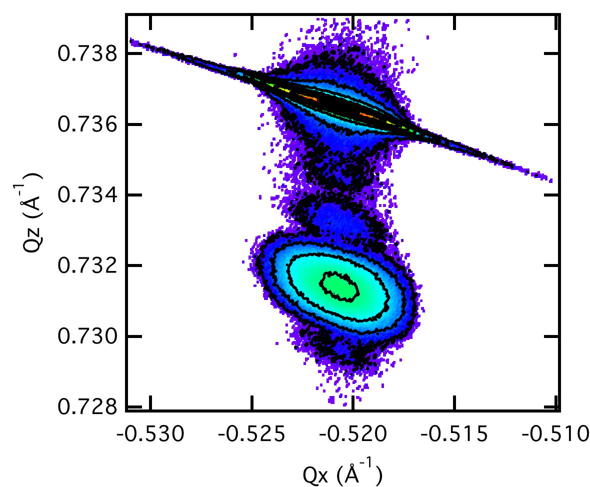

FIG. 4. X-ray diffraction (224) reciprocal space maps of a 75 nm GaP film on Si with very little relaxation [PD305].

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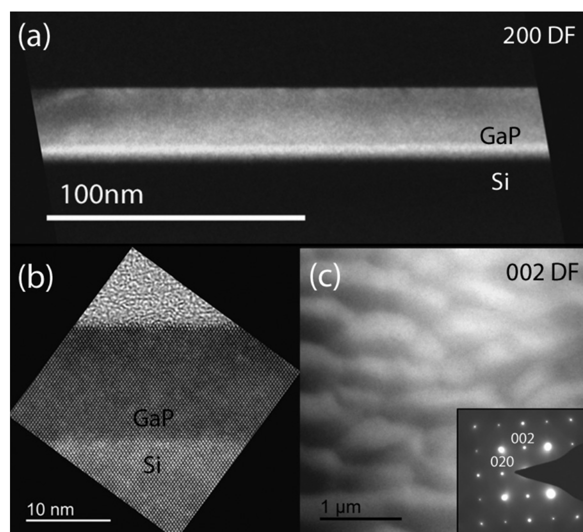

FIG. 5. (a) Cross sectional (200) DF TEM image of a GaP film grown on a Si(100) substrate with a 4°-[111] offcut showing no APDs, (b) high resolution TEM of GaP/Si interface, (c) plan view (002) DF TEM of a 96 nm GaP film; the inset {001} selective area electron diffraction image indicates the presence of zinc-blende GaP [PD288, PD341].

GaP grown on MOCVD-grown homoepitaxial layers,[3] no faceting of the Si due to step bunching was observed.

Plan view (002) dark field (DF) analysis of both 30 and 96 nm thick GaP films grown under the same conditions as the cross-section sample revealed contrast mainly associated with surface topography as well as a few strain-related features, but no APDs (Fig. 5(c)). The presence of strong {200} diffraction spots in selective area electron diffraction for a plan-view thinned sample (Fig. 5(c), inset) and energy-dispersive X-ray spectroscopy (not shown) confirm that this thinned region is zinc-blende GaP and not Si. No APDs were observed in multiple (002) DF plan-view images (total area = 160 μm^2), setting a conservative upper limit of $6 \times 10^5\,cm^{-2}$ for the number of APDs. In the thinner (30 nm) films, images were also taken using (220) DF to look for threading dislocations (TD), but none were observed, setting an upper limit on TDs at $2 \times 10^6\,cm^{-2}$.

Plan view TEM analysis of a 96 nm thick GaP film showed very little strain relaxation from misfit dislocation glide, which supports the observations from XRD that there is very little strain relaxation in these films. However, the film thickness is beyond the standard Matthews-Blakeslee critical thickness, and widely spaced misfit dislocations are observed, presumably due to glide of existing threading dislocations from the Si substrate. New dislocations likely have not formed because the activation energy for the nucleation of dislocation half-loops at the surface is higher than the available elastic energy, leaving the film metastable to glide and highly strained. The nucleation of new dislocations at a surface is generally catalyzed by stress-concentrating defects/structures, and these films are relatively flat and defect-free.

In conclusion, we have demonstrated that an *in situ* AsH_3 treatment is capable of removing C and O contaminants from offcut Si(100) substrates, and can produce a single domain (1×2) As/Si surface reconstruction on offcut Si substrates without the need for a homoepitaxial buffer layer. GaP films grown on Si prepared in this manner appear to be free of APDs and other nucleation-related defects. While this process was developed in a research reactor, *in situ* RDS characterization of the surface provides a metric that should enable this process to be transferred to manufacturing scale reactors. The low thermal budget and short process time of this pre-treatment process advances the feasibility of direct growth of III-Vs on Si for industrial applications.

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