A 98dB 3.3V 28mW-per-channel multibit audio DAC in a standard 0.35µm CMOS technology

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I. Introduction
The development of a number of multimedia systems has increased the demand for audio digital-to-analog converters (DAC) that meet the low-cost needs of consumer applications and achieve the wide dynamic range and high linearity required for professional use [1-4]. In addition to a cost-effective die size, there are several key requirements for such consumer high-end audio DAC’s:
• dynamic range (DR) to be in excess of 16b;
• robustness with respect to the considerable clock jitter of commercially available audio inter-face IC’s;
• fully integrated system: this implies not to require any external additional filter;
• low power consumption in order to house a stereo implementation in a small, low-cost plastic package; this is also important in terms of thermal dissipation when these devices are embedded in high-complexity mixed-mode systems;
• use of standard scaled-down CMOS technology: this is in trade-off with DAC performance due, for instance, to the impossibility to use low-threshold devices which would give small on-resistance switches [1];
• accurate in-band and out-of-band frequency response: this forces to use a high-order Switched-Capacitor (SC) filter which features a considerable folded-in-band noise;
• limited out-of-band noise (quoted by the ratio SNRout = Noise in the band [Fsout/2 – 2·Fsout] to be ≥ 60dB, with Fsoul=44.1kHz): this is in great contrast with power consumption. In fact a large SNRout can be achieved only by using high-order reconstruction filter which reduces DR and THD and increases power consumption;
• single-ended output: this allows to drive grounded loads and to have the number of external pins; it is in contrast with the audio high-performance typically reached only with differential structures.
This paper describes the design of a multibit Sigma Delta (ΣΔ) DAC that fulfills all the above demands. This has been possible thanks to the development of both architectural and circuit level solutions. On the architectural side, a single-loop dithered 3rd-order multibit architecture has been developed. At circuit level, the adopted 3rd-order fully-integrated SC filter topology allows to achieve low noise and high linearity. Using these design solutions, a fully-integrated stereo audio DAC with all filtering functions required for audio applications has been developed in a standard 0.35µm CMOS. The DAC achieves in a single-ended output a 98-dB A-weighted dynamic range in the band [20Hz-20kHz], and consumes 28mW per-channel (analog+digital) from a single 3.3V supply. The 3rd order filter allows to perform a SNRout larger than 60dB. Finally the device is able to drive a 10pF//40kΩ load.

II. Overall DAC Architecture
The overall adopted topology for the proposed DAC is shown in Fig. 1. The input 24b word at 44.1kHz is interpolated by a factor 64x. The resulting signal (24b) is passed through a 3rd-order multibit digital ΣΔ Modulator (ΣΔM) operating at 2.8224MHz which feeds a 13level bitstream to the 3rd-order fully differential analog reconstruction filter. The Diff-to-Single converter supplies the grounded output pin.

The key choice is the use of a multibit ΣΔM which gives the following advantages:
• a multibit quantizer gives extra resolution and then the OSR can be reduced. This results in relaxed speed requirements for the analog components and reduced power consumption;
• the multibit bitstream results in lower step at the output of the opamp in the reconstruction filter: this makes easier the opamp design;
• the design of the 3rd-order modulator is easier due to the relaxed stability requirements for the lower out-of-band noise.

The problem of a multibit ΣΔM is the non-linearity of the multibit feedback digital-to-analog interface, which is realized by a number of integrated unit elements (resistors, capacitors, current sources), due to the mismatch between the components. A Dynamic Element Matching (DEM) system is then adopted to linearize the interface behaviour. Such a DEM system is optimized with respect to the silicon implementation, depending on the amount of mismatch to be compensated, and its complexity. In this design a simplified implementation of the Data Weighted Average (DWA) algorithm [5] is adopted, in which only a certain number of unit elements are ‘scrambled’, while the other ones are fixed.

![Fig. 1 - Overall DAC architecture](image-url)
Regarding the reconstruction filter, a 3rd-order Chebyshev transfer function is adopted. This allows to accurately and deeply reject the out-of-band noise. The filter has been implemented with SC technique in order to reduce the sensitivity of the system on clock jitter. This is a key feature due to the considerable clock jitter of commercially available audio inter-face IC’s. In fact, if modulated by the clock jitter, the high frequency quantization is folded in the signal band, and this results in an in-band noise performance degradation. This problem is reduced by lowering the high-frequency quantization noise at the analog-to-digital interface. This has been done by using a multibit quantizer and by implementing a low-pass digital filter with a zero at Fs/2. The differential analog output signal of the SC reconstruction filter is finally processed by the Differential-to-Single ended block which presents a pole at 1.2MHz.

III. Multibit \(\Sigma \Delta\) Digital modulator

The targets of the digital \(\Sigma \Delta\) are the following:
- SNR=110dB in the audio band [20Hz-20kHz];
- Signal attenuation in the audio band < 0.001dB
- Harmonic distortion < -90dB;
- Idle Tones amplitude < -130dB.

These results are achieved by using:
- a third order−single loop structure;
- a multibit quantizer with 7 levels (one level on 0);
- an oversampling ratio OSR=64.

The zeros of the NTF are given by the Chebyshev response in order to obtain a flat noise floor in the audio band. One zero is placed at dc and the other two zeros are placed at ±17kHz. This allows to obtain an improvement of about 6dB for the DR compared to the case in which all zeros are placed at dc. The noise attenuation due to the zeros is partially compensated by the poles placed near the audio band. The positions of the poles of the NTF are determined by the out-of-band−gain of the NTF (defined as \(\text{NTF}\)). This parameter is dimensioned by achieving a good compromise between an increase of DR and the reduction of the stability margin. In fact there is a trade-off between stability and DR. To improve stability, the minimum value of \(\text{NTF}\) which gives approximately SNR=110dB (i.e. \(\text{NTF}=2\)) has been adopted.

![Fig. 2 - Digital \(\Sigma \Delta\) Modulator](image)

The \(\Sigma \Delta\) M achieves the following results:
- Maximum dynamic of the input signal 0dB;
- SNR(0dB)=111dB;
- SNR(60dB)=51.7dB;
- Idle Tones amplitude near to -132dB.

The STF is determined by the type of architecture chosen to realize the NTF. In order to realize an NTF with the previous characteristics and a low pass STF, the CRFB (Chain of Resonator in Feedback Form) architecture, as reported in Fig. 2, has been chosen.

The quantizer has seven levels and their values in the analog domain are \([-1.5, -1, -0.5, 0, 0.5, 1, 1.5]\). The \((1+z^{-1})\) block at the output of the modulator attenuates the high frequency noise and the idle tones (this also reduced the sensitivity of the system from jitter). A drawback of this output filter is the double of the output level number. The output levels are 13, they are centered around zero and their analog values are: \([-3, -2.5, -2, -1.5, -1, -0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3]\).

Idle tones attenuation is provided by inserting a white noise (dither) in the modulator. The dither generator is realized with a PRSG (Pseudo Random Sequence Generator) made of 19 unity delay elements. The effect of this dither (9dB DR improvement) is shown in the SNR plot of Fig. 3.

![Fig. 3 - Digital \(\Sigma \Delta M\) SNR plot](image)

IV. SC DAC Filter

The target of the analog filtering section is to smooth the digital bitstream and to reject the out-of-band noise. SC implementation guarantees reduced sensitivity to the clock jitter. The use of a multibit input word implies a smaller amount of charged injected in the virtual ground (with respect to the 1b solution). This allows to relax the slew-rate requirements for the opamp, in particular for low-level input signals. In audio, the performance at a very small signal level such as –60dBFS is important.

The structure of the SC filter is shown in Fig. 4 in its single-ended configuration (in the actual form a differential structure is adopted).

![Fig. 4 - 3rd-order SC reconstruction filter](image)

A 3rd order filter with a Chebyshev transfer function is used in order to strongly reduce the out-of-band noise. An array of 12 unit capacitors controlled by the 13-level word fed by the \(\Sigma \Delta\) M operates as input structure. The design employs the direct charge transfer (DCT) technique, where the array of 12 SC’s is used for input sampling and feedback [6]. A multibit DAC implementation using this technique makes the slew component of the sampling capacitors negligible, resulting in output drive requirements comparable to
continuous-time implementations [3]. Table I reports the capacitor value (in pF). The fully differential circuit operates at a clock rate of 2.8224MHz. During the sampling phase, they sample either VDD or GND depending on the corresponding input data. During the integration phase, all capacitors are connected in parallel between the 1st opamp input node and the SC filter output. The output level is generated passively by distributing the charge in the feedback path.

**TABLE I - CAPACITOR VALUES (IN PF)**

<table>
<thead>
<tr>
<th>Cin</th>
<th>C13</th>
<th>C14</th>
<th>C21</th>
<th>C22</th>
<th>C23</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.16</td>
<td>38</td>
<td>1.29</td>
<td>1.41</td>
<td>1.11</td>
<td>1.28</td>
</tr>
</tbody>
</table>

At the discrete-to-continuous-time interface of a SC circuit, the distortion performance is determined by the nonlinearity of the whole behaviour of the analog output waveform, instead of only its final value at the end of the clock phase. The nonlinearity results from opamp slew-rate, signal-dependent charge injection, and signal-dependent RC time constant. The DCT scheme eliminates spikes generated by slew-rate limitation. The effect of charge injection are reduced by using four-phase nonoverlap clocks with delayed bottom plate switching [6].

### A. Opamp Design

The opamps embedded in the DAC have been designed with different schemes taking into account the different requirements they have. The first opamp is required to feature low-noise because it is the major output noise contribution. A class A folded cascode with gain-boosting opamp has then been used as shown in Fig. 5. On the other hand, the other two opamps in the SC filter are required to guarantee driving capability with less stringent noise requirement. The two-stage class AB structure shown in Fig. 6 has then been used. The driving capabilities of the 3rd opamp has to be larger than that of the 2nd, and then it draws larger current. Table II summarizes the opamp features.

**TABLE II - OPAAMP FEATURES**

<table>
<thead>
<tr>
<th>Opamp</th>
<th>1st</th>
<th>2nd</th>
<th>3rd</th>
<th>Diff-to-Sing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain [dB]</td>
<td>120</td>
<td>106</td>
<td>106</td>
<td>110</td>
</tr>
<tr>
<td>GBW [MHz]</td>
<td>45</td>
<td>40</td>
<td>42</td>
<td>5</td>
</tr>
<tr>
<td>Phase margin [°]</td>
<td>7</td>
<td>85</td>
<td>55</td>
<td>6</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>7.9</td>
<td>3.3</td>
<td>4.6</td>
<td>5.5</td>
</tr>
</tbody>
</table>

### B. System optimization

The distortion has been optimized by using 4-phase clock scheme, while no advantage has been taken from the standard technology for the switch realization (no low threshold device are available [1]). Optimum settling for the opamp is obtained by letting the adjacent opamps to settle independently. This is also exploited in power saving. In fact the opamps are drawing the nominal current only during the phase in which they are processing the signal, while during the other phase their power consumption is reduced [7]. This allows a 30% power saving with respect to the case in which the opamps are drawing always the nominal currents. Regarding noise performance, in such a SC filter structure, only the noise of the first opamp reaches the output. In addition, the use of the input capacitor placed in the overall feedback allows that the gain of the noise of the 1st opamp reaches the output node with unitary gain [8]. The noise performance of the SC filter has been evaluated, as given in Table III. The switches and the opamp thermal noise (due only to the 1st opamp) have been designed to be at the same level. 1/f noise is made negligible by using large input stage device (the input device size is 2500µm/0.8µm).

**TABLE III - EVALUATED NOISE CONTRIBUTION**

<table>
<thead>
<tr>
<th>Maximum allowable noise for DR =100dB [pV²]</th>
<th>237.00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantization noise [pV²]</td>
<td>15.85</td>
</tr>
<tr>
<td>Switches thermal noise (kT/C) [pV²]</td>
<td>67.60</td>
</tr>
<tr>
<td>Opamp thermal noise [pV²]</td>
<td>55.28</td>
</tr>
<tr>
<td>Opamp 1/f [pV²]</td>
<td>6.35</td>
</tr>
<tr>
<td>Total noise [pV²]</td>
<td>160.93</td>
</tr>
</tbody>
</table>

### V. Experimental results

The chip photograph of the audio DAC is shown in Fig. 7, where two (stereo) channels are realized. The chip measures 2.9mm² in 0.35µm double-poly five-metal CMOS. The active area is 45% digital and 54% analog. The DEM overhead is only 1% of the total die area.

All measurements were taken by using Audio Precison System 2. No additional external filter is adopted. In addition all the measurements have been done at the single-ended output node. This gives worse performance than those achievable at the differential internal nodes. An optical data link between the test board and audio analyzer was used for better isolation.
Fig. 8 shows the overall DAC frequency response (a -10dBFS input signal is applied). In Fig. 9 line A shows the output spectrum for a 5kHz –60dBFS input signal. The noise floor is approximately −130dBFS, and the largest in-band tone is smaller than −115dBFS.

The noise floor is approximately −130dBFS, and the largest in-band tone is smaller than −115dBFS. For audio applications, dynamic range is usually calculated as SNDR at −60dBFS, which is 98dB. This yields a 98dB dynamic range. The SNDR at full-scale is 86dB. Fig. 9 demonstrates also the effectiveness of the DEM. Line A refers to the case with DEM machine on, while for line B the DEM is turned off. Finally, Fig. 11 shows the out-of-band noise spectrum. This results in a SNRout=78dB, which is considerably higher than in other competitive solutions. This is achieved thanks to the 3rd order SC filter. The DAC performance is summarized in Table IV. Channel separation between the two audio channels is more than 120 dB. The total power dissipation is 56mW from a single 3.3V supply, for the two stereo channels.

**TABLE IV - DAC PERFORMANCE SUMMARY**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td></td>
<td>Standard 0.35µm CMOS 2P5M</td>
</tr>
<tr>
<td>Power supply</td>
<td>V</td>
<td>3.3</td>
</tr>
<tr>
<td>Analog power consumption</td>
<td>mW</td>
<td>32.6</td>
</tr>
<tr>
<td>(stereo)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital power consumption</td>
<td>mW</td>
<td>23.1</td>
</tr>
<tr>
<td>(stereo)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output swing Vrms</td>
<td></td>
<td>0.9</td>
</tr>
<tr>
<td>Dynamic Range (A-weighted)</td>
<td>dB</td>
<td>98</td>
</tr>
<tr>
<td>SNDR Peak</td>
<td>dB</td>
<td>86</td>
</tr>
<tr>
<td>Channel separation</td>
<td>dB</td>
<td>120</td>
</tr>
<tr>
<td>SNRout</td>
<td>dB</td>
<td>78</td>
</tr>
<tr>
<td>Chip size (stereo)</td>
<td>mm²</td>
<td>2.9</td>
</tr>
</tbody>
</table>

VI. Conclusions

In this paper one of the most performing 3.3V voltage mode fully-integrated DAC in a standard CMOS technology is reported. The high reconstruction filter order allows to achieve an accurate in-band frequency response and a large out-of-band noise rejection without any external component. The already significantly low power consumption could be dramatically reduced by relaxing the out-of-band noise rejection requirements.

Acknowledgements

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References
