A Low-Power BiCMOS Switched-Capacitor Filter for Audio Codec Applications

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Abstract—A fully integrated fourth-order filter embedded in a complete 16-b oversampled D/A converter to be used in an audio stereo codec is presented. The possible noise and distortion sources have been accurately evaluated in the design and their contributions have been properly limited. This allows the reduction of the power consumption while satisfying the application requirements.

The filter is realized in 0.7-μm BiCMOS technology with an active area of about 1.3 mm². A total harmonic distortion (THD) of −75 dB for a full scale input signal and an SNR of 96 dB have been achieved. The power consumption of the filter has been maintained within about 40 mW from a single 5-V supply voltage.

Index Terms—Analog integrated circuits, switched capacitor filters.

I. INTRODUCTION

In audio frequency range, digital signal processing (DSP) has become dominant with respect to analog alternatives. Audio signals are typically processed by DSP using 16-b accuracy, and no conceptual limitations exist to increase the number of bits. Practical limitations, however, arise from the front-end (A/D converter) and back-end (D/A converter) interfaces which are necessarily of analog nature. Therefore, in order to guarantee the 16-b accuracy in audio signal processing, codec architectures use high-performance A/D and D/A interfaces [1]–[6].

In a stereo codec system under development, for each channel the back-end D/A converter presents the structure shown in Fig. 1. A 44.1-kHz 16-b input digital signal (with the typical audio signal band of 20 Hz–20 kHz) is processed by a finite impulse response (FIR) interpolating filter which increases the sampling rate to 11.2896 MHz (i.e., 256 × 44.1 kHz). This signal is then fed into a second-order digital ΣΔ modulator which shapes the quantization noise spectrum.

Finally, the resulting 11.2896 MHz 1-b bit stream is passed through a low-pass filter to reconstruct the analog signal.

In this paper the filtering section which performs the low-pass function of the digital bit stream is presented. In the signal band [20 Hz–20 kHz], the filter is required to feature an SNR of 96 dB (16 b) and a total harmonic distortion (THD) better than −72 dB for a full-scale input signal. In addition, in the same band a linear phase response and −0.2 dB maximum attenuation are required. Since the noise and distortion performance of the digital ΣΔ modulator are better than −110 dB, the performance of the whole D/A converter will be limited by the filter performance.

The realized low-pass filter is composed by the cascade of a third-order switched capacitor (SC) section and a first-order RC active section. The SC section operates at the same frequency of the input bit-stream (i.e., 11.2896 MHz). The SC technique has been chosen in order to have an accurate frequency response and to reduce the effects of the bit-stream nonidealities (like clock jitter and inaccurate edges). The input bit stream is single-ended, and the output signal is required to be single-ended. For the SC section, a fully differential implementation has been chosen since it improves the SNR with respect to the single-ended implementation. This is due to the larger available signal swing and to the better immunity from the unwanted coupling of disturbs, normally of common-mode nature. Finally, the RC section also performs the differential-to-single-ended transformation. The filter (and the overall converter) has been realized in a 0.7-μm BiCMOS technology. The noise and THD requirements have been satisfied using only about 40 mW, which is a small power amount if compared with previous implementations with similar architecture [1]–[4].

The structure of the paper is the following. After this introduction the filter design is described in Section II. The transfer function optimization and its implementation in the SC–RC networks are given. The adopted solutions for the noise and distortion reduction are then depicted. In Section III experimental results are reported, and Section IV gives conclusions.

II. FILTER DESIGN

The developed filter architecture is given in Fig. 2. The first block is a single-ended to fully differential converter which is fed by the input bit stream. It is followed by the cascade of a third-order fully differential SC filter and a first-order continuous-time (CT) filter. The use of the SC technique guarantees a good accuracy in the frequency response; therefore it is possible to correct the gain loss (−0.2 dB) at 20 kHz with a predistortion of the previous FIR digital filter transfer function. In addition, the SC sampled-data operation allows a natural interfacing with the previous digital section.

The first-order continuous-time filter allows the smoothing of the SC filter output signal. In addition, it accomplishes the final fully differential to single-ended transformation. The cutoff frequency has been designed to be equal to 500 kHz, i.e., much higher than the one of the SC filter in order to reduce the effects of the R and C imprecision in the in-band filter frequency response.
A. Filter Transfer Function

The required accuracy of the frequency response in the signal band is achieved by using SC technique. The SC section implements a third-order Bessel transfer function in order to satisfy both amplitude and phase requirements with the following poles and quality factor: $f_{p12} = 108.93$ kHz with $Q_{1,2} = 0.691$, and $f_{p3} = 99.525$ kHz. The $-3$ dB frequency is $75$ kHz. The filter sampling frequency has been set as the input bit-stream frequency ($F_s = 11,2896$ MHz) in order to avoid noise components (in particular the quantization noise) being folded in-band by the sampling operation. The normalized transfer function is

$$H(z^{-1}) = \frac{Z(z^{-1})}{(1 - 1.912z^{-1} + 0.916z^{-2})(1 - 0.9416z^{-1})}$$

where $Z(z^{-1})$ depends on the positions of the zeroes being properly optimized. This transfer function will be realized with a cascade of a second-order and a first-order cell, as shown in Fig. 4.

B. SC Filter Implementation

The third-order SC transfer function has been implemented with the cascade of a second-order Fleischer&Laker biquad [7] and a first-order cell, as shown in Fig. 4, in its single-ended

Typically, one zero is placed at the Nyquist frequency ($F_s/2$). In this case $Z(z^{-1})$ is given by $(1 + z^{-1})$. This solution has to be evaluated with respect to the available output swing at each opamp node, assuming unity gain at the peak. The frequency responses at each opamp node relative to this case are given in Fig. 3(a). Line I gives the amplitude frequency response up to the Nyquist frequency for the internal node of the biquad, line II refers to the output node of the biquad, and line III refers to the SC filter output node. These responses, however, must be considered in conjunction with the input quantization noise spectrum coming from the previous $\Sigma\Delta$ modulator. The total quantization noise at each opamp can be evaluated integrating from 0 to $F_s/2$ the quantization noise spectrum passed through the relative transfer function [Fig. 3(a)]. In this case, assuming the input bit-stream with levels equal to $\pm1.3$ V, the total output quantization noise at the first opamp output node is about $55$ mVrms,\(^1\) which reduces the available signal swing.

If a couple of zeroes are added at $F_s/4$, the expression of $Z(z^{-1})$ is given by

$$Z(z^{-1}) = (1 + z^{-1} + z^{-2} + z^{-3}) = (1 + z^{-1} + z^{-2})(1 + z^{-1}) = (1 + z^{-1})(1 + z^{-2})$$

The frequency responses of Fig. 3(a) are changed in the ones given in Fig. 3(b). In this case, the total quantization noise at the first opamp is reduced to $26$ mVrms. This solution does not increase the output nonquantization noise but allows the increase of, for a given opamp output swing, the possible signal amplitude.

\(^1\)Notice that for the SNR performance the noise is integrated in the signal band [20 Hz–20 kHz]. On the other hand, the evaluation of the total noise integrated in the full band (i.e., in $[0, F_s/2]$) is important to set the proper amount of output signal, for a given swing available at the opamp output node.
Fig. 5. Input branch realization: (a) complete digital-to-analog input branch and (b) SC building block realizing $C(1 + z^{-1})$.

The transfer function of this filter topology is given by

$$H(z^{-1}) = \frac{AN(z^{-1})}{(DB + DF)z^{-2} + (-2DB - DF + AC)z^{-1} + DB}$$

$$\times \frac{C1/(C1+C2)}{1 - \frac{C2}{C1+C2}z^{-1}}$$

where $N(z^{-1})$ is the input voltage-to-charge transfer function implementing $Z(z^{-1})$ as given in (2). The Fleischer&Laker biquad is used in its $F$-type configuration which is more suited for low-impedance applications, as it is with the case under development. The structure of the first-order cell has been chosen in order to improve its linearity performance.

An efficient implementation of $N(z^{-1})$ is possible if $N(z^{-1})$ is written as in the second part of (2), a part the dimension factor $C$. This is shown in Fig. 5(a), where the digital nature of the input bit steam BS has been exploited in the generation of the required additional delay blocks. In this way, in the analog section only two blocks implementing the transfer function $C(1 + z^{-1})$ are required. These blocks can be implemented as shown in Fig. 5(b). Since BS is a digital signal with high-level of analog noise, it has been used to drive the control gate of switches which toggle the input sampling capacitor between two “clean” reference voltages or $V_{REF}$. These reference voltages are generated with a resistive partition from the power supply. $V_{REF}$ is equal to 1.3 V and $V_{CM}$ is equal to 2.5 V. Notice that a negative input signal is obtained exchanging $V_{CM} + V_{REF}$ and $V_{CM} - V_{REF}$. In this way, the single-ended to fully differential conversion at the input of the SC filter can be realized by passive sampling of the input signal, without additional power consumption for extra opamps and without parasitic sensitive SC structures. The reference voltages are driven by proper buffers $B_P$, $B_N$, and $B_{CM}$ in order to reduce noise contribution and coupling between the two stereo channels. These buffers are designed with bipolar devices in order to have lower noise at the same current level than with MOS devices.
C. Noise and Distortion Reduction

The proposed smoothing filter has been designed in order to optimize noise and distortion characteristics. In order to reduce harmonic distortion, the following arrangements have been adopted [8]. The use of an SC filter allows the reduction of the distortion due to the transient behavior of the bitstream, which is quite different from an ideal square wave (i.e., with accurate wave edges). Regarding the distortion arising from opamp output node transient behavior due to limited slew-rate, we observe that there is no continuous-time path from input to output. Therefore it is important to reduce opamp-slew-rate induced distortion only at the output node and to provide a good settling for all other opamp output nodes. Therefore, in order to decrease the overall filter distortion, the particular configuration for the final first-order cell has been chosen. In fact, with this configuration, during integration phase sampling capacitor \( C_1 \) is connected in parallel with the integrating capacitor \( C_2 \). Therefore, during the integration phase, just a charge redistribution between \( C_1 \) and \( C_2 \) occurs which does not take any current from the opamp. Thus the opamp during transient is required to deliver the current only for the external load, and this reduces its slew-rate requirements. Finally, in order to reduce the distortion due to the signal-dependent charge injection, all the switches are driven with a classical eight-clock phases schedule [9]. In order to optimize SNR performance, an accurate noise evaluation has been carried out [10], [11]. Regarding the thermal noise from switches, the noise contribution from the first integrator is dominant, therefore different unit capacitance values have been used for the first and second opamp virtual ground. This results in the following capacitor values: \( A = 0.4076 \) pF, \( B = 4.364 \) pF, \( C = 1.779 \) pF, \( D = 42.90 \) pF, \( E = 0.4 \) pF, \( G = 0.8894 \) pF, \( H = 0.8894 \) pF, \( C_1 = 0.4 \) pF, \( C_2 = 7.021 \) pF. Regarding the opamp white-noise contribution, the bandwidth has been optimized for the tradeoff between large bandwidth (and good settling time but large output noise) and small bandwidth (and long settling time but small output noise). Concerning the opamp \( 1/f \) noise source, large PMOS input devices (500 \( \mu \)m/5 \( \mu \)m) have been used. Finally, the fully differential-to-single-ended (FD-to-SE) filter (implemented with an RC structure with \( R_1 = 36 \) k\( \Omega \), \( R_2 = 10 \) k\( \Omega \), \( C = 30 \) pF) performs a gain loss of 1/3.6 to be taken into account in the noise calculation. For the opamp noise, it is has been assumed to use the opamp with 60 MHz unity-gain bandwidth, 10 nV/\( \sqrt{Hz} \) white noise level, and 100 kHz 1/\( f \) noise corner frequency; these parameters correspond to the used opamp. The estimated noise contributions integrated in the band [20 Hz–20 kHz] are summarized in Table I. With a 0.8-Vp output signal amplitude, the total output noise results are sufficiently low to satisfy the SNR specifications, and therefore, the dominant 1/\( f \) noise was not cancelled.

D. Opamp Design

The scheme of the opamp used in the SC and CT filters is shown in Fig. 6 [12]. It is a two-stage BiCMOS opamp with a class AB output stage, used in order to drive the large capacitors implemented in the cell. \( V_{CMFB} \) is the common-mode voltage control generated from a dynamic common-mode feedback (CMFB) circuit. A rail-to-rail output swing is achieved in order to maximize signal amplitude and, therefore, SNR. Different opamp designs have been implemented for
the different capacitive loads and for different contributions to the total output noise. In fact, the noise of the opamp has been reduced at the cost of a higher power consumption, while for the other opamps the power consumption has been reduced. In details, the power consumption for the first, the second, and the third opamp in the SC section and the one in the CT section are 11 mW, 7 mW, 7 mW, and 7 mW, respectively. The typical performance for the first opamp (the one with the largest capacitor, i.e., $D = 42.99$ pF) with 5 V supply are: unity gain bandwidth of 60 MHz, dc-gain of 80 dB, differential output voltage swing of 8 Vpp, white noise density of 10 nV/$\text{Hz}$, and $1/f$ noise corner frequency of 100 kHz.

### III. Experimental Results

The proposed filter (embedded in a complete stereo codec structure) has been realized in a 0.7-µm BiCMOS technology. In addition to the improved driving capability and reduced noise contribution of bipolar devices, the use of a BiCMOS technology allows the achievement of a good separation between the analog and the digital section, which is entirely realized in a separate p-well [13]. Fig. 7 shows the chip photograph. The chip area for the smoothing filter is about 1.3 mm$^2$. The total power dissipation for a single filter is about only 40 mW, and the circuit can drive 20 pF and 2 kΩ load.

The output spectrum for a full-scale input sinewave in the input bit stream at 2 kHz is shown in Fig. 8. The full scale corresponds to 0.8 V output sinewave amplitude. A $-75$ dB THD is achieved. This value, in agreement with simulation results, satisfies the application requirement. The output noise power density floor is about 6.8 nV/$\text{Hz}$, and the total output noise integrated in the [20 Hz–20 kHz] band is 9 µVrms. This corresponds to an SNR of about $-96$ dB (i.e., 16 b). A good agreement with the evaluation of Table I is achieved and demonstrates the validity of the estimation. Finally, for a full-scale input sinewave in one channel at 2 kHz, the crosstalk in the other channel (which has no input signal applied) is about $-95$ dB. Table II summarizes the overall filter performance.

### IV. Conclusion

A fourth-order low-pass filter to be used in an oversampled D/A converter for stereo audio codec application is reported. The filter performs a 0.2-dB attenuation and linear phase in the band [20 Hz–20 kHz]. In a 0.7-µm BiCMOS technology, a 96 dB SNR and $-75$ dB THD have been achieved with a power consumption of only 40 mW. This makes the proposed realization competitive, in particular in terms of power consumption, with the other ones of the same kind. Even if $1/f$ noise is dominant, no $1/f$ noise cancellation scheme was adopted, and this could be an aspect for future improvement and development.

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### REFERENCES


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**TABLE II**

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<tr>
<th>DAC Smoothing Filter Performance Summary</th>
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<td>Technology</td>
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