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DTMOS-Based Low-Voltage and Low-Power Two-Stage OTA

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***Abstract*—A dynamic threshold MOS (DTMOS) based operational transconductance amplifier (OTA) with low supply voltage and low power consumption is proposed in this paper. A two-stage structure is used to achieve higher voltage gain. The proposed OTA for eliminating common-mode signals and fixing the common-mode output voltage has a feedforward and feedback paths on the first and second stage, respectively. This OTA is designed and simulated with TSMC 0.18µm CMOS technology. The operating voltage of this circuit is 0.8 V and its DC gain is 75.31 dB. The unity gain frequency (UGF) and the phase margin of this OTA are 8.40 MHz and 54°, respectively. The power consumption of the proposed OTA with a 13 pF and 100 kΩ loads at output nodes is equal to 160 µW. Based on simulation results, using the proposed DTMOS-based OTA in low voltage and low power applications is a very good option.**

Keywords—Dynamic threshold MOS (DTMOS), Low-voltage and low-power, Operational Transconductance Amplifier (OTA), Two-stage structure.

I. INTRODUCTION

Operational transconductance amplifier (OTA) is the main component of many analog circuits and has been used in many continuous time circuits and systems such as G_m-C filters, oscillators, wireless receiver networks and other applications [1]. An OTA converts differential input voltage to output current and can be modeled as a voltage controlled current source (VCVS). Due to its ability to adjust with bias current and its high speed compared to conventional operational amplifiers (Op-Amps), in many applications the use of OTA has been proposed as a preferred option. For the first time, a differential transconductor based on six CMOS inverters was proposed by Nauta [2]. It is a very powerful building block in the implementation of high frequency G_m-C filters. Since then, CMOS inverters have been used as one of the options in designing OTA-based circuits [2,3]. The modified Nauta's transconductors with multi-input floating gate transistors (MIFGT) and double CMOS pair were presented [1,4,5].

Circuits with very low power consumption without losing too much speed have always been considered by circuit designers. The need for such circuits is becoming more acute with the increasing demand for portable applications with longer battery life. Nowadays, in order to take advantage of low-scale fabrication technologies, the operation of low-voltage analog circuits has become a necessity. At the present time, the operation of analog circuits at supply voltages below 0.8 V is inevitable. However, it is difficult to use differential pairs at 0.8 V supply voltage in the conventional fully differential OTA structure. The idea of using CMOS inverters instead of differential pairs to reduce voltage performance has been proposed in the literatures [6,7]. However, CMOS inverters require $2V_{th}$ so operating at low voltages below 0.8 V may be difficult. Besides, the battery industry has not grown much in the past few years, optimizing the use of portable equipment has been one of the motivations of designers in recent years. With the electronics industry moving towards battery based portable equipment, there is an urgent need for new strategies to minimize both voltage and power parameters in these devices. As the voltage of the power supply in such circuits decreases, the operation of the circuit will undergo significant changes, which can sometimes be detrimental. Therefore, under low-voltage limitations, new topologies must be used that can maximize the operating range of the circuit and minimize power consumption without dangerously affecting on other circuit performance parameters [1].

In analog applications of CMOS inverters, the main limiting factor for low-voltage performance is the threshold voltage (V_{th}) of MOSFETs. We can lower the threshold voltage in the manufacturing process, but this method will increase the leakage current. Also, using a process with multiple threshold voltages imposes additional costs. So, we cannot simply reduce the threshold voltage. Also, this reduction in supply voltage reduces the maximum circuit speed. In order to increase the speed and reduction of power consumption, the floating gate MOS technique (FGMOS) [8]

and the dynamic threshold MOS (DTMOS) technique [9] have been suggested in the literatures.

The rest of this paper is organized as follows. In the second part of this paper, a fully differential OTA based on DTMOS inverters is introduced. In the third section, the design and simulation results of the proposed DTMOS-based OTA are presented and compared with other previous designs. Finally, a conclusion is presented in the fourth section.

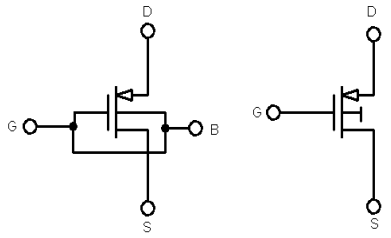
II. Proposed Design

Since the introduction of the DTMOS technique in 1994 [9,10], it is widely used in digital and analog applications and many circuit applications [11,12] have been proposed based on this design method. As shown in Fig. 1, in DTMOS technique the body and gate of the MOSFET transistor are connected to each other. It reduces the leakage current when the transistor is turned off and reduces the threshold voltage while the transistor is on to increase the overdrive voltage.

The DTMOS technique can offer several advantages over low-voltage analog circuits, although the bulk terminal of the PMOS transistor has some limitations [12]. The advantages of this technique are: lowering the threshold voltage, smaller circuit with fewer transistors and wide range of input voltages compared to the case where the signal is applied only to the gate terminal.

In the DTMOS technique, the threshold voltage is expressed as (1) and it is expected that the threshold voltage V_{th} will decrease for $V_{BS}> 0$. In (1), φ_F is the Fermi potential, γ is the coefficient of the body effect and V_{th0} is the threshold voltage at $V_{BS}= 0$. By changing the absolute value of V_{BS}, V_{th} decreases by more than 25% [13].

$$V_{th} = V_{th0} + \gamma\left[\sqrt{|2\varphi_F - V_{BS}|} - \sqrt{2|\varphi_F|}\right] \quad (1)$$



(a) (b)

Fig.1. DTMOS technique (a) equivalent circuit, (b) symbol

The structure of the proposed two-stage OTA is shown in Fig. 2. This circuit has two stage in order to achieve higher DC gain and includes the feedforward and feedback paths. In this circuit, feedforward and feedback paths have been used to limit the common-mode gain and to stabilize the common-mode output voltage. The proposed OTA for eliminating common-mode signals has a feedforward path on the first stage, and a common-mode feedback (CMFB) circuit on the second stage is provided to stabilize the common-mode output voltage [14]. The common-mode input voltage is detected using the transistors on the first stage (M5, M6, M11, M12), and after averaging, the common-mode voltage is feedforwarded to the main path using the transistors M7, M8, M13 and M14. Also, using the transistors on the output stage in the feedback path (M19, M20, M25, M26), the common-mode output voltage is detected and averaged and then feedbacked to the main signal path on the second stage (M29, M30, M31, M32). The advantage of this structure is that the differential-mode signals are not feedforwarded or feedbacked due to the averaging. Also, it is optimized for low-voltage and low-power applications using the DTMOS technique. This optimization causes that, in the case where the input signal is applied to the gate of the transistors [15], due to the lower overdrive voltage, the input voltage range in the common-mode is increased and also the bias current of the used transistors is reduced. Also, reducing the bias current of the transistors will reduce power consumption.

In [16] was suggested that NMOS inverters be used as a solution for low-voltage and low-power applications. Using of NMOS inverter, due to its class A performance, will not eliminate the differential signal in the intermediate stages, and as mentioned in [15], it is necessary to make changes in the structure of OTA, and this problem will be solved at the cost of adding very large resistors up to 220 kΩ on the output stage of the OTA. Our idea is to use DTMOS transistors in the CMOS inverter structure. The advantage of using DTMOS transistors is that they reduce the power consumption of the circuit [15] and it is not necessary to make changes to the circuit structure and increase the chip area.

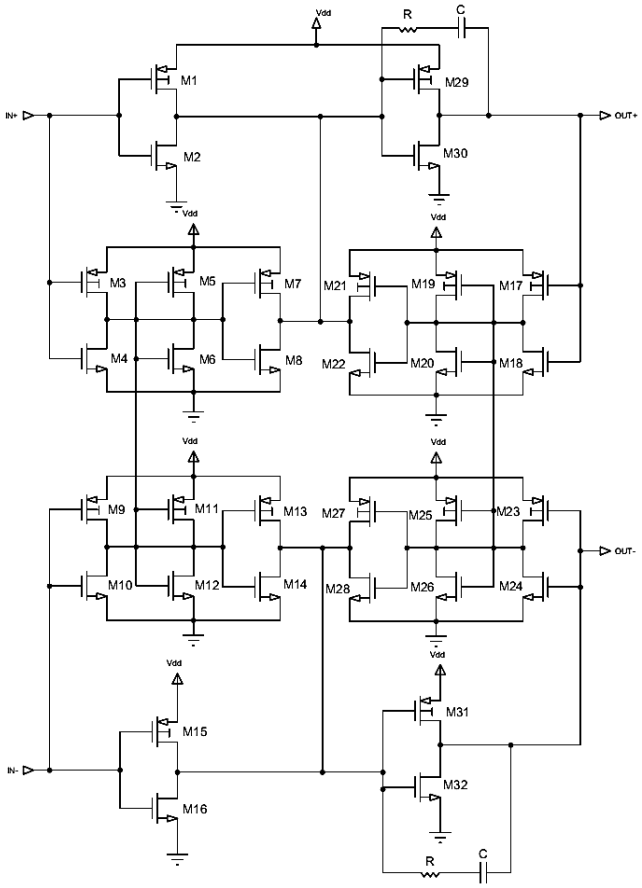


Fig.2. Schematic of the proposed two-stage OTA

The dimensions of the first stage transistors are all the same, in order to eliminate the common-mode in the first stage with a high-ratio. On the second stage, all transistors except (M29, M30, M31, M32) must have the same dimensions as the first stage transistors, and the transistors (M29, M30, M31, M32) because they have a larger output current, their dimensions are 10 times larger than the first stage transistors. Using 0.18 µm CMOS technology to design the proposed circuit, we select the aspect ratio of NMOS and PMOS transistors 6µm/1µm and 3µm/1µm, respectively.

Because the proposed structure is two-stage, we need compensation on the second stage. Fig. 2 shows the Miller compensating capacitor (C_C). The value of C_C is equal to 3pF and the value of R_C is equal to 3 KΩ.

III. Simulation Results

The DTMOS-based two-stage OTA was designed and simulated with TSMC 0.18 µm CMOS technology and 0.8 V supply voltage using HSPICE software. Fig. 3 shows the open loop gain and phase margin of the proposed OTA based on post-layout simulation. From Fig. 3, the differential-mode gain of 75.31 dB and the phase margin of 54° can be easily measured, which is improved compared to the previous design [16].

The common-mode gain of the proposed design at a frequency of 10 kHz (from Fig. 4) is -41dB. Also, the frequency response of CMRR in the proposed OTA is shown in Fig. 5. At frequencies below 1 kHz its value is equal to 116.31 dB. Fig. 6 shows the maximum output voltage swing. Each output has a swing equal to 700mV_{p-p}, which is too high for a low supply voltage, and the differential voltage swing of the proposed OTA is 1.4V.

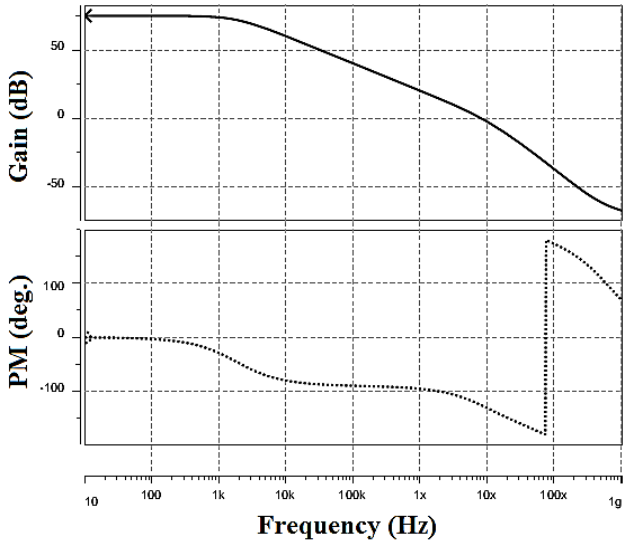


Fig.3. Open loop gain and phase margin of the proposed OTA

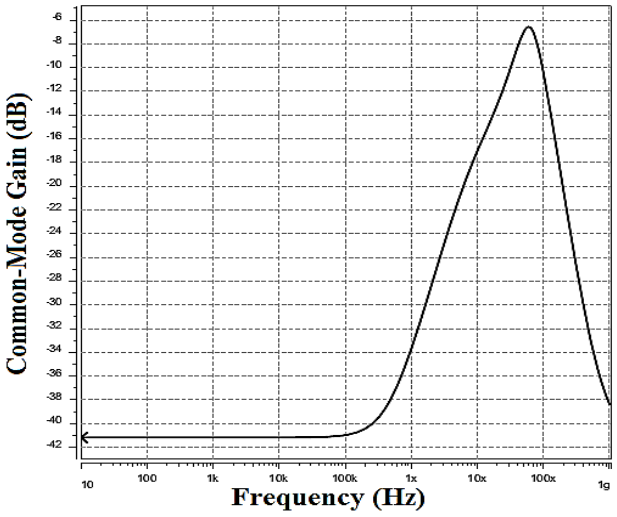


Fig.4. Frequency response of the common-mode gain of the proposed OTA

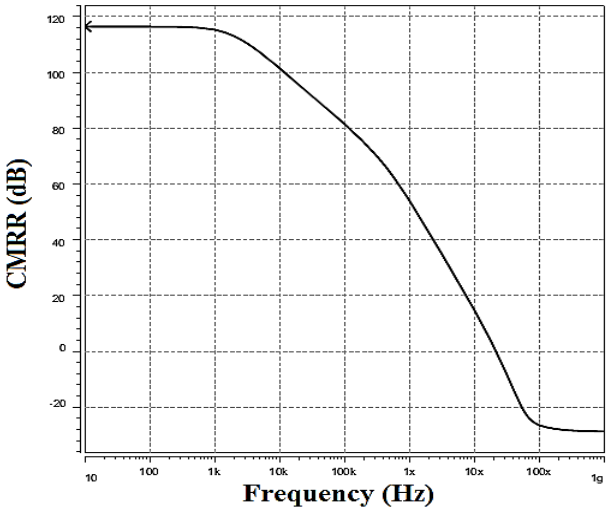


Fig.5. CMRR of the proposed OTA

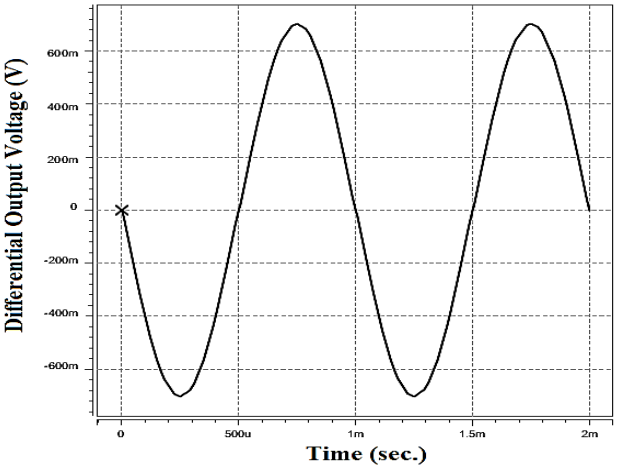


Fig.6. Output swing of the proposed OTA

Monte Carlo analysis was performed on the proposed OTA with 1000 runs, taking into account device mismatches and process variations. The result of this analysis on differential-mode gain, common-mode gain and output common-mode voltage is shown in Fig.7 to Fig.9, respectively. These results indicate that the proposed OTA is well resistant to process variations and device mismatches.

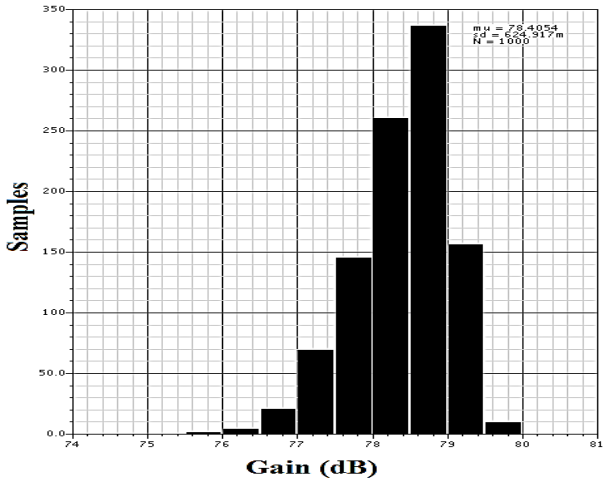


Fig.7. Monte Carlo simulation of the DC gain of the proposed OTA for 1000 samples

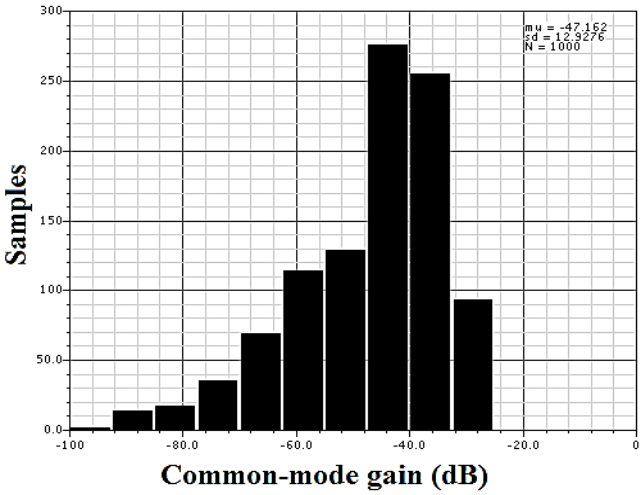


Fig.8. Monte Carlo simulation of the common-mode gain of the proposed OTA for 1000 samples

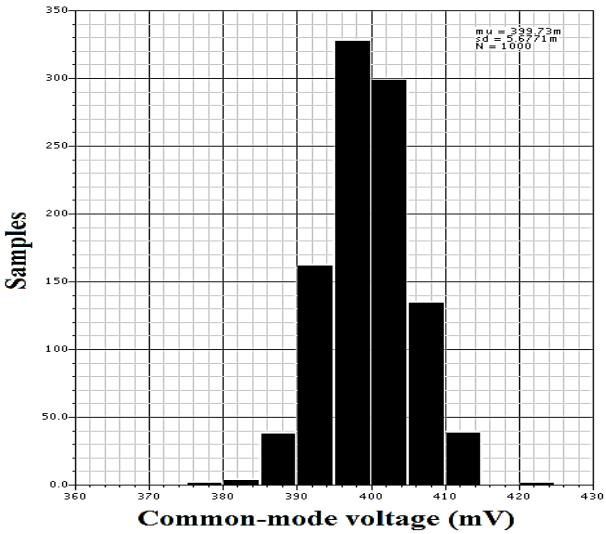


Fig.9. Monte Carlo simulation of the output common-mode voltage of the proposed OTA for 1000 samples

The simulation results are summarized in Table I and the results indicate the appropriateness of our proposed design. It is worth noting that in Table I we present the post-layout simulation results of our proposed design.

To evaluate this work and compare it fairly with other previous works, a figure of merit (FOM) can be defined as follows:

$$\text{FOM} = \frac{\text{Gain}\ (dB)\times\text{UGF(MHz)}}{Supply\ Voltage\ (V)\times Power(mW)} \qquad (2)$$

Based on this FOM, it is observed that the proposed design has the best FOM among the other designs reported in Table I.

The proposed OTA layout using the Cadence IC Design software is shown in Fig.10. The size of this chip is 152.43 µm×178.77 µm, which leads to a chip area of 0.027mm^2.

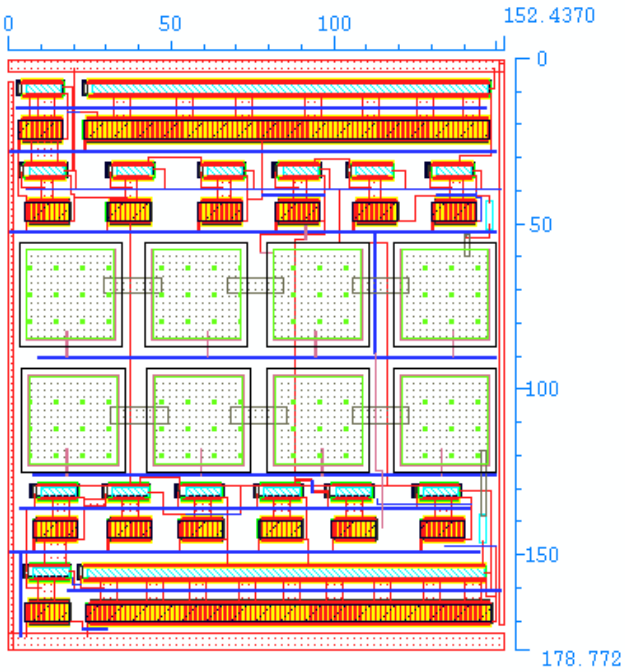


Fig.10. Layout of the proposed OTA

TABLE I. PROPOSED OTA SIMULATION RESULTS AND COMPARISON WITH PREVIOUS DESIGNS

	[9]	[16]	[17]	[18]	[19]	This work
Tech. (µm)	0.18	0.18	0.18	0.5	0.18	0.18
Supply Voltage (V)	1	1.0	1.8	±1	±0.9	0.8
Power (mW)	0.118	0.17	11.90	0.12	0.072	0.16
Gain (dB)	50	42	79	81.7	77	75.31
UGF (MHz)	8.82	9	86.5	4.75	2.65	8.4
PM (deg.)	45	52	50	60	86	54
CMMR (dB)	73.8	75	-	78	-	116.31
PSRR+ (dB)	-	-	-	72	-	76
PSRR- (dB)	-	-	-	74	-	75
SR+ (V/µs)	-	-	74.1	9.8	43.1	7.43
SR- (V/µs)	-	-	-	7.6	-	12
Input ref. noise ($nV/\sqrt{Hz}$)	-	-	0.8	35	-	20
C_L (pF)	13	13	200	70	25	13
FOM ($\frac{dB\times MHz}{V\times mW}$)	3717	2223	319	1616	1574	4942

IV. CONCLUSION

In this paper, a modified two-stage OTA based on the DTMOS technique is presented. The proposed design was simulated with TSMC 0.18 µm CMOS technology and using DTMOS transistors in the structure of this design, the supply voltage and power consumption were reduced to 0.8 V and 160 µW, respectively. The differential-mode gain and the unity gain bandwidth are 75.31 dB and 8.4 MHz, respectively, and the phase margin is 54°. Due to the DTMOS inverter being class AB, there is no need to change the structure of OTA and add large resistors in the output stage. Therefore, the proposed circuit is expected to take up less chip area.

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