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Investigation of Different Combinations of CNTFET and MOSFET In the Structure of a Hybrid Ring Oscillator

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***Abstract*—In this paper, several carbon nanotube field effect (CNTFET) and MOSFET based hybrid ring oscillators are presented. In these designs, both the advantages of high frequency performance without compromising on power consumption and the capabilities of the CNTFET have been used. Studies on a three-stage ring oscillator have shown that the location of inverters based on CNTFET and MOSFET can have a significant effect on the oscillation frequency of a three-stage ring oscillator. Based on the simulations and the results obtained in the technology of 32 nm and the supply voltage of 0.8 V, the oscillation frequency of these designs are in the range of several GHz and in terms of the power delay product (PDP) is in the range of several tens of aJ. PDP of the proposed designs are extremely low compared to up-to-date advanced techniques, which makes these designs very suitable for low power and high frequency applications.**

Keywords—Hybrid Ring Oscillator, Carbon Nanotube Field Effect Transistor (CNTFET), Low Power, Power Delay Product (PDP).

I. INTRODUCTION

Nowadays, with the pervasiveness of portable electronic equipment, the production of high-performance reference clock signals with low power consumption has become one of the most important requirements in the design of electronic circuits. The generated signals are essential for both digital and analog systems, and telecommunications standards are one of the most common uses for these signals. A clock generator circuit, regardless of whether the clock signal is designed for analog or digital applications, must ensure that the correct and flawless operating speed is guaranteed for the devices that use it. In addition, nowadays, due to the requirements of portable devices, the clock signal must be adjusted over a wide range of frequency bands. This requires a voltage controlled oscillator (VCO) and a phase locked loop (PLL).

LC oscillators and CMOS ring oscillators are two common types of VCOs that have been widely introduced and used in the literature. Because the combination of inductor and capacitor in LC oscillators leads to a large area of the chip, CMOS ring oscillators are preferred. The advantages of ring oscillators include no need for an on-chip inductor, ease of output frequency control, flexibility of on-chip integration, and a wide adjustment range.

As technology scales down, low-power ring oscillators with low-energy consumption are essential for many applications, including various cellular communication systems, RFID tags, wireless sensor networks, and medical circuits and systems. Many research has been done to address the low power requirements of a ring oscillator. The most common low-power techniques presented in the papers for the ring oscillator are summarized as the current-starving (CS) technique [1], the use of sub-threshold transistors [2], the use of controllable digital switches [3], the negative skewed delay (NSD) technique [4], combining two CS and NSD techniques in a single circuit [5], adding a reverse phase feedback inverter to a node of the main inverter [6] and frequency multiplication using sub-harmonic current injection [7]. However, since power is directly proportional to the oscillation frequency, these methods compromise with power consumption and still do not show significant improvement in terms of power delay product (PDP).

CMOS technology faces significant challenges at the nanoscale regime due to a number of factors. To preserve Moore's Law, we must now look for alternatives, such as carbon nanotube field-effect transistors (CNTFETs), which have gained much prominence in recent years as a promising alternative to silicon CMOS in digital integrated circuits. Carbon nanotubes (CNTs) are a promising material for electronic devices that have many

applications in digital circuits such as arithmetic circuits, full adders, subtractors and memory cells [8,9] and there is the ability to combine MOSFET and CNTFET to improve performance for digital or analog design [10,11].

To answer the above challenges, in this paper, several high frequency and low power ring oscillators with a combination of MOSFET and CNTFET are proposed to take advantage of high frequency performance without compromising on power consumption and carbon nanotube field effect transistor capabilities. This paper is organized as follows: The basic structure and features for CNTFETs are discussed in Section 2. Section 3 shows the design of the proposed circuits and their operating principles. Section 4 presents the simulation results and their analysis. Section 5 concludes with a concluding remarks.

II. Overview of CNTFET

Single-walled carbon nanotube (SWCNT) is considered as a sheet of graphite wrapped and packed along the chiral vector [12]. The chiral number is considered as a vector (n_1, n_2) and depending on the value of this vector, SWCNTs are classified into three groups as follows:

$$\begin{cases} if\ n_1 = 0\ or\ n_2 = 0 \Rightarrow zigzag\ nanotube \\ if\ n_1 = n_2 \Rightarrow \text{armchair}\ nanotube \\ if\ n_1 \neq n_2 \neq 0 \Rightarrow \text{chiral}\ nanotube \end{cases} \quad (1)$$

When the relationship between two indices (n_1, n_2) for an integer i is $n_2 - n_1 \neq 3i$, SWCNT will have a semiconductor property and can be used as a channel between the source and the drain of MOSFET [13]. CNTFET is a MOSFET transistor made of SWCNT. CNTFET can be a good alternative to silicon-based transistors due to its unique properties, and its principles of operation is similar to conventional silicon counterparts. Depending on the operating mechanism, CNTFET-like MOSFET (C-CNTFET), Schottky barrier CNTFET (SB-CNFET), tunneling CNTFET (T-CNTFET) and double-gate CNTFET (DG-CNTFET) belong to the CNTFET family [14-16].

Due to the similarity between MOSFET and C-CNTFET in terms of performance and features, we will use this type of CNTFET in the design of our proposed ring oscillator circuits. The structure of a C-CNTFET device is shown in Fig. 1, where the distance between two adjacent centers of a carbon nanotube under the same gate of a C-CNTFET is called a pitch. The pitch value directly affects the gate width (W_g) and its contacts. The total size of the C-CNTFET can be determined by setting the minimum gate width (W_{min}) and number of tubes (N) as follows:

$$W_g = \text{Max}(W_{min}, N \cdot \text{pitch}) \quad (2)$$

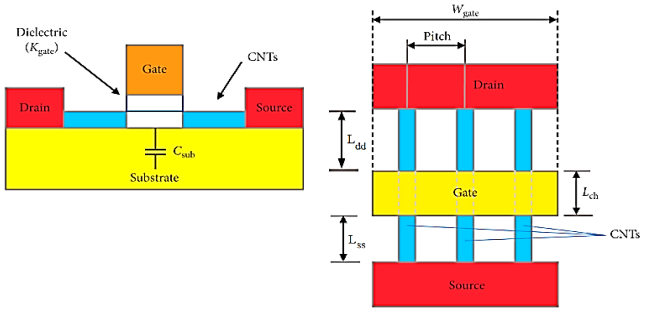

Fig. 1. Structure of a C-CNTFET [8]

Given the effect of threshold voltage on switching speed, current consumption and leakage power, determining the threshold voltage (V_{th}) to design a circuit with the best performance in terms of average power consumption and speed is very important. For a SWCNT with chirality (n_1, n_2), the threshold voltage is inversely related to the diameter of the carbon nanotube (D_{CNT}), which is determined as follows:

$$V_{th} = \frac{0.43}{D_{CNT}} = \frac{0.43}{0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2}} = 5.491(n_1^2 + n_1 n_2 + n_2^2)^{-1/2} \quad (3)$$

III. Peoposed Design

A ring oscillator consists of delay stages where the output of the last stage returns to the input of the first stage. A conventional ring oscillator in a feedback loop consists of an individual number of inverter cells connected in series. The schematic of a three-stage ring oscillator, which will be examined in this paper, is shown in Fig. 2. In this circuit, the output parasitic capacitor consisting of the gate capacitor of the transistors in each subsequent stage is discharged through the P-type transistor on the V_{dd} rail in half cycle and in the next half cycle this parasitic capacitor is discharged through the N-type transistor on the GND rail. Therefore, continuous charging and discharging of the capacitor in each cycle leads to oscillations and the frequency of the ring oscillator is determined by (4). Here, n is the number of stages and t_d is the delay of each stage. By changing the current passing through the inverter, t_d changes and as a result the oscillation frequency changes. This current is determined by the aspect ratio of both P-type and N-type transistors in the inverter stage.

$$f = \frac{1}{2 \times n \times t_d} \quad (4)$$

In a ring oscillator, the dynamic power dissipation ($P_{dynamic}$) is determined by (5). In (5), C_L is the sum of the output load capacitors in each inverter stage, V_{dd} is the oscillator supply voltage and f is the oscillation frequency. According to (5), it is clear that power consumption is directly proportional to frequency. So that lower frequency leads to lower power consumption and vice versa. Therefore, the architecture of the ring oscillator needs to be further modified to ensure low power consumption and at the same time operate at higher frequencies.

$$P_{dynamic} = C_L \times V_{dd}^2 \times f \quad (5)$$

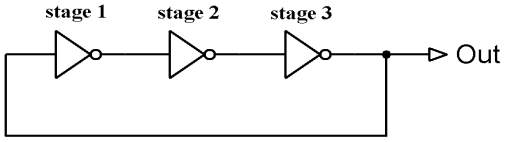

Fig. 2. Block diagram of 3-stage ring oscillator

In this paper, we examine different combinations for first to third-stage inverters. In previous work reviewed in the articles, inverters have been implemented either entirely with MOSFET or with CNTFET. We will consider different combinations for these inverters here with a combination of MOSFET and CNTFET. Table I shows the different combinations for the inverters used in the structure of the three-stage ring oscillator.

TABLE I. DIFFERENT COMBINATIONS FOR INVERTERS USED IN THE STRUCTURE OF A THREE-STAGE RING OSCILLATOR

Structure	Stage 1	Stage 2	Stage 3
Design 1	MOSFET	CNTFET	MOSFET
Design 2	CNTFET	MOSFET	CNTFET
Design 3	CNTFET	CNTFET	MOSFET
Design 4	MOSFET	MOSFET	CNTFET

In the proposed design 1, the first-stage inverter is considered entirely with MOSFET, the second-stage inverter is considered entirely with CNTFET, and the third-stage inverter is considered entirely with MOSFET. Fig. 3 shows a schematic of the proposed design 1.

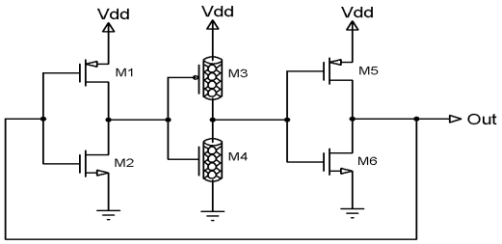

Fig. 3. Proposed design 1 for a 3-stage ring oscillator

In the proposed design 2, the first-stage inverter is considered entirely with CNTFET, the second-stage inverter is considered entirely with MOSFET, and the third-stage inverter is considered entirely with CNTFET. Fig. 4 shows a schematic of the proposed design 2.

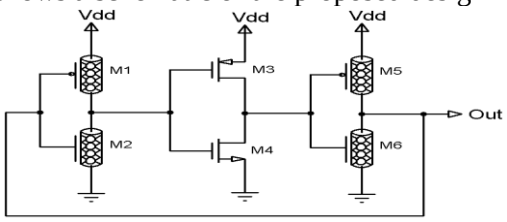

Fig. 4. Proposed design 2 for a 3-stage ring oscillator

In the proposed design 3, the first- stage inverter is considered entirely with CNTFET, the second-stage inverter is considered entirely with CNTFET, and the third-stage inverter is considered entirely with MOSFET. Fig. 5 shows a schematic of the proposed design 3.

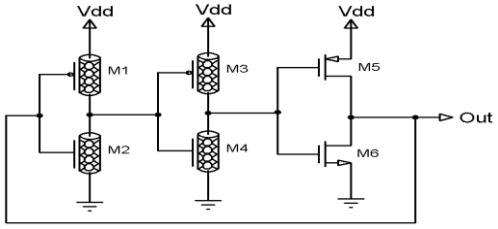

Fig. 5. Proposed design 3 for a 3-stage ring oscillator

In the proposed design 4, the first- stage inverter is considered entirely with MOSFET, the second-stage inverter is considered entirely with MOSFET, and the third-stage inverter is considered entirely with CNTFET. Fig. 6 shows a schematic of the proposed design 4.

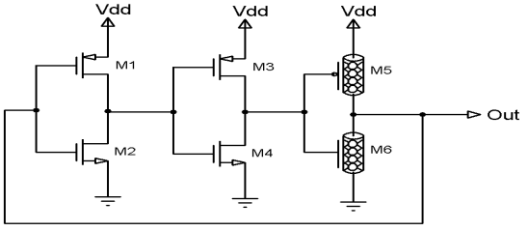

Fig. 6. Proposed design 4 for a 3-stage ring oscillator

IV. SIMULATION RESULTS

The proposed circuits were simulated with a 32 nm model for CNTFET and 32 nm technology for MOSFET with a supply voltage of 0.8 V and Hspice software. In order to achieve high performance speeds while maintaining low power consumption, the whole paper was considered the same size for all proposed designs for MOSFETs and CNTFETs to ensure similar working conditions for a fair comparison. For better comparison, PDP is considered as an energy measure, which is defined as $P_{avg} \times t_d$, where P_{avg} is average power consumption and t_d is gate delay. For low power applications, the PDP value is considered as a figure of merit (FOM) that should be

minimized. For a ring oscillator, this criterion is determined as follows:

$$PDP = P_{avg} \times t_d = \frac{P_{avg}}{2 \times n \times f} \quad (6)$$

where n is the number of stages and f is the oscillation frequency.

For a fairer comparison, we simulated all the proposed circuits under the same conditions at a supply voltage of 0.8 V, and the performance of the proposed circuits in Table 1 is compared at room temperature. According to the results shown in Table 1, it can be seen that among the four proposed designs, the highest frequency belongs to proposed design 3, in terms of power consumption, low power consumption belongs to proposed design 4 and the lowest PDP belongs to proposed design 4.

TABLE II. COMPARISON OF THE PROPOSED 3-STAGE RING OSCILLATORS

Design	V_{dd} (V)	f_{osc} (GHz)	Power (µW)	PDP (aJ)
Propsed Design 1	0.8	6.392	2.872	74.89
Propsed Design 2	0.8	20.093	4.973	41.25
Propsed Design 3	0.8	**22.339**	3.917	29.22
Propsed Design 4	0.8	5.856	**2.859**	**81.39**

The performance of the proposed schemes is compared with other work related to the low power schemes proposed in the articles in Table II. As can be seen, the current study has shown improved performance compared to new and up-to-date research.

TABLE III. COMPARISON OF PROPOSED DESIGNS WITH OTHER PREVIOUS WORKS

Design	Technology	V_{dd} (V)	PDP (fJ)
[1]	180nm CMOS	1.8	728.33
[3]	180nm CMOS	1.8	261.81
[4]	0.35µm CMOS	3	1250
[7]	0.8µm CMOS	5	2078.74
[8]	65nm CMOS	1	0.65
[9]	180nm CMOS	1.8	228.92
[10]	180nm CMOS	1.8	8.33
[17]	130nm CMOS	1.2	53.16
[18]	65nm CMOS	1	49
[19]	180nm CMOS	1.2	1000
Proposed Design 1	32nm CMOS-CNTFET	0.8	**0.07489**
Proposed Design 2	32nm CMOS-CNTFET	0.8	**0.04125**
Proposed Design 3	32nm CMOS-CNTFET	0.8	**0.02922**
Proposed Design 4	32nm CMOS-CNTFET	0.8	**0.08139**

The supply voltage change-dependent behaviors in the proposed 3-stage ring oscillators under the same conditions are compared in Fig. 7. Here, it can be seen that by changing the supply voltage in the range of 0.7 V to 0.9 V, the oscillation frequency of the first proposed design changes in the range of 5.85 GHz to 6.95 GHz, the oscillation frequency of the second proposed design changes in the range 18.70 GHz to 21.90 GHz, oscillation frequency of the third proposed design changes in the range of 22.30 GHz to 25.80 GHz, oscillation frequency of the fourth proposed design changes in the range of 5.30 GHz to 6.17 GHz.

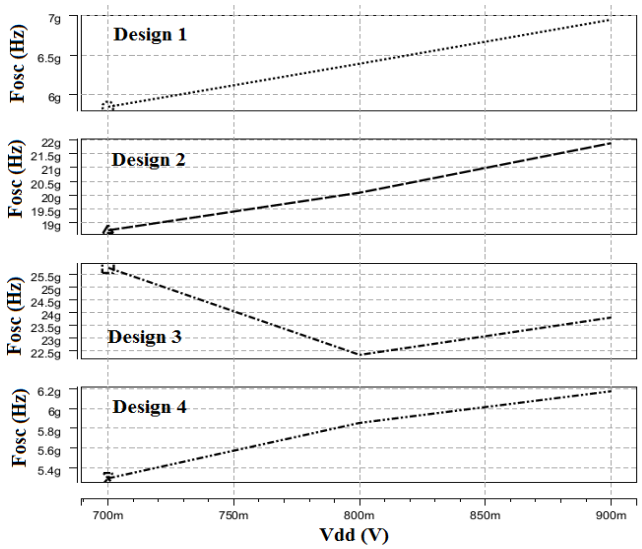

Fig. 7. Oscillation frequency variation in terms of supply voltage change for different structures of the proposed 3-stage ring oscillator

V. CONCLUSION

In this paper, a hybrid 3-stage ring oscillator was proposed, which was a combination of silicon MOSFET and CNTFET. Four hybrid structures were evaluated and it was observed that different positions of inverters based on MOSFET and CNTFET can have a significant effect on the oscillation frequency of the three-stage ring oscillator. Based on the simulation results, it was observed that among the four proposed designs, the highest oscillation frequency belongs to the proposed design 3, in terms of power consumption, the proposed design 4 is low consumption and the lowest PDP belongs to the proposed design 4. Very high oscillation frequency with low power consumption was obtained in the proposed designs. Comparing the four proposed designs with other modern designs, it was observed that our proposed circuits can find potential applications in high frequency systems and other low power applications.

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