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Hybrid CMOS-SET Inverter Design for Improved Performance using Tied Body-backgate Technique

Prashant Gupta, Shashank Kumar Ranu, Manish Kumar Pandey*, Aminul Islam
Department of Electronics and Communication Engineering, Birla Institute of Technology (Deemed University), Mesra, Ranchi, Jharkhand, India

Abstract

Single-electron transistors (SETs) are an attractive candidate for future functional elements in LSIs, because of their low-power consumption and small size. Integration of current CMOS technology with the emerging SET devices is an effective approach for improving density of integration in VLSI chips and ensuring ultra low power dissipation along with the advantages of CMOS technology like high gain, current drive, speed and matured fabrication technology. This paper investigates hybrid CMOS-SET-based inverter for its functionality and performance. It then proposes and analyzes the effect of tied body-backgate technique on design metrics (propagation delay and power-delay product (PDP)). The proposed technique offers 2.38× and 4.09× improvement in propagation delay and power-delay product, respectively.

Keywords: *CMOS, single electron transistors, propagation delay, power delay product*

****Author for Correspondence*** E-mail: manish1468.11@bitmesra.ac.in

INTRODUCTION

Aggressive scaling of CMOS devices in deep nanoscale regime has led to increased subthreshold leakage, gate oxide leakage and transistor performance variability. Quantum mechanical effects are effective in these small structured devices thereby making it necessary to introduce new nanoscale structures which utilize these effects to provide functionalities which are unattainable with CMOS. Single electron transistor (SET) is one of such emerging nanoelectronics technologies. Single electron circuits have nano-feature size and ultralow-power consumption making them suitable for logic and memory circuits.

SET is based on the physical principle of quantum tunneling. It operates by controlling the flow of charge to and from an "island" *via* two tunnel junctions. The SET properties are determined by quantum mechanical properties of matter which add characteristics, such as coulomb oscillation, coulomb blockade, etc., to the devices. These characteristics of SET devices make it a promising candidate for nanoelectronics applications, such as sensitive electrometers [1], thermometers [2], and turnstiles, for current standards [3], [4] and quantum bits for quantum information processing [5–7]. However, SET has certain disadvantages, such as low current drivability, extremely low temperature operation, low voltage gain, background charge effect, premature fabrication technology etc.

Integration of current CMOS technology with the emerging SET devices is an effective approach to overcome the disadvantages of SET and challenges of scaling of CMOS in sub-45 nm regime. Hybrid CMOS-SET circuits combine the advantages of CMOS technology like high gain, current drive, speed and matured fabrication technology with SET advantages like sub-10 nm scale feature size, unique Coulomb blockade, oscillation characteristics and ultralow-power dissipation.

In view of the above, this paper makes the following contributions:

1) It investigates hybrid CMOS-SET inverter circuit for its functionality.
2) It then proposes a Tied Body-Backgate (TBB) inverter circuit which offers better performance in terms of design metrics such as delay (t_p) and power-delay product (*PDP*).

Extensive simulations of Hybrid CMOS-SET based gates were carried on HSPICE using 16 nm PTM (developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University (ASU) [8] and analytical SET model for SPICE simulation [9].

The remainder of this paper is organized as follows. SET structure is briefly reviewed in Section II. Section III presents brief discussion on Hybrid CMOS-SET based circuits. Section IV describes the simulation setup for estimation of design metrics. Simulation results are discussed and compared in Section V. Finally, the conclusion of the paper appears in Section VI.

SET STRUCTURE AND OPERATION

A SET device typically consists of a quantum dot (traditionally called island) connected to source and drain contacts through high resistance tunnel junctions (Figure 1(a)).

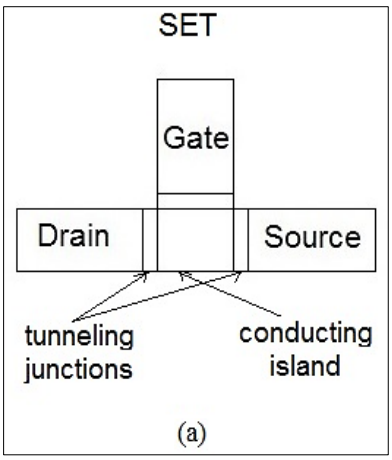

Fig. 1(a): *Simplified Structure of SET.*

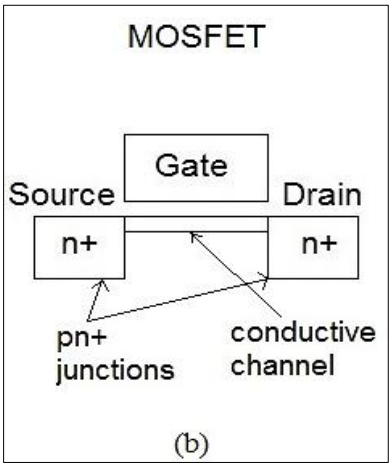

Fig. 1(b): *Compared with MOSFET.*

"The fundamental physical principle of SET is the tunneling effect which is an intrinsically quantum mechanical phenomenon. As per classical physics, an electron cannot tunnel through a junction having potential greater than the energy of electron. However, in quantum world, when the size of junction becomes very small, electrons can tunnel through such junctions as a consequence of wave particle duality of matter and Heisenberg uncertainty principle. Minimum voltage across the tunnel junction, required for tunneling of one electron through that junction is termed as the critical voltage *Vc*, which can be calculated from [10]

$$V_c = \frac{e}{2(C_e + C_t)} \quad (1)$$

where C_t is tunneling junction capacitance and C_e is equivalent capacitance of the circuit (C_e) as viewed from the tunnel junction's perspective. Tunneling event does not occur for voltages less than the critical voltage.

The island is initially electro-neutral, i.e., has equal number of electrons and protons in its crystal lattice. The electric field generated by the island in neutral state is negligible beyond its border, thereby making the probability of tunneling of an electron through the barrier greater than zero.

The tunneling of an electron through the junction imparts a net charge Q equal to $-e$ (charge of a single island) to the otherwise neutral island. The tunneled electron increases the electrostatic energy (E_c) of the island which if given by

$$E_c = \frac{e^2}{2C} \quad (2)$$

where C is the effective capacitance of the island. Electrostatic energy E_c is very high due to extremely small value of capacitance (< 3 aF) in nanoscale structures. The high E_c prevents further tunneling of electrons across the junction.

This phenomenon is known as "Coulomb Blockade" and E_c is termed as Coulomb charging energy or Coulomb blockade energy. For SET operations electrons have to tunnel through the junction from the source to the drain *via* the central island. In order for tunneling to happen, it is required that the

charging energy E_c should be greater than the thermal energy and also the tunneling resistance R_T, should be greater than the resistance quantum h/e^2. Therefore, the conditions for observing single electron phenomenon can be expressed as

$$\frac{e^2}{C} > K_B T \tag{3}$$

and,

$$R_T >> \frac{h}{2\pi e^2} = 25813\Omega \tag{4a}$$

where e is electronic charge, h is Planck's constant, K_B is Boltzmann's constant, C is the capacitance of the central island and T is the temperature.

SET can function as a switch by going into the Coulomb blockade state (OFF condition) and conducting the current through tunneling mechanism (ON condition), thereby making it possible to mimic MOSFET logic architecture and development of hybrid CMOS-SET logic family.

The simplified structure of SET (Figure 1a) is compared with that of a MOSFET (Figure 1b). The SET device resembles a MOSFET with 'drain', 'gate' and 'source' terminal.

However, SET contains a small conducting island (quantum dot) between drain and source and tunnel junctions instead of the usual inversion channel and p-n junctions found in MOSFETs.

HYBRID CMOS-SET INVERTER

Hybrid CMOS-SET architecture, which combines the advantages of CMOS and single electron transistor devices, is a promising practical implementation of nanoscale logic circuit design.

In this work, inverter based on hybrid CMOS-SET logic is analyzed. The architecture utilizes the PMOS network as the pull-up network (PUN) and SET network as the pull-down network (PDN) (Figure 2).

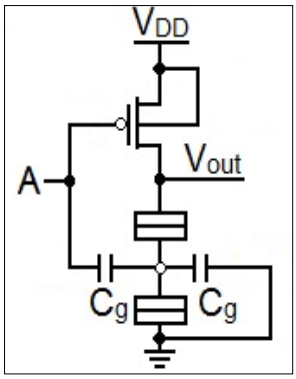

Fig. 2: *Design of a Hybrid CMOS-SET Inverter Using SET and PMOS. (In this figure, body of the PMOS is tied to V_{DD} and the backgate of the SET is tied to 0 V. A is the input voltage signal and V_{out} is the output voltage signal. C_g represents the gate capacitances while V_{DD} denotes the power supply.)*

TIED BODY-BACKGATE HYBRID CMOS-SET INVERTER

The hybrid CMOS-SET based circuits work analogously with CMOS counterparts since the PMOS networks form the pull-up network and SET network forms the pull-down network. The back-gate of SET is a metallic "island" containing large number of free electrons. In Tied Body-Backgate Hybrid CMOS-SET (TBB HCS) inverter (Figure 3), the body of PMOS is connected to the backgate of the SET (when A = 0 or A = V_{DD}). Forward body bias will result in reduction in threshold voltage (V_{th}) as per the expression:

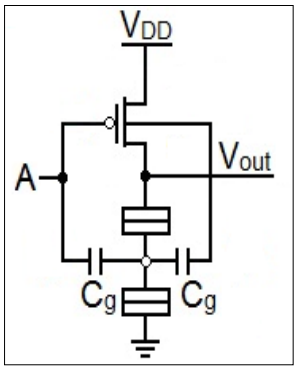

Fig. 3: *Design of the Proposed Hybrid SET-MOS Inverter. (In this figure, body of the PMOS is tied to the backgate of the SET. A is the input voltage signal and V_{out} is the output voltage signal. C_g represents the gate capacitances while V_{DD} denotes the power supply).*

Table 1: *SET Parameters.*

Parameter	Value
Gate capacitance (C_g)	1aF
Drain capacitance (C_d)	1aF
Source capacitance (C_s)	1aF
Backgate capacitance (C_b)	0.1aF
Drain resistance (R_d)	1MΩ
Source resistance (R_s)	1MΩ

$$V_{th} = V_{t0} + \gamma(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}) \quad (4b)$$

where V_{t0} is the V_{th} for V_{bs} = 0; is a physical parameter with 2^{φ_f} typically 0.6 V; γ is a fabrication-process parameter given by:

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_D}}{C_{ox}} \quad (5)$$

where, q is electronic charge, N_D is the doping concentration of the n-type substrate and ε_s is the permittivity of silicon. The reduced V_t increases the drain current, thereby improving the drivability and propagation delay of the inverter (Figure 3). Since the leakage current is the result of transport of electrons from the island of the SET to the body of the PMOS, the consequent current and hence power drawn from the voltage source is reduced.

SIMULATION SETUP

The design metrics propagation delay and power-delay product (t_p, *PDP*) of the circuit were estimated using HSPICE. The supply voltage was varied from 0.35 V to 0.60 V to cover the subthreshold, near-subthreshold and super threshold region of operation for the PMOS. The values for various SET parameters used are mentioned in Table 1. The simulations were performed at room temperature i.e., 25 °C. The (*W/L*) ratio for the PMOS was fixed at 32 nm/16 nm (2:1). The nominal threshold voltage (V_{th}) for PMOS is set at −0.43 V.

SIMULATION RESULTS AND DISCUSSION

In this section, proposed circuit (Figure 3) is compared with its counterpart inverter circuit (Figure 2) in terms of design metrics such as t_p, *PDP* (Tables 2 and 3). Figure 4 provides the output signals from the Hybrid CMOS-SET inverter and the proposed Tied Body-Backgate technique based Hybrid CMOS-SET inverter. The proposed design exhibits less noise during t_{LOW} (time during which signal remains at lower rail voltage). Figures 5 and 6 provide the graphical representation of the estimated data. As seen from the tables the proposed circuit provides on an average 2.38× and 4.09× improvement in propagation delay and power-delay product respectively.

The estimated design metrics prove the improvement in circuit performance using Tied Body-Backgate technique.

Table 2: *Supply Voltage V_{DD} (V).*

Supply Voltage V_{DD}	Propagation Delay (ps)	
	HCS	TBB HCS
0.35	8.92	2.33
0.40	11.2	2.47
0.45	11.0	5.78
0.50	10.2	3.79
0.55	9.95	3.51
0.60	9.42	2.28

Table 3: *Supply Voltage V_{DD} (V).*

Supply Voltage V_{DD}	Power Delay-Product (J) ($x10^{-19}$)	
	HCS	TBB HCS
0.35	4.10	1.14
0.40	7.25	1.81
0.45	9.56	4.27
0.50	11.4	4.14
0.55	13.8	4.72
0.60	14.8	3.74

CONCLUSION

This paper successfully investigates Hybrid CMOS-SET-based inverter circuit for its performance. It also proposes Tied Body-Backgate technique to enhance the performance of Hybrid CMOS-SET inverter circuit in terms of design metrics (t_p, *PDP*). This improved hybrid structure combines the advantages of both CMOS and SET technology in a improved approach thereby making single electron transistor a promising nanoscale structure in post CMOS VLSI era.

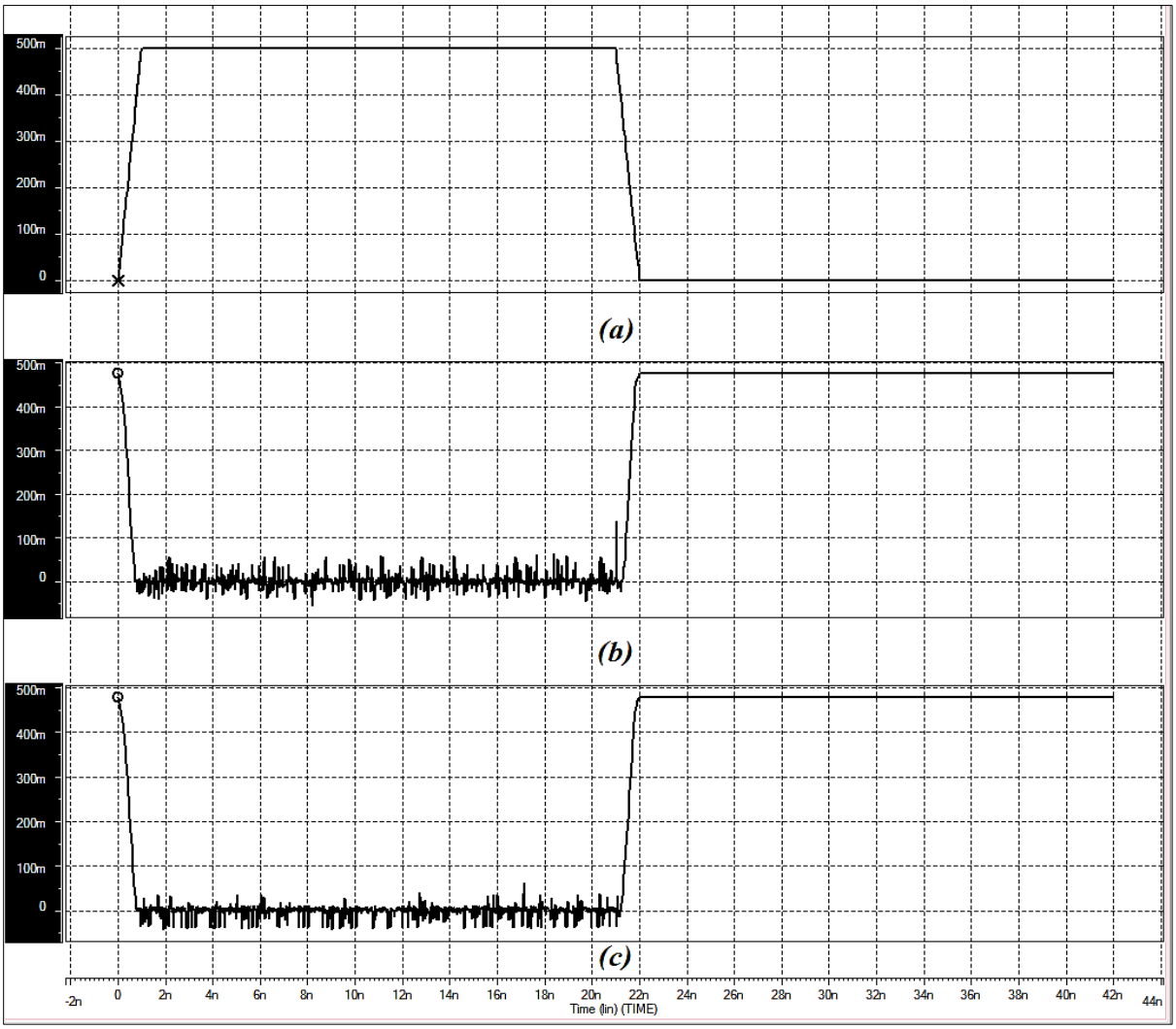

Fig. 4: *(a) Is the Input Signal. (b) and (c) Are the HCS and TBB HCS Inverter Output Signal Respectively.*

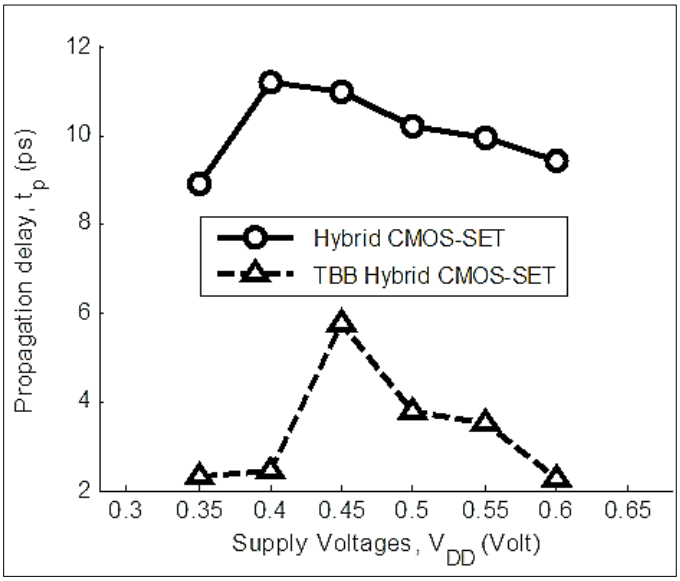

Fig. 5: *Propagation Delay of Hybrid CMOS-SET Inverter and TBB Hybrid CMOS-SET Inverter versus Supply Voltage (V_{DD}).*

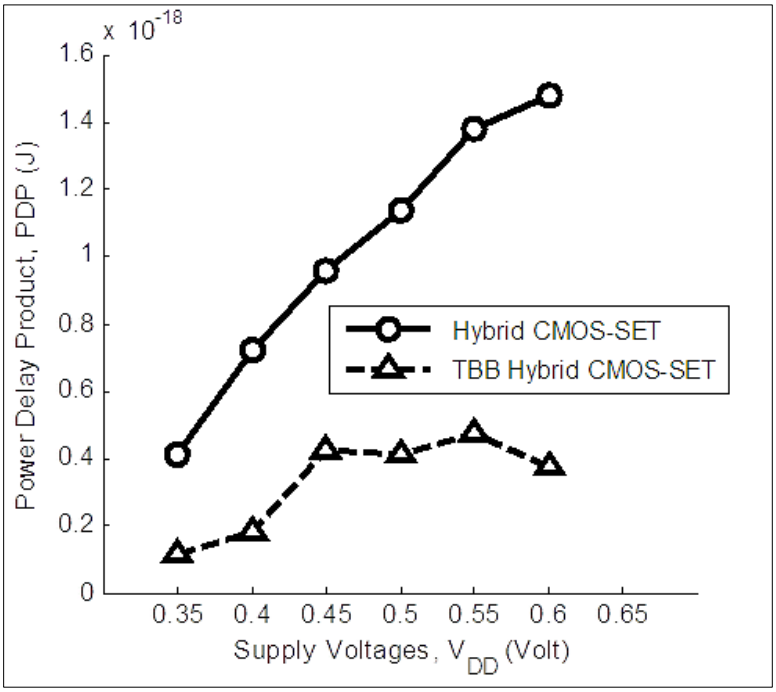

Fig. 6: *Power-Delay Product of Hybrid CMOS-SET Inverter and TBB Hybrid CMOS-SET Inverter versus Supply Voltage (V_{DD}).*

REFERENCES

1. Schoelkopf RJ, Wahlgren P, Kozhevnikov AA, Delsing P, Prober DE. The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer. *Science*. May 1998; 280(5367): 1238–42p.
2. Pekola JP, Hirvi KP, Kauppinen JP, Paalanen MA. Thermometry by arrays of tunnel junctions. *Phys. Rev Lett.* Nov. 1994; 73(21): 2903–6p.
3. Gallop J. The quantum electrical triangle. *Philos. Trans. Roy. Soc. A.* Sept. 2005; 363(1834): 2221–47p.
4. Zimmerman NZ, Keller MW. Electrical metrology with single electrons. *Meas. Sci. Technol.* Aug. 2003; 14(8): 1237–42p.
5. Fujisawa T, Hayashi T, Sasaki S. Time-dependent single electron transport through quantum dots. *Rep. Prog. Phys.* Mar. 2006; 69(3): 759–96p.
6. Hanson R, Kouwenhoven LP, Petta JR, Tarucha S, Vandersypen LMK. Spins in few-electron quantum dots. *Rev. Mod. Phys.* Oct. 2007; 79(4): 1217–65p.
7. Morton JJL, McCamey DR, Eriksson MA, Lyon SA. Embracing the quantum limit in silicon computing. *Nature.* Nov. 2011; 479(7373): 345–53p.
8. Nanoscale Integration and Modeling (NIMO) Group, Arizona State University (ASU). (Online). Available: http:// ptm.asu.edu
9. Inokawa H, Takahashi Y. Experimental and simulation studies of single-electron-transistor-based multiple-valued logic. *Proceedings of 33rd International Symposium on Multiple-Valued Logic.* 16–19 May 2003: 259, 266p.
10. Jana A, Halder RS, Sing JK, Sarkar SK. Design and Implementation of a Hybrid SET-CMOS Based Sequential Circuits. *Journal of Nano- and Electronic Physics.* 2012; 4(2): Pages/record No. 02004-1-02004-5, 2012.

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