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PENTACENE-BASED ORGANIC THIN FILM TRANSISTOR WITH SiO_2 GATE DIELECTRIC

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An organic thin film transistor (OTFT) based on pentacene was fabricated with SiO_2 as the gate dielectric material. We have investigated the effects of the thickness of pentacene layer and the organic semiconductor (OSC) material on OTFT devices at two different thicknesses. Au metal was deposited for gate, source and drain contacts of the device by using thermal evaporation method. Pentacene thin film layer was also prepared with thermal evaporation. Our study has shown that the change in pentacene thickness makes a noteworthy difference on the field effect mobility (μ_{FET}), values, threshold voltages (V_T) and on/off current ratios (I_{on}/I_{off}). OTFTs exhibited saturation at the order of μ_{FET} of 3.92 cm^2/Vs and 0.86 cm^2/Vs at different thicknesses. I_{on}/I_{off} and V_T are also thickness dependent. I_{on}/I_{off} is 1×10^3, 2×10^2 and V_T is 15 V, 27 V of 40 nm and 60 nm, respectively. The optimized thickness of the pentacene layer was found as 40 nm. The effect of the OSC layer thickness on the OTFT performance was found to be conspicuous.

Keywords: OTFT; pentacene; SiO_2; thickness; mobility.

1. Introduction

The interest for the organic-based transistors has increased consistently with increasing technological demand since the first polymer and small molecule semiconductor-based organic film transistors were produced and studied.[1–5] Recently, a significant success has been reached in organic thin film transistor (OTFT) technology and the field effect mobility (μ_{FET}) value has reached to a level of 3.2 cm^2/Vs which is considerably high.[6] OTFT has become a very

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attractive tool for electronic applications such as radio frequency detection (RFID) devices,[7] flexible displays,[7,8] sensors[9] and electronic barcodes.[10,11]

The basic layers of OTFTs are organic semiconductor (OSC) and polymeric insulator (dielectric). Some of the high conjugate OSCs, which have been studied recently in common are pentacene,[12–14] pentacene derivatives,[15] alpha-hexathienylene,[16] rubrene,[17] poly(3-hexylthiophene),[18–21] poly-(9,9-dioctylfluorene-co-bithiophene),[22] poly(3,3‴-dialky-quarterthiophene).[23]

Small molecule OSC materials, which are used as an alternative to the polymeric materials, can be used to produce a thin film by either dissolving in a solvent or evaporating at high temperatures. An aromatic compound pentacene, with its five benzyl chain, is the best example among the materials that their thin films can be grown by evaporation method.

OTFTs which have been produced using pentacene OSC with inorganic materials such as SiO_2 and Al_2O_3 are commonly in use.[24] Pentacene is a *p*-type OSC material that has the most common use at OTFT production. The highest mobility value of pentacene in which polymeric insulator was used is $3\,cm^2/Vs$.[25] However, the mobility value for the pentacene OTFTs which were grown on the chemically altered SiO_2/Si layers was recorded as $6\,cm^2/Vs$.[26] In addition to choosing the OSC material for an OTFT design, choosing the suitable gate insulator material is also another important issue which plays a significant role as a performance parameter.[27] Transistor parameters such as mobility and threshold voltage are all deeply related to the chemical structure and the dielectric properties of the insulating materials.[28] Many research groups have been working on pentacene TFT dielectric interface properties and the correlation between the pentacene and oxygen.[29–31]

Recent studies show that the high performance bottom-contact (cBC) structure is often used for pentacene-based OTFTs (Table 1).[32–36]

In this study, pentacene-based OTFT was produced in which *p*-type Si/SiO_2 was used as a dielectric layer. We obtained the μ_{FET}, on/off current ratio (I_{on}/I_{off}) and threshold voltages (V_T) from the output and transfer characteristic curves for two different pentacene thickness driven by top contact pentacene OTFTs as depicted in Fig. 1.

Table 1. Summary of pentacene-based OTFTs.

	μ_{max} ($cm^2/V{\cdot}s$)	I_{on}/I_{off}
Ref. 32	0.001	$\sim 10^3$
Ref. 33	0.003	2.4×10^3
Ref. 34	0.05	2.1×10^4
Ref. 35	0.24	1.9×10^5
Ref. 36	2.3	$\sim 10^5$
	4.2	
	4.4	
	4.8	
This work	3.92	1×10^3
	0.86	2×10^2

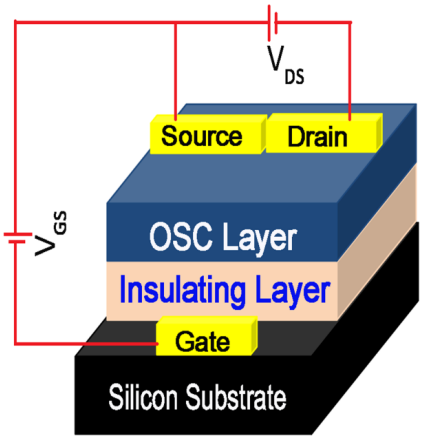


Fig. 1. Scheme of common top contact geometry for pentacene OTFT.

2. Experimental

2.1. *Pentacene-based OTFT production*

Pentacene (Fig. 2) and thermally oxidized Si wafers (Fig. 3(a)) are commercially obtained. Pentacene ($M_n = 278{,}35\,g/mol$, purity $> 99\%$) was purchased from Sigma-Aldrich. The thickness of silicon layer is $500\,\mu m \pm 50\,\mu m$, the thickness of the oxide layer on the Si is $500\,nm \pm 50\,nm$ and it is highly p-doped Si in (111) orientation.

At the first step of the production, we have removed some SiO_2 from one side of the silicon surface. SiO_2 is also known as the best insulating inorganic material for OTFT fabrication (Fig. 3(a)). We have maintained a contact on the silicon layer at one side of the substrate from which SiO_2 was removed.

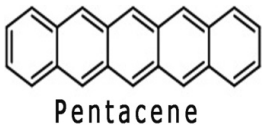


Fig. 2. Structure of the pentacene molecule.

Then, SiO_2 and Si surfaces were cleaned by technical solvents and by distilled water in the ultrasonic bath. Later, argon bath gas is also applied as the final cleaning (Fig. 3(b)). The following process is to take a gate contact on the Si layer and then we have coated the pentacene on SiO_2 layer by thermal evaporation method under 3.7×10^{-6} mbar pressure (Fig. 3(c)). After the pentacene deposition, source and drain electrodes with thickness of 50 nm were deposited by Au over the pentacene layer using a shadow mask under a pressure of 4×10^{-6} mbar using the thermal evaporation method again (Fig. 3(d)). Finally, we have connected the contacts as in (Fig. 3(d)) to perform the characteristic measurements of our OTFT.

According to the production step and to the design of our OTFT, our device geometry is a top contact transistor model, which has drain and source contacts on the semiconductor layer and the gate at the bottom (Fig. 1).

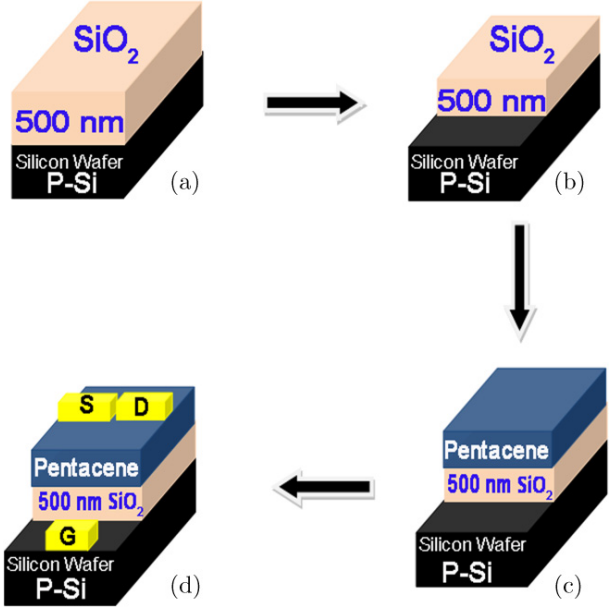


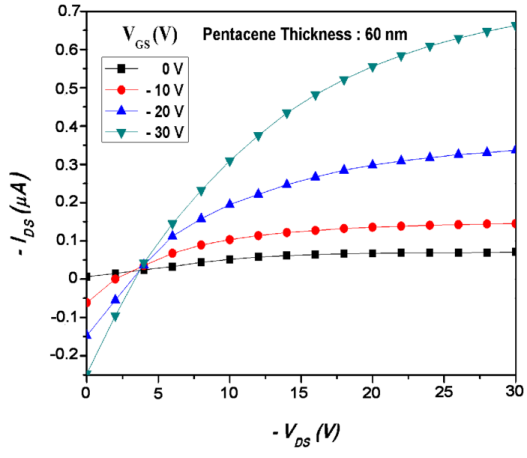
Fig. 3. The production steps of the OTFT.

3. Results and Discussion

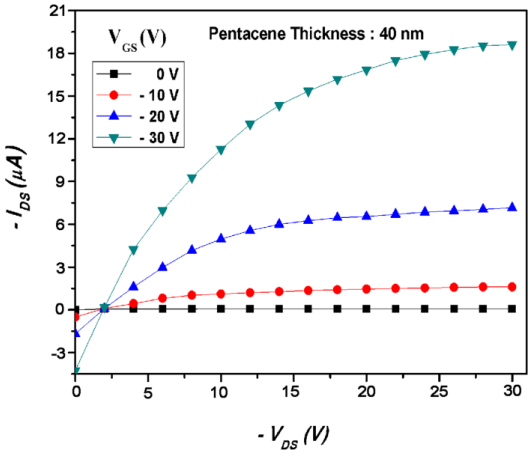
3.1. *The investigation of the current–voltage characteristics of the pentacene/SiO_2-based OTFT*

The current–voltage characteristics of our devices were investigated by using a Keithley 4200 semiconductor characterization system (SCS). The V_{DS}–I_{DS} curves were plotted for two different pentacene thicknesses at four different gate voltages (Fig. 4). The device output and transfer values were measured with the Keithley 4200 SCS.

The thickness of the pentacene film was measured by a profilometer. The thickness of the oxygen layer of SiO_2 is 500 nm. Output and transfer characteristics of

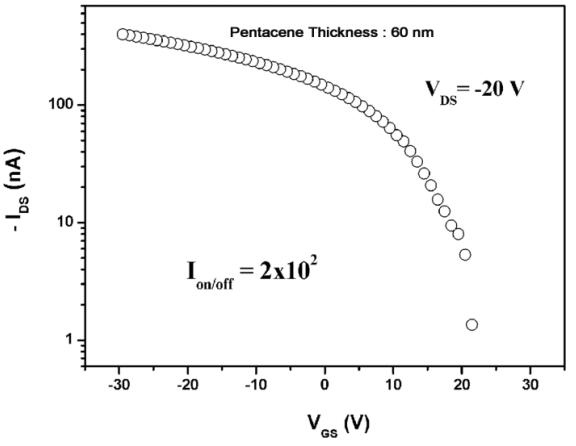


(a)

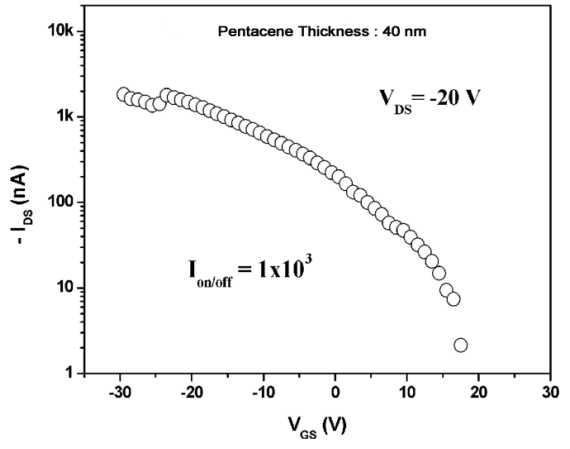


(b)

Fig. 4. I_{DS}–V_{DS} negative output curves of SiO_2/pentacene-based OTFT at different V_{GS} potentials (a) 60 nm pentacene thickness (b) 40 nm pentacene thickness.



(a)



(b)

Fig. 5. SiO_2/Pentacene-based OTFT I_{DS}–V_{DS} output values ($V_{DS} = -20$) (a) 60 nm pentacene thickness, (b) 40 nm pentacene thickness.

the pentacene/SiO_2-based OTFT are as follows: W/L ration is 1000 μm/17 μm. The device exhibits good saturation characteristics at 30 V operation voltage ($V_{GS} = 0$ to -30 V). The μ_{FET} values for 40 nm and 60 nm pentacene thin film layers were obtained as 3.92 cm^2/Vs and 0.86 cm^2/Vs, respectively.

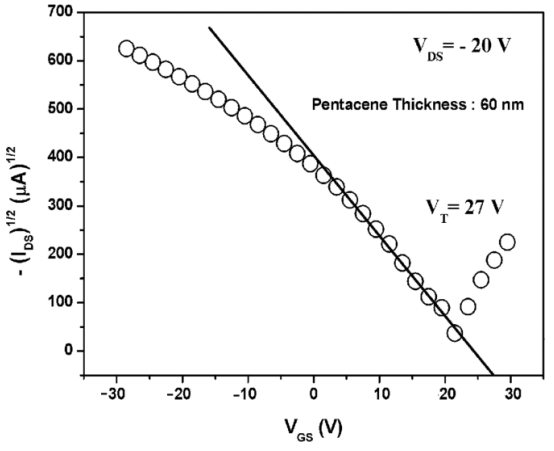
We have evaluated the V_{GS} vs I_{DS} curves for the same value of the V_{DS} at -20 V. In order to reach the I_{on}/I_{off} values we take the logarithm of current values (Fig. 5). As it can be seen from the graph, the I_{on}/I_{off} values for 60 nm and 40 nm pentacene were found as 2×10^2 (Fig. 5(a)) and 1×10^3 (Fig. 5(b)), respectively.

Finally, as shown in Fig. 6, the μ_{FET} can be determined from the slope of a plot between $|I_{DS}|^{0.5}$ vs V_{GS} output curves derived from Eq. (1). The extrapolated x-intercept of this plot yields the value of the threshold voltage.

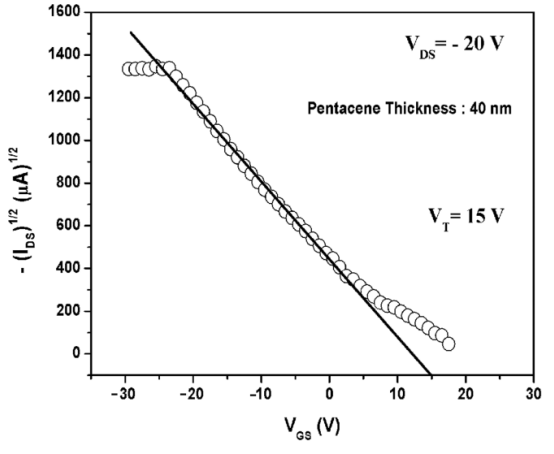
$$I_{DS} = \mu_{FET} \frac{WC_i}{2L} (V_{GS} - V_T)^2. \quad (1)$$

Where C_i is capacitance of insulator layer, W is width of source and drain electrodes, L is length between source and drain electrodes and μ_{FET} is field effect mobility of OTFT device. In this study, we have used SiO_2 as insulator layer. Si/SiO_2 was purchased commercially and capacitance of SiO_2 layer was 10 nF.

We have calculated the mobility value of the SiO_2/pentacene-based OTFT in its saturation zone



(a)



(b)

Fig. 6. $(I_{DS})^{1/2}$-V_{GS} output curves of SiO_2/Pentacene-based OTFT ($V_{DS} = -20$) (a) 60 nm pentacene thickness, (b) 40 nm pentacene thickness.

from the slope (α) of the best fitted curve applying the formula shown in Eq. (2).

$$\alpha = \left(\frac{WC_i}{2L}\right)^{1/2}, \tag{2}$$

where α is slope of the $(I_{DS})^{1/2}$ vs V_{GS} plot.

4. Conclusion

The thickness of pentacene layers was found to have a prominent influence on the performance of pentacene OTFTs. The reason why the SiO_2 dielectric layer did not show good interface characteristics with pentacene thin layer in our OTFT devices is related to the organic/inorganic incompatibility of the interface. On the other hand, the mobility of our devices and their performances are found to be almost in accordance with some literature values, whereby a new verification of a promising assembly and material is added to the literature. Additionally, because the performance of OTFT based on pentacene device such as μ_{FET} and I_{on}/I_{off} will be affected by the OSC thickness, precise thin films have to be optimized and employed.

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