A D&T Roundtable

Design Automation in Europe

D&T: What design automation concerns do we face in Europe?

Borel: Process capabilities have been growing steadily since the early 1970s, approximately doubling in complexity every 18 months. Process has reached a mature engineering level, with 80% of process modules reused from one generation to the next. About 20% of the modules require change chiefly because of interconnections. With design automation, the figures are the same but reversed: 80% of the modules change and only 20% are reused. Compared with 60% increased process capabilities each year, we achieve only a 20% increase in design efficiency. We call this the process-design gap.

Ghenassia: With current process capabilities, we can now embed several programmable cores in circuits. The design environment must therefore address the integration of hardwired logic and processors. Besides, these processors run large programs: Being able to write the embedded software in a high-level language (mainly C) is not always feasible because of the lack of optimizing compilers, especially for digital signal processors. The availability of such compilers is essential to increase design productivity.

D&T: What ingredients would narrow the gap?

Rosenstiel: The system-on-a-chip (SOC) era has, of course, more degrees of freedom than traditional multichip designs, but the additional freedom requires additional optimization for competitive designs. Therefore, to bridge the design-technology gap, we urgently need better tools and methodologies to solve the increasing productivity problem. We especially need concurrent developments in IP reuse, hardware-software co-design, and system-level design. System-level design is particularly important in Europe because Europe is strong in the system design areas of automotive, telecommunications, and consumer electronics.

Borel: The first ingredient is IP reuse, especially in the short term. In some (ideal case)
examples today, 90% of a circuit's blocks can be reused but only by improving our design efficiency by a factor of 10. This has a cost, however. The second ingredient is hardware-software codesign, which allows us to design at a higher level of abstraction. With architectural design and hardware-software partitioning, we expect another order of magnitude efficiency gain. Finally, specification validation through virtual silicon is key. Today, it's a problem because we see 60% of production prototypes failing because of noncompliance with specifications. Solving the specification validation problem will save a lot of money and improve time to market.

**Ghenassia:** Software and core reuse are key to increased productivity. This implies that we need hardware-software codesign tools as well as optimizing C compilers.

**Perea:** From the digital point of view, we need to design an RF front-end together with analog-to-digital conversion, which is completely different and for which no tools are available. We need to extend hardware-software codesign to the analog world, which is currently hardwired: We have no automation, we must go to lower levels of design, and we must keep our experienced designers, which is costly. Additionally, we must pass all the constraints from the bottom to the top, including parametric and parasitic effects.

**Borel:** Two other considerations are of paramount importance. First, these evolutions in acquiring better tools and methodologies must simultaneously help to shorten the time to market. This time constraint means that design solutions should focus on dedicated applications, that is, on heavily reusing IP in a given process for a dedicated application. Second, the performance increase in products —low power, high speeds— requires a better matching of silicon to the application. We can obtain 10 to 100 times better gains in computational efficiency, which will improve mobile system performance. Once we have developed a global ASIC solution for design automation, we'll have to develop silicon application platforms for higher SOC performance. This may well be the future focus for Europe. Moreover, the silicon application platform concept could help Europe in the continuation of MicroElectronics Development for European Applications (MEDEA) by giving European system houses an advantage, in terms of SOC performance and time to market. Such a platform would require semiconductor and system house cooperation.

**D&T:** Is design automation in Europe strong because authorities are encouraging?

**Sauer:** Public authorities (government agencies) support us by promoting the needs of European companies. For example, application projects in MEDEA, a Eureka program in which 130 partners from 11 countries cooperate on 45 different projects, involve key European silicon and system companies.

**Borel:** European programs are helping to solve problems not otherwise addressed by large electronic design automation (EDA) companies. For example, the UMTS project has a system house and a semiconductor manufacturer collaborating on a complete system architecture plus a library of "pico power" for mobile equipment. More development is needed for this project; it is a dedicated application that the European Community can support. Another success is new European start-ups, such as CoWare and Arexsys, that address hardware-software codesign.

**Ghenassia:** MEDEA is a nice framework for cooperation, as it enables technology transfer from universities to industry. MEDEA is also a good catalyst for cooperation between companies, which can then foster the emergence of technology standards.

**Rosenstiel:** From the university point of view I also can confirm that MEDEA is a very good vehicle for cooperation. On one hand, research results in the SOC area are, as early as possible, transferred within the MEDEA projects to industrial partners and applications. On the other hand, industrial
needs directly influence research activities at universities and research institutes.

D&T: How does MEDEA contribute to Europe's EDA programs?

Sailer: About 100 companies, universities, and institutes work together in research and development for MEDEA, which is one of the largest Eureka projects. Companies, normally competitors, cooperate in R&D and share the risk costs, which we call horizontal cooperation. MEDEA also supports vertical cooperation, which includes system houses and silicon vendors. This far-ranging cooperation is the reason why governments support leading European companies.

D&T: What sort of resources can MEDEA and other programs rely on?

Sailer: MEDEA’s total budget of 2,000 million euros (US$2,200 million) extends over four years, 1997 to 2000. Half comes from the partners, half from public authorities. MEDEA involves two major groups: silicon companies and equipment manufacturers on the one hand, and system companies in consumer electronics, automotive electronics, and communications on the other. MEDEA has seven ongoing design projects in four areas of CAD: deep submicron, system-level, analog, and RF. The strategy is to share results, to develop tools complementary to those of the main EDA vendors. Some of the CAD projects include key CAD vendors. Other national programs support EDA, notably ESPRIT, a program funded by the European Union.

D&T: Earlier, Joseph said that IP and codesign will boost productivity by a factor of 10; comments?

Rosenstiel: We expect design reuse to be the key enabler in design methodologies, for both short- and long-term development, and MEDEA will be at the forefront. IP reuse is one of the hottest topics in the domain of SOC design to solve the productivity problem. Besides the purely technical view of IP reuse, business models and legal questions are vital to the success of IP development and exchange strategies.

Today, reuse is either restricted to dedicated solutions integrated into specific EDA tools or else takes place in parallel to the conventional design flow. Reuse-oriented techniques require both: a complete integration in the design flow and the introduction of business models customized to the companies’ needs. The introduction of reuse is complex. Unlike a tool’s introduction, comprehensive reuse requires a new design methodology and a modification of the design flow. This complexity compares to that of a design framework containing both metadata and design data.

Borel: IP reuse has been applied in the past. What is new is that companies have agreed on socketing rules, so now the concept can be more widely spread. Internally, European companies have started teaching this new approach to culture, and preliminary results are already measurable (such as the compliance of some designs versus blue book specifications). Converting companies’ internal IP, however, to something reusable remains a huge task.

Rosenstiel: Existing hardware reuse approaches cannot support several abstraction levels but are restricted to just a few reuse aspects. We must focus on both design for reuse and the reuse of existing designs—achieving the factor-of-10 productivity gains discussed earlier requires both. Both approaches require databases and standard interfaces to implement mature reuse management systems. A first step in this direction is the Virtual Socket Interface Alliance (VSIA).
Perea: "Analog and most RF systems are still in a similar stage of development from the design automation viewpoint; designs are very dependent on the process and the packaging."

Tools must follow these standards to offer both the exchange of virtual components and the exchange of reuse management systems. In addition, database classification and retrieval techniques are also required.

D&T: People generally say, "It is difficult to reuse what was not designed for reuse." Comments?

Rosenstiel: Without a design for reusability, yes, it is much more difficult to adapt a given module for a new design environment. Explicit parameterization is missing, and often there has not been enough effort for design integration and verification.

Ghenassia: Right; it’s difficult. It is also difficult to reuse blocks that were designed for reuse if they don’t share a common set of characteristics such as the design language and rules (for example, reuse of a block designed with Verilog in a circuit mainly designed in VHDL). Design rules are important to design reuse.

Rosenstiel: IP design should include the design tools and design flows. IP design must be done on different abstraction levels, and a corresponding reuse management system—in terms of a complete reuse framework or environment—is necessary.

Borel: Quality will make or break IP. Bad quality is a killer for IP, yet IP vendors hardly realize that.

Rosenstiel: On the other hand, by reusing designs, the quality will improve because reused designs will be better debugged than designs used just once.

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Ghenassia: "It is... difficult to reuse blocks that were designed for reuse if they don’t share a common set of characteristics such as the design language and rules..."
Rosenstiel: "We must support co-debugging of hardware and software components, and the use of heterogeneous emulation platforms."

Borel: From a designer’s point of view, the main problem is the top-down constraint propagation. If we implement the design at the gate level, optimization may be difficult because we may find that we cannot meet the speed requirements, for example.

Ghenassia: System constraints must be considered throughout the entire design process, and tools should support such top-down propagation. At the same time, it should be possible to feed information extracted from detailed simulation models of blocks into system-level simulations to verify that the design really meets the specified constraints.

D&T: What is Europe’s part, specifically, in the analog domain?

Borel: Europe is leading in several applications in which analog and mixed analog-digital functions are key for system-level applications: for example, telecommunications and automotive. As far as STMicroelectronics is concerned, only 50% of the sales are purely digital.

Designing and manufacturing analog or mixed analog-digital systems is a strategic issue. Digital products are very sensitive to memory shortages because memory processes are rapidly converted into ASIC processes. We need open design solutions to address concurrent analog/RF and digital aspects so that the complete system is optimized, not just the parts. Solutions are starting to appear on the market but unfortunately they remain partial solutions.

Phillips, STMicroelectronics, Bosch, Nokia, and others are leaders in several application domains where analog is a key technology. This explains why they suffer less in a worldwide memory shortage.

D&T: What is noteworthy about Europe’s analog expertise?

Perea: Europe is ahead in the analog domain mainly because of the basic research efforts carried out by European universities. Also, many companies are leading sales in the analog arena, such as STMicroelectronics, Bosch, and Ericsson, among others.

Borel: Our processes are more suitable for mixed-signal applications. To a digital backbone, we add options (such as analog, RF, and nonvolatile memory). These give the digital blocks portability—which is in fact the options’ specification.

Perea: Analog design doesn’t require very advanced technologies. Our analog design’s value is in making the mixed
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digital-analog design more powerful. Europe excels in two areas: analog/RF, since its good academic basis helps the development of good analog tools, and low power, because of the extremely stringent requirements of portable terminals. We must consider dynamic power versus standard power. To optimize the complete system, we must also consider analog power consumption. Europe is turning its traditional microwave expertise into RF, and STMicroelectronics is leading in several areas in this regard.

D&T: What European highlights in design automation would you conclude with?

Ghenassia: Design tools are emerging that take into account hardware and software with the capability to explore architecture trade-offs. The challenge is to educate designers to use them.

Borel: Europe is the leader in system-level design according to a joint US-Europe survey, which has shown that Europe includes more research than the US. Consequently, European industries should benefit from this investment in their move to SOC.

Rosenstiel: We especially need tools and methodologies to support SOC design. In this context, hardware-software codesign is important so that we can assess, as early and as precisely as possible, the expected performance, the chip area, and the power consumption. Higher level synthesis is the enabling technology for hardware-software codesign, which also lets us obtain precise estimations in very early design stages. Furthermore, the integration of standard components and IP cores on SOC underscores the need for IP reuse. The reuse of IP cores and the more sophisticated memory structures require the use of synthesis tools at all levels of abstraction. Finally, in such complex systems, better validation, especially the development of new and efficient debugging methods, is increasingly important.

Borel: R&D in Europe will continue to be strong. We should encourage start-ups as much as possible, with support from semiconductor and system houses.

Sauer: In cooperative projects, R&D efforts should include the CAD work of system houses and of silicon designers. From applications, we can derive the needs for design automation and integrate them in the development flow.

Coming Next Issue

Is hardware-software codesign the real problem we're facing today? Or, is it embedded system design? Look for the answer in the January-March 2000 issue of IEEE Design & Test. Our experts participated in a roundtable on hardware-software codesign at the CODES workshop held last May in Rome, Italy. Their comments may surprise you.