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Modeling of FPGA- and DSP-Based Pulse Width Modulation for Multi-Input Interleaved DC/DC Converter

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Abstract – *This paper proposes a development of Pulse-Width Modulation (PWM) switching signals based on Field Programmable Logic Array (FPGA) and Digital Signal Processor (DSP) to control multi-input interleaved DC/DC converter (MIC). The proposed PWM signals for the MIC do not only require a control of duty cycle, but also operation at different PWM frequency. In order to solve this problem, a simple programmable control scheme using a digital controller can be employed to facilitate the realization of PWM signals generation. The PWM signals are designed by using Altera Cyclone II FPGA board. The duty cycle employed to regulate output voltage is attained from the dSPACE DS1103 board using a Proportional-Integral (PI) controller. This paper also highlights design guidelines, simulation and experimental results. Experiment results show that the proposed DC converter can be driven by PWM signals, by integration of both controllers.*

Keywords: *Pulse-Width Modulation, Digital Signal Processor, Field Programmable Logic Array, Multi-Input Converter, Proportional Integral*

Nomenclature

V_n	n^{th} input voltage (n=1,2)
S_n	n^{th} power switch (n=1,2,3,4)
V_{Sn}	n^{th} switching signal (n=1,2,3,4)
i_{L1}	Current at inductor 1
i_{L2}	Current at inductor 2
D_n	n^{th} diode (n=1,2,3,4)
V_{out}	Voltage across output
L_1	Inductor 1
L_2	Inductor 2
L_{r1}	Resonant inductor 1
L_{r2}	Resonant inductor 2
C_{r1}	Resonant capacitor 1
C_{r2}	Resonant capacitor 2
C_{out}	Output capacitor
R	Load resistance
n	Number of bits
t	Time
t_n	n^{th} time range (n=1,2,3,4)
k	Constant
f_c	Frequency
f_{clk}	Main clock frequency
t_c	Clock time (s)
t_{on}	Turn-on state
t_{off}	Turn-off state
V_{ref}	Reference voltage
V_{tri}	Triangular voltage
Δd	Duty cycle resolution
d	Duty cycle
c	1, for up or down counter and; 2, for up-and-down counter

I. Introduction

In recent years, numerous researches on multi-input converter (MIC) have revealed the advantages of simple circuitry, such as low output ripples and high efficiency. MICs are used in combination of two or more input powers with different voltage magnitudes. The research on MIC has been explored in previous studies in various fields such as grid connection [1], [2], street lighting [3], hybrid electric vehicle (HEV) [4] and DC bus [5], in which the inputs are supplied by photovoltaic panels [6], fuel cells, wind turbines, batteries and a combination of renewable energy [3], [7]-[9]. However, the overlapping voltage between switching signals in MIC, which causes a higher input ripple, is not considered in the design. The size of inductors will be increased causing an increased weight and cost of the system. Inappropriate design of Pulse-Width Modulation (PWM) switching scheme can cause a high input current stress in the circuit.

PWM technique is widely used in numerous power electronics converter and has been intensively researched in the past few years. Several common approaches and techniques to generate PWM signals for DC and AC converters have been presented in [10]-[14], [20]-[23]. Basically, a PWM technique is an on-and-off signal used to trigger a switch to permit current to flow through a circuit. The amount of current flow is dependent on the 'on' state over a period.

Therefore, the amount of current flow in the circuit is directly proportional to the 'on' state switching of the system. PWM signals can be generated using analog or digital circuit. Some advantages of digital systems that use microcontrollers, compared to analog circuit, are

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discussed in detail in [15]. Analog systems require a large number of components, especially passive components, which can reduce system reliability due to hardware complexity, besides affecting space and energy utilization. Besides that, analog systems are difficult to reconfigure without changing the hardware circuits. In fact, they also have poor and limited computational capability to solve complex mathematical operations.

Nowadays, digital systems have become more attractive as they allow realization of complex control strategies with powerful mathematical solver. Thus, advanced and sophisticated control techniques can be implemented in short periods by using any superior computational software. Digital Signal Processors (DSPs) are commonly used to solve complex mathematical functions or algorithms with floating-point operations. In certain applications, single Field Programmable Logic Array (FPGA) can completely replace the dedicated DSP; however, FPGA can never replace the general purpose of DSP in floating-point performance. One way to enhance DSP performance is by employing multiple DSPs in parallel. However, this will require more space and memory, which in turn increases the cost of hardware. A better solution is to use a DSP processor, a microprocessor, or a micro-controller with FPGA as a co-processor. However, due to certain limitations, the controller is required to work with one or more microcontrollers, as outlined in [16]. Hybrid structures, which combine both categories of processes, have been introduced in [17]-[19] with fast computational and scalable performance, where highly complex operation can be implemented in simpler manner. This paper presents a proposed design of PWM signals for multi-input interleaved converter (MIC) using FPGA and DSP tools. The MIC requires four PWM switching signals operating in two different frequencies to turn on and off the switches according to control algorithm. In the proposed design, Altera DE2-70 board with EP2C70F896 is used to generate PWM signals with multiple frequencies in fixed-point arithmetic. In the meantime, dSPACE DS1103 Digital Signal Controller (DSC) is used to process the PI control algorithm in floating-point computation. FPGA is used to generate PWM signals with multiple frequencies by synchronizing clocks, which is a significant drawback of DSP. With the proposed PWM switching strategy that is specifically designed for Pulsating Voltage Source Cell (PVSC) configuration, it can overcome the issue of overlapping unregulated input sources which results in high input current ripple. The integration of both controllers will be further discussed in Section III.

II. Circuit Configurations

Fig. 1 shows the proposed MIC structure. There are four power switches (S_1, S_2, S_3, and S_4), which require four PWM switching signals to turn on and off depending on the input voltage at V_1 and V_2. The frequency of the primary (S_1 and S_2) and secondary (S_3 and S_4) circuits are 50 kHz and 100 kHz, respectively.

The secondary circuit is actually an interleaved two-phase boost converter operating with interleaving method to minimize the output current and voltage ripple. The secondary circuit, which is formed by resonant inductors (L_{r1} and L_{r2}) and capacitors (C_{r1} and C_{r2}), operates in Zero-Voltage Switching (ZVS) condition in order to reduce the voltage stress across the switches. The input voltages from V_1 and V_2 are not always in the same magnitude, with assumption that the inputs are connected to different types of power sources, for example, PV arrays, wind turbine, battery or ultra-capacitor.

Therefore, the PWM signals for the primary and secondary circuits should be designed to operate simultaneously in order to accommodate the variation of load conditions.

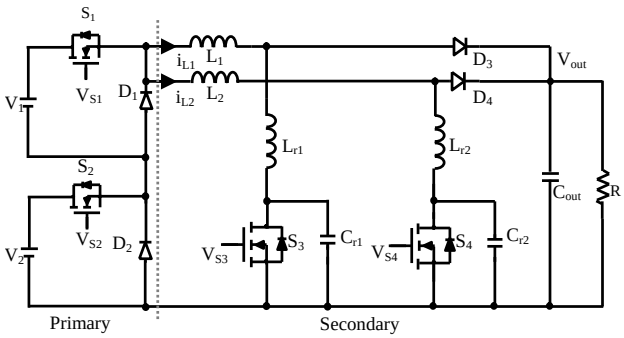
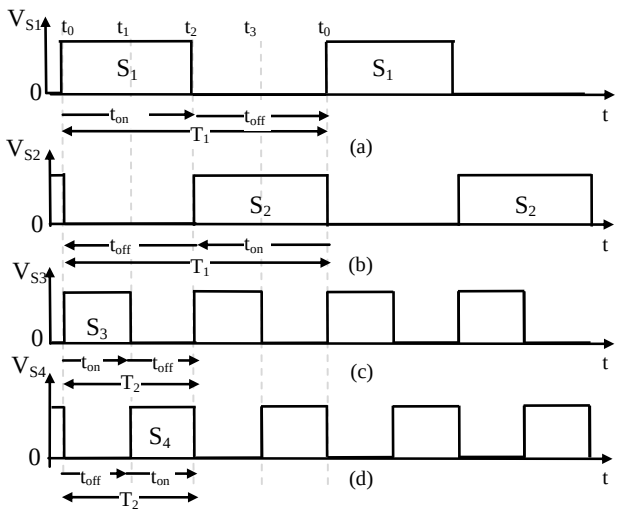


Fig. 1. Proposed multiple-input converter

III. Proposed Switching Strategies

Figs. 2 show the switching strategies for the proposed converter. Figs. 2(a), (b), (c) and (d) depict the PWM signals for V_{S1}, V_{S2}, V_{S3} and V_{S4}, respectively. Four PWM signals are used to trigger the four switches, starting at t_0.



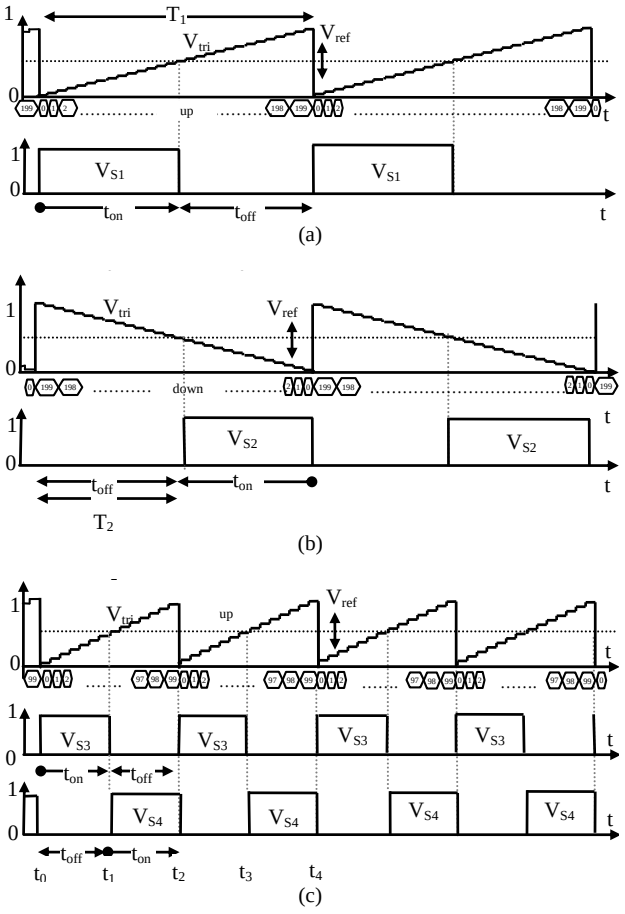
Figs. 2. PWM control of multi-input interleaved DC/DC converter and associated waveform for digital implementation

The PWM switching signals for S_1 and S_2 are entirely dependent on their sources, which are not always at the

same level. Additionally, the designs for the PWM signals for S_1 and S_2 are according to the variation of the input voltages, which can be categorized into three states: $V_1=V_2$, $V_1<V_2$ and $V_1>V_2$. The PWM signals for secondary switches S_3 and S_4 are in the same duty cycle with 180° phase-shift, with respect to each other in order to prevent unbalanced inductor currents (i_{L1} and i_{L2}) through inductors L_1 and L_2. Meanwhile, the maximum duty cycles for S_3 and S_4 are set to 50 percent or slightly less, depending on the allowable current flow through inductors L_1 and L_2.

III.1. Digital Switching Technique

The technique to generate the PWM signals digitally is identical to that attained through the analog circuit, which involves the use of comparators. Figs. 3 show the proposed techniques to generate PWM signals for the DC converter. As referred to Fig. 3(a), there are triangular and straight-line waveforms to represent V_{tri} and V_{ref}, respectively. In digital implementation, the triangular waveform represents a digital counter, while the straight line represents reference waveform.



Figs. 3. Associated PWM technique using digital implementation for switches (a) S_1 (b) S_2 and (c) S_3 and S_4

As mentioned before, the switching frequencies of the primary and secondary circuits are 50 kHz and 100 kHz, respectively, therefore, the counters set for primary and secondary switching are 200 and 100 pulses, respectively, which are fed from a 10-MHz clock. The carrier frequency related to the main clock frequency and the up/down counter can be calculated using Eqs. (1) and (2):

$$f = \frac{f_{clk}}{\left(2^n - 1\right)c} \ [\text{Hz}] \tag{1}$$

or:

$$f = \frac{1}{\left(2^n - 1\right) c \ t_c} \ [\text{Hz}] \tag{2}$$

where:

$$t_c = \frac{1}{f_{clk}} \tag{3}$$

$$\Delta d = \frac{1}{\left(2^n - 1\right) c} \tag{4}$$

For n number of up/down with the main clock frequency, the carrier frequency can be calculated. The counter for V_{S1} will start counting up from 0 to 199. Simultaneously, the counter for V_{S2} will count down from 199 to 0; this process will repeat continuously. In the meantime, the secondary counter will count up from 0 to 99.

All counters are clocked externally by the 10-MHz main clock frequency (f_{clk}), which equals to t_c=1/100 MHz (100 ns) per clock, calculated using Eq. (3). The duty cycle resolution per counter, Δd, can be calculated using Eq. (4). Meanwhile, V_{S3} turns on at t_0 (counter=0), and V_{S4} turns on at t_1 (counter=49). The maximum duty cycles for V_{S3} and V_{S4} are at t_1 (counter=49) and t_2 (counter=99), respectively. The duty cycle, d, can be adjusted in discrete steps, identical to the counter resolution. Therefore, a high-resolution counter will result in favorable control performance. The PWM signals for V_{S1} and V_{S2} are independently and simultaneously controlled using optimization techniques, which are based on certain relationship of the input voltages. The crossover between V_{ref} and V_{tri} will produce desired PWM signals. The calculated duty cycle resolutions for the primary and secondary PWM signals are 0.005 and 0.01 per counter, respectively.

III.2. FPGA and DSP

Fig. 4 shows the block diagram of the complete system integration. FPGA is used to generate PWM signals and a DSP board is used to implement the closed-loop system according to the desired control law, such as PID, fuzzy and neural network, using MATLAB/Simulink environment. In this study, DSC model DS1103 with TMS320F240 from Texas Instruments had been used, which has 1-GHz clock, 50-

bit input and output channels, 36 analog-to-digital channels (16 bits), and 8 digital-to-analog channels (16 bits). The Real-Time Interface (RTI) is fully programmable from the Simulink block diagram environment, and all inputs and outputs can be configured graphically. By using the dSPACE DS1103 Real-Time Interface, the input and output can be easily monitored, measured and controlled during the process.

A voltage sensor is used to measure the output voltage signal across the load. The measured voltage will be analyzed and processed by a specifically designed PI controller in MATLAB/Simulink software. All necessary experimental results can be monitored via Real-Time Interface (RTI) using the Control Desk software.

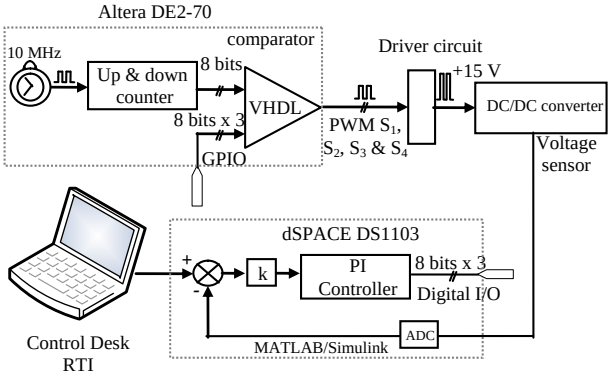


Fig. 4. Block diagram of the system

Nonetheless, there are some difficulties in implementing the PWM signals by the proposed design using dSPACE DS1103 controller due to the limitations in generating multiple frequencies.

This is because the proposed PWM signals have two different switching frequencies for the primary and secondary circuits.

Available Simulink blockset for PWM *(DS1103SL_DSP_PWM)* as provided by dSPACE is incapable of generating corresponding PWM signals with different frequencies, even with the combination of other Simulink blocksets, such as the three-phase PWM generation *(DS1103SL_DSP_PWM3)* and space vector PWM generation *(DS1103SL_DSP_PWM_SV)*. Even though PWM Simulink blockset can be used to generate a PWM signal up to 5 MHz and provide more than three PWM signals, the frequencies could not be set separately. In addition, digital IO ports are only capable of producing less than 50 kHz of sampling frequency. Other than that, Digital-to-Analog Converter (DAC) ports have an output offset drift (30 µV/k), which will affect the shape of PWM signals with each increase of the switching frequency. Hence, this is where FPGA plays the prominent role in generating PWM signals. The signals can be easily created using available logic block, custom megafunction, Verilog, and VHDL programming. Quartus II software offers a variety of megafunctions, including library of parameterized modules (LPM) functions and other parameterized functions.

III.3. Quartus II

Fig. 5 shows the block diagram file (*.bdf) for the proposed DC/DC converter programmed using Quartus II software. It consists of *altpll*, three *lpm_counter* and comparator. The *altpll* is a phase-locked loop (pll) feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. The *altpll* then generates a stable frequency to the input of the counter. The input of the *altpll* is connected to 50-MHz internal clock from *PIN_AD15* to generate a 10-MHz output. The *lpm_counter* block is a binary counter that creates up, down, and up/down counters. It can generate up to 256-bit-wide load ports with clear, set, synchronous and asynchronous options. There are three 8-bit *lpm_counter* used for this design. The first *lpm_counter* is for S_1, which is set to count up from 0 to 199. The second *lpm_counter* is for S_2, which is set to count down from 199 to 0. The third *lpm_counter* is for S_3 and S_4, to count up from 0 to 99. Even though the *lpm_counter0* uses only 7 bits (from 0 to 99), the *lpm_counter* is set to 8 bits because the inputs from the switch for dSPACE are all set to 8 bits. The outputs from the *lpm_counter* are connected individually to each comparator, which are then compared with the input to produce respective PWM switching signals for S_1, S_2, S_3 and S_4. All the pins are connected according to the proper sequence based on LSB and MSB. The comparators are programmed using Very High Description Language (VHDL), referring to the initial design as shown in Fig. 3. Table I shows the VHDL programming with logical operation derived from the basic concept as depicted in Fig. 3. The program is synthesized using IF ELSE statement in individual blocks.

TABLE I
LOGICAL FORM TO GENERATE PWM SIGNAL USING VHDL

Name (*.bdf)	IF (function)	THEN (output)	ELSE (output)
compare	a <= (b-1) and a <= 200	S_1= ‘1’	S_1= ‘0’
comparator	p <= (q) and p <= 199 and p >= 1	S_2= ‘1’	S_2= ‘0’
comparatorx	x <= y and x <= 49	S_3= ‘1’	S_3= ‘0’
comparatorx1	d >= 50 and d <= (50+e)	S_4= ‘1’	S_4= ‘0’

a, p, x, d = input counter ; b, q, y and e = input reference

III.4. MATLAB/Simulink Software

Fig. 6 shows the experimental setup of the system, while Fig. 7 shows the MATLAB/Simulink program using the PI controller.

The program functions to read and process the input (ADC), and write the output for digital IO. The outputs from the voltage sensor will be reduced to +5 V and read by multiplexed ADC *DS110MUX_ADC_CON1* and *DS110MUX_ADC_CON2*, referring to primary and secondary circuits, respectively.

These provide read access with ±10 Volts. The signal is multiplied with the gain and constant value, based on the voltage sensor coefficient.

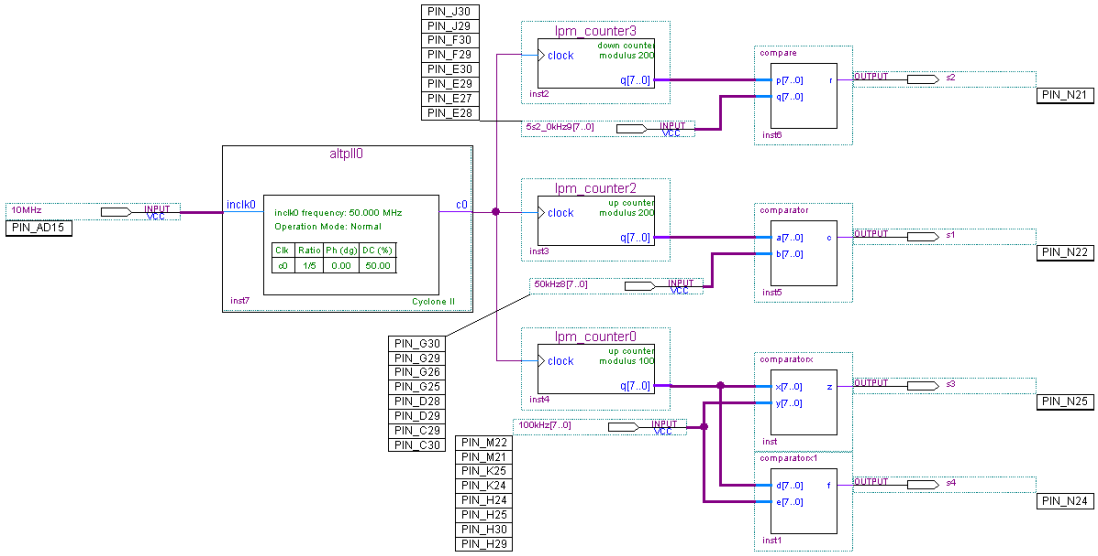


Fig. 5. Block diagram file (*.bdf) for PWM switching signal generation for S_1, S_2, S_3 and S_4

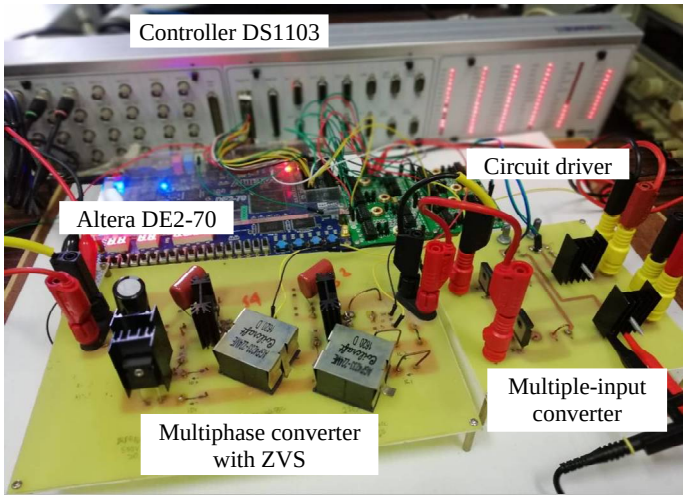


Fig. 6. Experimental setup

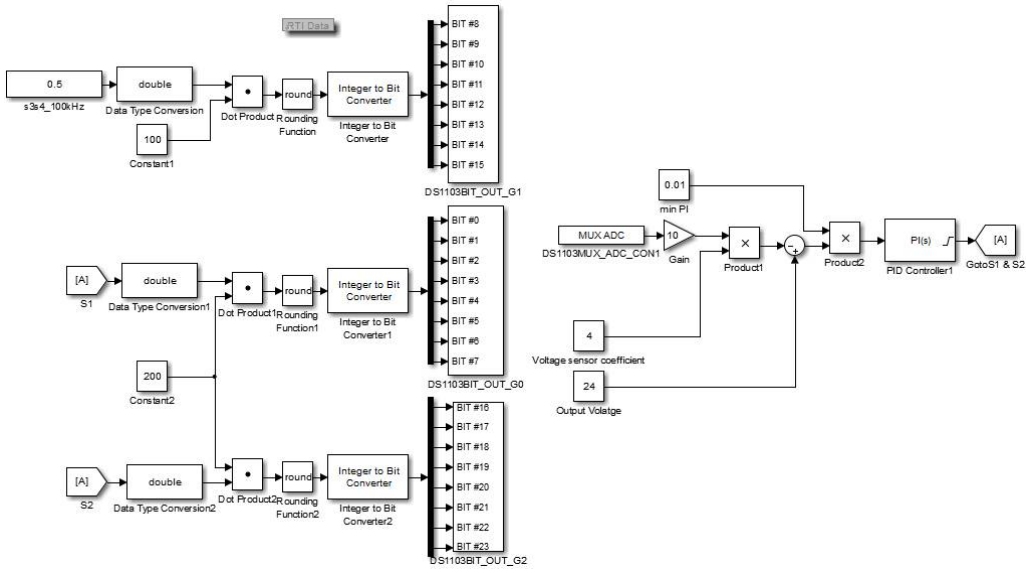


Fig. 7. MATLAB/Simulink program on dSPACE DS1103 platform using PI controller

Next, the outputs will be compared with the reference value before being processed by the PI controller. The 8-bit output signal from the PI controller is in double format. The signals are then multiplied by a constant value for the counter, and afterward proceed to the rounding function block. Finally, the rounded value is converted into an 8-bit signal. 8 bits out of the 32-bit digital output are sent out to the Altera DE2-70 General Purpose Input Output (GPIO) through digital output *DS1103BIT_OUT_GX*. The digital outputs provide write access to the 8-bit group. However, all digital channels of one group can be used either for input or for output only.

IV. Simulation and Experimental Results

The simulation of the PWM signals can be performed using the vector waveform file (*.vwf). There is an option to add a signal to a node, which is observable in the simulation waveform. This option is helpful to observe the output waveform—the input and output base of a number system (radix) for the input and output can be changed to binary, signed decimal, unsigned decimal, octal, fractional, ASCII, or hexadecimal forms. Fig. 8 shows the simulation results for the PWM signals using the vector waveform file. In this simulation, switching characteristics had been emphasized to ensure that switches S_3 and S_4 are driven by non-overlapping rectangular waveforms.

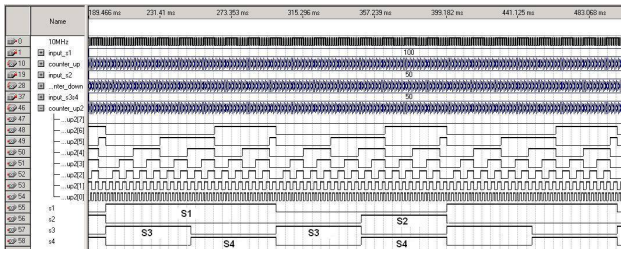


Fig. 8. Simulation results for PWM switching for duty cycles for S_1 (d=0.5), S_2 (d=0.25), S_3 (d=0.5) and S_4 (d=0.5)

Figs. 9 and 10 show the experimental results of PWM signals, measured using Tektronix TDS 3024 four-channel digital oscilloscope. The PWM signals were measured from the output of the gate driver circuits. The figures indicate that the duty cycle of each signal operated according to the desired control strategies.

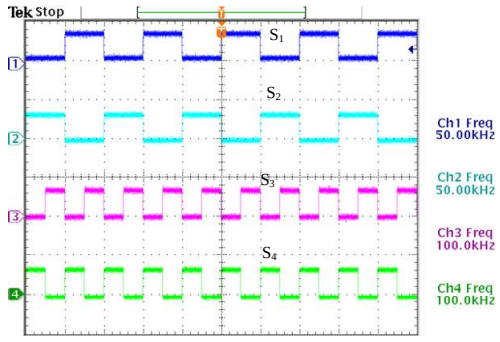


Fig. 9. Measured PWM signals for S_1, S_2, S_3 and S_4 with 0.5 duty cycle; voltage: 20 V/div; time: 10 µs/div

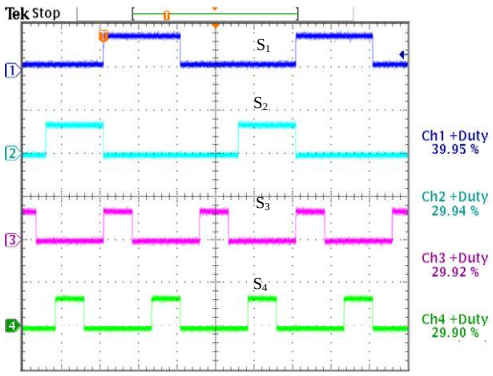


Fig. 10. Measured PWM signals for S_1, S_2, S_3 and S_4 with different duty cycles; voltage: 20 V/div; time: 4 µs/div

V. Conclusion

The proposed PWM signals designed using FPGA and DSP have been successfully implemented in multi-input DC/DC converter. This paper has outlined the techniques to generate PWM signals from analog to digital, with prospects of using digital counter, logic gates and VHDL programming. This study intends to show that, with the use of digital systems, even sophisticated design techniques can be solved. In addition, digital switching provides greater advantages over analog switching in terms of operation frequency, hardware size, programmability, energy consumption, and response time. Equally important is the capability of producing a more accurate system by using digital system processing. However, the methods of designing the controller entirely depend on the complexity of the system, and more in-depth knowledge in programming will certainly contribute to simpler yet more effective design.

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