Modeling the Impact of Multi-Fingering Microwave MOSFETs on the Source and Drain Resistances

Fabián Zárate-Rincón, Student Member, IEEE, Roberto S. Murphy-Arteaga, Senior Member, IEEE, Reydezel Torres-Torres, Member, IEEE, Adelmo Ortiz-Conde, Senior Member, IEEE, and Francisco J. García-Sánchez, Senior Member, IEEE

Abstract—Modern MOSFETs operated at high frequencies are designed and fabricated using a multi-fingered structure to enhance performance, especially to reduce gate resistance. However, even though the layout-dependent effect of other parasitics, such as that related to the source and drain resistances, is becoming more important, it has not been extensively investigated at high frequencies. In this paper, source and drain resistances are experimentally determined and analyzed for several microwave MOSFETs to characterize their corresponding dependence on the layout. This allows for the quantification and modeling of the impact of the device’s geometry on its parasitic extrinsic parameters. Physically based closed-form equations are proposed here to accurately represent S-parameters of MOSFETs operating at microwave frequencies with layouts considering different numbers of gate fingers, and grouping devices in cells with multiple source and drain junctions. The proposed models are compatible with SPICE-like circuit simulators, and an excellent model-experiment correlation is obtained when using the proposed scalable equations to represent different geometry MOSFETs up to 60 GHz.

Index Terms—Microwave modeling, parameter extraction, RF-CMOS, S-parameters.

I. INTRODUCTION

MICROWAVE MOSFETs present special features to enable CMOS technology to operate at high frequencies [1]. One of these features is to increase the capacity to handle the drain current while minimizing the device’s parasitics by increasing the total gate width using multi-fingered geometries. This approach has been widely used for many years since it allows a considerable reduction of the gate resistance ($R_g$). The importance of reducing $R_g$ relies on the fact that this parameter negatively impacts figures-of-merit such as the noise figure and the maximum frequency of oscillation [2]–[4]. Consequently, much research has been dedicated to characterize and represent this important parameter for modeling purposes [5], [6], but also to provide information to develop improved devices [7]. In fact, models that allow for an adequate representation of $R_g$ for different geometries, including multi-cell and double-sided gate electrodes, are available in the literature [8]. In this regard, some research on the geometry dependence of the substrate resistance has been carried out [9], [10]. Nonetheless, in spite of the fact that the geometry dependence of other extrinsic parameters, such as the drain and source series resistances and junction capacitances, is also becoming important for advanced devices [11], scalable models for these parameters still need to be developed. Among the reasons that make the development of geometry-dependent models for the extrinsic impedances important—in addition to $R_g$—we highlight the corresponding impact on the MOSFET’s input and output features [12], [13]. High-frequency models are required to accurately represent the variation of these impedances with the number of fingers ($N_f$) present in the device without assuming constant values for fixed total channel widths.

Experimental S-parameter measurements can be used to develop scalable models for the extrinsic MOSFET elements since the model parameters can be obtained using a single device without involving data regressions requiring either devices with different geometries or multiple bias points [14]–[17]. This represents an advantage over dc methods that need several devices varying in the gate length. Thus, when the extracted parameters obtained from S-parameter measurements are analyzed for devices with different geometries, geometry-dependent models can be developed even including bias-dependent components. In this regard, in [18] RF-MOSFETs with different number of fingers are characterized, focusing on the effects that become apparent as the channel width becomes narrower. For simplicity, in [18], the effects of the series parasitics are not taken into account, which makes further investigation in this direction necessary.

In our previous work on multi-fingered transistors in a 90-nm technology node [19], we presented the effect of the number of fingers on the series parasitic resistances when the total gate area is fixed. In that paper, we describe how the source, drain, and gate resistances decrease with the number of fingers and pointed out the importance of developing a model to describe this behavior.

In this work, MOSFETs designed to be operated within the range of tens of gigahertz are exhaustively characterized to identify the impact of geometry on their extrinsic elements. This allows the development of closed-form equations to represent the...
parasitics associated with the drain and source resistances for devices with fixed total gate width and gate length, but having different number of fingers. Excellent S-parameter model-experiment correlations for devices with different number of fingers are achieved up to 60 GHz.

II. GEOMETRY OF A MICROWAVE MOSFET

To increase the transconductance and current-handling capacity of a MOSFET for a given gate length \( L_g \), the total gate width \( W_{\text{total}} \) has to be increased, which implies an increase in \( R_g \). To reduce this undesirable effect, the transistor is multi-fingered. Moreover, using a double-sided contacted gate electrode, a lower \( R_g \) can be achieved [4]. Additionally, if a very wide transistor is required, several cells corresponding to a multi-finger device can be connected in parallel to efficiently use the design area while allowing the use of scalable models. This is convenient since the resistances between single cells do not significantly increase the source \( R_s \) and drain \( R_d \) resistances, which is due to the fact that the cross-sectional area of the inter-cell interconnects is much larger than \( L_g \) and \( W_{\text{total}} \)[12], [13]. In addition, it is important to remark that the substrate resistance varies with the number of cells \( N_f \) even though \( W_{\text{total}} \) is fixed.

In order to show the multi-cell layout concept, Fig. 1 presents the layout for a common source/bulk MOSFET designed to present \( W_{\text{total}} = 192 \mu \text{m} \), where \( N_f \) is 2, the number of fingers per cell \( (N_f) \) is 16, the finger width \( (W_f) \) is 6 \( \mu \text{m} \), and the number of vias \( (N_v) \) to contact each drain/source junction is 12. Moreover, Fig. 2 shows the resistance network that represents the distributed source resistance of a single cell, illustrating the cell resistances \( R_{\text{cell},s} \) and \( R_{\text{cell},d} \); in this case, the cell presents \( N_f = 4 \) and 3 vias per finger. In the distributed network used to represent the MOSFET’s source terminal in Fig. 2, \( R_{\text{met},s} \) and \( R_{\text{met},d} \) are the metal resistances, \( R_{\text{cont},s} \) is the contact resistance, and \( R_{\text{series},s} \) includes the effect of the resistances associated with the highly doped drain (HDD) and lightly doped drain (LDD) regions (i.e., \( R_{\text{series},s} = R_{\text{HDD},s} + R_{\text{LDD},s} \)). In a similar fashion, the resistance network of the drain terminal can be represented by the substitution of the subscript \( s \) for \( d \).

The representation of a multi-fingered MOSFET that allows for the analysis of the impact of the undesired extrinsic parasitics assumes that each finger is associated with a single device, whose terminal resistances can be considered externally. Hence, these devices can be connected in accordance with Fig. 3 to represent the complete MOSFET. Notice that the equivalent circuit includes the effect of \( R_{\text{seris},s} \) and \( R_{\text{series},d} \) and of the series external resistances \( (R_{\text{seris},s} \text{ and } R_{\text{seris},d} ) \) by considering that the terminals of adjacent single devices share the parasitic component. Thus, in the case of the source, \( R_{\text{cell},s} \) corresponds to the equivalent resistance for the circuit formed by \( R_{\text{seris},s}, R_{\text{met},s}, R_{\text{cont},s} \), and \( R_{\text{seris},s} \). In addition, \( R_{\text{cell},s} \) and \( R_{\text{cell},d} \) can be divided into two resistances, each one where the source or drain are shared between single transistors. This can be done due to device symmetry, which allows to place the equivalent circuits of each finger in parallel, as shown in Fig. 3.

Accordingly, the total number of vias and the total source/drain area in multi-finger MOSFETs are smaller than for single-finger devices. This fact permits the reduction of \( R_{\text{seris},s} \) or \( R_{\text{seris},d} \) through the use of a multi-finger transistor since they become significant in nanometer-scale devices as a consequence of the reduced channel resistance. Note that the distance between vias and their dimensions are equal for all structures maintaining constant \( R_{\text{met},s}, R_{\text{met},d}, \) and \( R_{\text{cont},s} \), whereas when \( N_f \) is modified, this number is different.

In fact, an increase in drain current \( (I_d) \) with \( N_f \), even when \( W_{\text{total}}\) and \( L_g \) are fixed, is observed, as shown in Fig. 4. This can be attributed to a change of the extrinsic geometry of the structure, which is more noticeable for higher gate–source voltages \( (V_{gs}) \). This behavior shows the importance of considering a scalable model for the variations, not only in \( R_s \) and \( R_d \) with the extrinsic geometry. In this case, the changing of \( R_s \) and \( R_d \) is mainly due to the bias-independent component since the bias-dependent component does not significantly vary. It is important to remark that the variations of the bias-dependent components, due to the LDD regions, are produced by the...
Fig. 3. Equivalent circuit for the two fingers of the right end of Fig. 2 considering the device symmetry.

Fig. 4. $I_d$ as a function of $V_g$, for different $N_f$ with a fixed total gate area.

difference between manufacturing processes. In addition, above a given $N_f$, high frequency and dc measurements are almost independent of this parameter due to the small change of the total number of vias and the total source/drain area.

As mentioned above, the microwave MOSFET layout can be represented by means of the parallel combination of the equivalent circuits of each finger. In fact, there are two fingers per cell that refer to the source regions in which vias are not shared between adjacent single devices and $N_f = 2$ fingers per cell that are the opposite. Thus, the total resistance ($R_{\text{total,cell}}$) between the source and drain terminals per cell is given by

$$R_{\text{total,cell}} = \frac{R_1 + 2R_{\text{ext,s}}}{N_f - 2} \left( R_2 + R_{\text{ext,d}} \right)$$  \hspace{1cm} (1)

where $R_1 = R_{\text{series,s}} + R_{\text{series,d}} + R_{\text{ch}} + 2R_{\text{ext,s}}$ and $R_{\text{ch}}$ is the channel resistance. In the case of a microwave MOSFET with two cells, the total resistance ($R_{\text{total}}$) is the following:

$$R_{\text{total}} = \frac{R_1 + 2R_{\text{ext,s}}}{N_f - 2} \left( \frac{R_1 + R_{\text{ext,d}}}{2} \right) + R_{\text{cell,s}} + R_{\text{cell,d}}$$  \hspace{1cm} (2)

This can be rewritten for several cells as follows:

$$R_{\text{total}} \approx \frac{R_1 + 2R_{\text{ext,s}}}{N_c (N_f - 2)} \left( R_1 + R_{\text{ext,d}} \right)$$

$$\approx \frac{(R_3 + R_{\text{ext,s}})}{N_c (2R_{\text{ext,d}} + N_f (R_1 + R_{\text{ext,d}}))}.$$  \hspace{1cm} (3)

In turn, $N_f (R_1 + R_{\text{ext,d}})$ is greater than $2R_{\text{ext,d}}$, which allows us to simplify (3). This is true since $N_f$ is often of the order of tens; $R_1$ and $R_{\text{ext}}$ are of the order of units and fractions of ohms, respectively. Thus, for instance for one of the considered devices, $N_f (R_1 + R_{\text{ext,d}})$ is more or less 11 $\Omega$ and $2R_{\text{ext,d}}$, 0.2 $\Omega$. In this way, it is valid that (3) can be rewritten as

$$R_{\text{total}} \approx \frac{R_1}{N_f N_c} + \frac{2R_{\text{ext,d}}}{N_f N_c}$$  \hspace{1cm} (4)

with

$$R_{\text{ext,s}} = \frac{A}{B} + R_{\text{met,2,s}}$$  \hspace{1cm} (5)

for the case of the source terminal, as shown in Fig. 5. The parameters $A$ and $B$ are given by

$$\frac{A}{R_{\text{cont,s}}} = N_c (N_f - 1) + \sum_{i=1}^{N_c} \left[ \frac{R_{\text{cont,s}}}{(2i)!} \prod_{j=-i}^{i-1} (N_c + j) \right] \hspace{1cm} (6)$$

and

$$B = \sum_{k=1}^{N_c} \left[ \frac{R_{\text{cont,s}}}{(2k-1)!} \prod_{i=-k+1}^{k-1} (N_c + i) \right].$$  \hspace{1cm} (7)

However, these equations are not practical to fit the experimental data. In order to simplify them, the assumption that $R_{\text{met,2,s}}$ is much smaller than $R_{\text{cont,s}}$ can be considered. Here, $R_{\text{cont,s}}$ consists of the resistance of the metal-to-semiconductor interface. Thus, the term $R_{\text{met,2,s}}$ can be neglected when its exponent is greater than 2.
and
\[
A \approx R_{\text{cont,s}}^{-1} + \frac{R_{\text{cont,s}}^{-2}R_{\text{met,s}}}{2} \left( N_v - 1 \right) N_v + \frac{R_{\text{cont,s}}^{-3}R_{\text{met,s}}^2}{24} \left( N_v - 2 \right) \left( N_v - 1 \right) N_v \left( N_v + 1 \right)
\]  
(8)

and
\[
B \approx R_{\text{cont,s}}^{-1} N_v + \frac{R_{\text{cont,s}}^{-2}R_{\text{met,s}}}{6} \left( N_v - 1 \right) N_v \left( N_v + 1 \right) + \frac{R_{\text{cont,s}}^{-3}R_{\text{met,s}}^2}{120} \left( N_v - 2 \right) \left( N_v - 1 \right) N_v \left( N_v + 1 \right) + \left( N_v + 2 \right)
\]  
(9)

where \( N_v = (\beta W_{\text{total}})/N_fN_c \), \( \beta \) is the number of vias per unit length, which is a constant, and \( N_v \geq 3 \). In this work, \( \beta \) is equal to two vias per 1 \( \mu m \). In this way, \( R_s \) and \( R_d \) resistances can be determined by
\[
R_s(V_{gs}, N_f) = \frac{R_{\text{LDD,s}}}{N_fN_c} + \frac{R_{\text{HDD,s}}}{N_fN_c} + \frac{2R_{\text{ext,s}}}{N_fN_c}
\]  
(10)

\[
R_d(V_{gs}, N_f) = \frac{R_{\text{LDD,d}}}{N_fN_c} + \frac{R_{\text{HDD,d}}}{N_fN_c} + \frac{2R_{\text{ext,d}}}{N_fN_c}
\]  
(11)

In our particular case, \( W_{\text{total}} \), which is equal to the product \( N_fN_cW_f \), is fixed to a given value, and thus, \( W_f \) decreases when \( N_f \) increases at the same rate. Similarly, \( R_{\text{LDD}} \) and \( R_{\text{HDD}} \) increase with the inverse of \( W_f \). Therefore, the terms \( R_{\text{LDD}}/N_fN_c \) and \( R_{\text{HDD}}/N_fN_c \) are independent of \( N_f \). \( R_{\text{HDD}} \) is bias independent, while \( R_{\text{LDD}} \) has two components, one of which is bias independent and the other is bias dependent (i.e., the part of the LDD region under the gate). Based on this, \( R_s \) and \( R_d \) can be rewritten as
\[
R_s(V_{gs}, N_f) = \frac{v_{s,s}}{V_{gs} - V_{th}} + R_{\text{ind,s}} + \frac{2R_{\text{ext,s}}}{N_fN_c}
\]  
(12)

\[
R_d(V_{gs}, N_f) = \frac{v_{d,d}}{V_{gs} - V_{th}} + R_{\text{ind,d}} + \frac{2R_{\text{ext,d}}}{N_fN_c}
\]  
(13)

where \( v \) is a parameter that takes into account the bias-dependent resistance due to the LDD regions under the gate [21]; \( V_{gs} \) is the gate–source voltage; \( V_{th} \) is the threshold voltage; \( R_{\text{ind}} \) is the bias-independent resistance, attributed to the HDD region and the part of the LDD region that is not under the gate; and the subscripts \( s \) and \( d \) denote the source and drain regions, respectively. Equations (12) and (13) allow the behavior of series parasitic resistances in microwave MOSFETs to be accurately modeled.

III. EXPERIMENT

Two-port \( S \)-parameter measurements of microwave MOSFETs were performed up to 60 GHz at different bias conditions, using a vector network analyzer (VNA) and a semiconductor device analyzer (SDA), as presented in Fig. 6. Fig. 7 shows a micrograph of one of the transistors used in this study, which were measured using ground–signal–ground coplanar probes with a 100-\( \mu m \) pitch, as depicted in Fig. 8. Before device measurements, the system was calibrated with the line–reflect–match procedure. Transistors with different \( N_f \) were then measured.

Fig. 6. Experimental setup used to perform RF Measurements under Different Bias Conditions, Illustrating the SDA, VNA, and Device-under-Test (DUT). (a) Photograph. (b) Schematic.

Fig. 7. Micrograph of one of the considered transistors.
with $N_f$ varying from 4 to 32. It is important to note that the total gate width ($W_{\text{total}}$) and gate length ($L_g$) are the same for all devices, fixed at 192 $\mu$m and 80 nm, respectively. One would thus expect the series parasitic resistances to depend on the number of fingers. In these devices, the source and bulk terminals are grounded since the transistors are configured in common bulk/source. Additionally, the process is based on shallow trench isolation (STI) to prevent leakage currents, and have LDD regions in both source and drain sides to reduce hot carrier effects. Before interpreting the experimental data, the pad parasitic effects were removed using a de-embedding technique for which open and short-all structures were measured [20].

**IV. VARIATION OF THE EXTRINSIC PARAMETERS WITH THE NUMBER OF FINGERS**

Before extracting $R_s$ and $R_d$ from high-frequency measurements, the substrate parasitic network has to be removed from the experimental data. This is done biasing the transistor in the cold condition, $V_{gs} = 0$ V and $V_{th} = 0$ V, following the procedure in [22]. $R_s$ and $R_d$ are then found when the transistor is biased at $V_{gs}$ greater than $V_{th}$, which is equal to 0.38 V for the measured devices. Therefore, the inversion channel is formed under the gate and the channel resistance ($R_{ch}$) becomes comparable to the source and drain resistances. Measurements indicate that $R_s$ and $R_d$ decrease with $N_f$ and $V_{gs}$, as shown in Figs. 9 and 10. This is due to the reduction of the number of vias when the transistor is folded, and due to the variation of carrier concentration in the LDD regions under the gate. This means that the drain current increases with $N_f$. However, one expects the drain current to be the same for all the transistors since the total gate width and gate length do not change. It is evident then that the variation of the series parasitic resistances with the extrinsic geometry cannot be neglected. The comparison of parasitic resistances in the source and drain between the extracted values and model are performed for different $N_f$ and $V_{gs}$, at drain–source voltage ($V_{ds}$) equal to zero, which allows the correct characterization of these components.

After fitting the experimental data in Figs. 9 and 10 by means of the Levenberg–Marquardt algorithm, it is possible to obtain the unknown variables of (12) and (13). In the case of the source, the following values were derived: $R_{cont,d} = 69.4$ $\Omega$, $R_{pref,d} = 0.1$ $\Omega$, $R_{pref,s} = 0.05$ $\Omega$, $R_{ind,s} = 0.08$ $\Omega$, and $v_{ds} = 0.3$ $\Omega$. On the other hand, the given values for the drain are $R_{cont,d} = 67.1$ $\Omega$, $R_{pref,d} = 0.06$ $\Omega$, $R_{pref,s} = 0.05$ $\Omega$, $R_{ind,d} = 0.08$ $\Omega$, and $v_{ds} = 0.3$ $\Omega$. The extracted resistance values $R_{cont}$ and $R_{pref}$ validate the assumption in (8) and (9) in which $R_{cont}$ is much smaller than $R_{pref}$.

The variation of $R_s$, $R_d$ and gate resistance ($R_g$) can be observed in the S-parameter measurements of the input ($S_{11}$) and output ($S_{22}$) ports. This is illustrated in Figs. 11–13, for which the measurements were taken at $V_{gs} = 0.58$ V and $V_{th} = 0$ V. From these figures, it is evident that the assumption of constant $R_s$, $R_d$, and $R_g$ does not allow to match the experimental data. This bias condition guarantees that the transistor is in strong

![Fig. 8. DUT, indicating the ground–signal–ground probes.](image)

![Fig. 9. Fit of the source resistance against total number of fingers with different $V_{gs}$ at $V_{th} = 0$ V.](image)

![Fig. 10. Fit of the drain resistance against total number of fingers with different $V_{gs}$ at $V_{th} = 0$ V.](image)

![Fig. 11. Simulated and experimental $S_{11}$ of microwave MOSFETs for different number of fingers at $V_{gs} = 0.58$ V and $V_{th} = 0$ V. The curve with diamonds corresponds to the simulation of the MOSFET with the obtained average values of $R_s$, $R_d$, and $R_g$.](image)
Fig. 12. Simulated and experimental $S_{22}$ of microwave MOSFETs for different number of fingers at $V_{gs} = 0.58$ V and $V_{ds} = 0$ V. The curve with diamonds corresponds to the simulation of the MOSFET with the obtained average values of $R_s$, $R_d$, and $R_g$.

Fig. 13. Simulated and experimental phase of microwave MOSFETs for different number of fingers at $V_{gs} = 0.58$ V and $V_{ds} = 0$ V. The curve with diamonds corresponds to the simulation of the MOSFET with the obtained average values of $R_s$, $R_d$, and $R_g$.

Fig. 14. Simulated and experimental $S_{11}$, and $1.3S_{22}$ of microwave MOSFETs for different number of fingers at $V_{gs} = 0$ 50 V and $V_{ds} = 0.7$ V. The curve with diamonds corresponds to the simulation of the MOSFET with the obtained average values of $R_s$, $R_d$, and $R_g$.

inversion since $V_{gs}$ is greater than $V_{th}$, and thus, the gate resistance affects mainly $S_{11}$ and source and drain resistances impact $S_{22}$. This is a consequence of the reduction of the channel resistance when the device is scaled down. It also shows the importance of considering the variation of the parasitic resistances with extrinsic geometry at high frequency. Additionally, it can be observed that the $S$-parameters do not significantly change for different transistors with fixed total width and a large number of fingers.

For practical applications, the transistor is biased in strong inversion at different values of $V_{gs}$. Thus, the comparison between the experimental data and the model for the transistor in the active region is mandatory. For instance, the $S$-parameters of input and output ports up to 60 GHz at $V_{gs} = 0.50$ V and $V_{ds} = 0.7$ V are presented in Fig. 14. It is important to note that channel resistance increases with $V_{th}$ due to the increase of the depletion region associated with the drain.

V. CONCLUSION

The work presented in this paper has demonstrated the importance of considering extrinsic source and drain series resistances when designing and simulating RF circuits based on multi-fingered MOSFETs. Neglecting their influence can lead to misrepresenting the $S$-parameters of the transistor and the associated derived quantities. A model to represent the behavior of source and drain resistances for microwave MOSFETs with different number of fingers, but equal total gate area was herein presented. This model, which incorporates the geometry dependence, shows an excellent correlation to experimental data, and highlights the effects affecting multi-fingered structures, especially when the number of fingers is small. Clearly, as frequency of operation increases, the influence of these extrinsic components has to be taken into account in order to improve the design and simulation stages of RF circuits based on the MOSFET.

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