Design and comparison of Single Bit SRAM Cell Under different Configurations

Dr. A. Q. Ansari[1] and Javed Akhtar Ansari [2]

[1,2] Dept. of Electrical Engineering ,Jamia Millia Islamia, New Delhi,India

E-mail:[1] aqansari62@yahoo.co.in, [2]javed.mbk@gmail.com

ABSTRACT

Memory is widely used in all electrical systems mainframes microcomputers and cellular phones etc. From the last more than five decades we are scaling down the size of the CMOS devices to make the devices portable and compact in size and to get better performance in terms of access time, power dissipation, delay etc. More memory means more information therefore more size and so more power consumption. Thus the demand for low size and low power memory has been raised. Working of low supply voltage and leakage energy has become main concern as the power consumption can be reduced significantly. We, in our work have designed the low power SRAM memory cells, which are used to store single bit information, under different configurations (6T, 8T, 9T) and compared various parameters of these cells. We have carried out the simulation work using Tanner SPICE. However, there is no universal way to avoid trade-offs between the power, delay and area. This is why; the designers are required to choose appropriate techniques that satisfy application and product needs.

Keywords: SRAM, Access Time, Power Dissipation

INTRODUCTION

STANDARD 6T SRAM CELL

The 6T bit cell is standard bit cell structure among the SRAM cells. It comprises of two cross coupled CMOS inverters (M1-M4) and two access transistors. These access transistors connect the inverters to the bit lines for read and write operations. The schematic of the 6T SRAM cell is shown in fig 1. Storage nodes are denoted by Q and QB, WL denotes the word line and BL and BLB are bit lines.

Read Operation-

Both the bitlines are precharged to VDD.

The word line is set high and the access transistors M5 and M6 are turned ON . Thus storage nodes transfer data to the bit lines. This creates a small voltage difference between the voltages of the bit lines.

This voltage difference in the bit lines is measured with sense-amplifier and the output of the sense-amplifier is sent to the Data Out buffer. Depending on the difference in the voltage 1 or 0 is read.

Write Operation

The word line is set high and the access transistors transfer the data from the bit lines to the storage nodes. The bitlines BL and BLB are charged to logic '0' voltage and logic '1' voltage respectively.

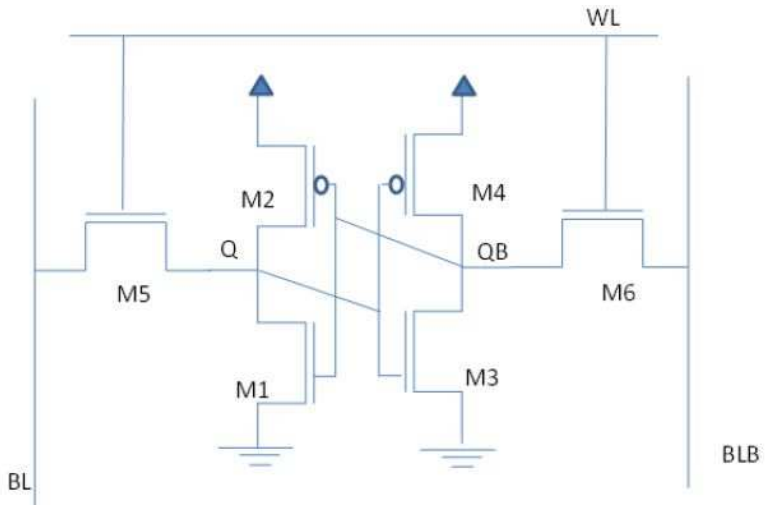

Fig. 1: Schematic of 6T SRAM cell

OTHER CONFIGURATIONS OF SRAM CELLS

Fig. 3 shows the 8T SRAM cell which is created by adding two more transistors; the read operation is entirely decoupled from the write operation by sensing the data through a separate read stack controlled by a separated read world line (RWL).

The 9T SRAM cell (Fig. 4), The upper part is a typical 6T SRAM cell. Write signal (WL) controls M5 and M6. The data is stored within this upper memory sub-circuit. The lower sub circuit of this 9T cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9) [1-2].

SIMULATION OF SRAM CELLS

The simulation work for all the SRAM cells is carried out using the Tanner SPICE tool 90nm technology [3-4].

6T SRAM CELL

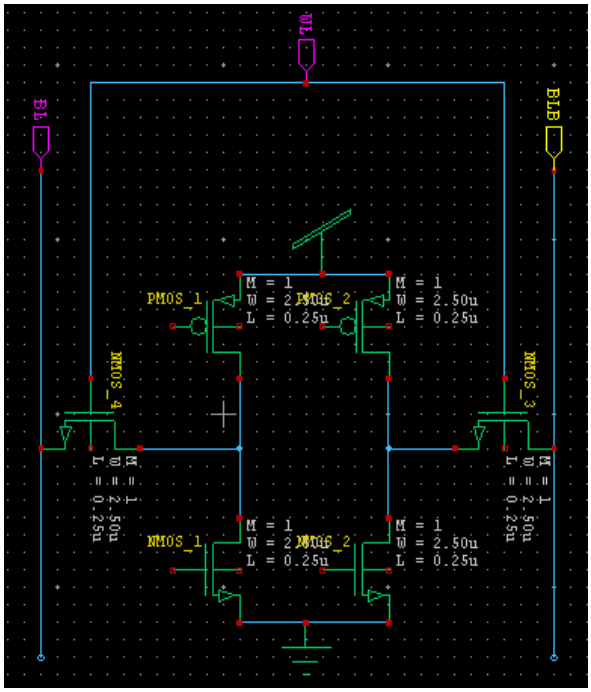

Fig. 2: 6T SRAM cell

8T SRAM CELL

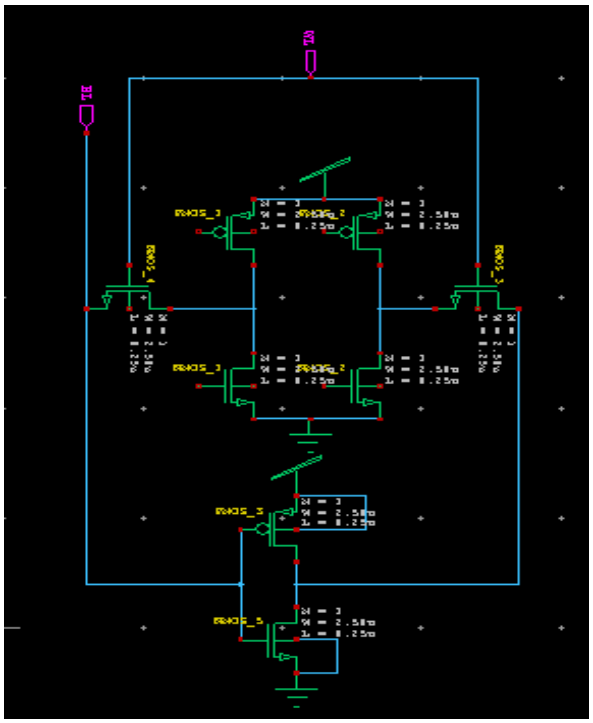

Fig. 3: 8T SRAM cell

9T SRAM CELL

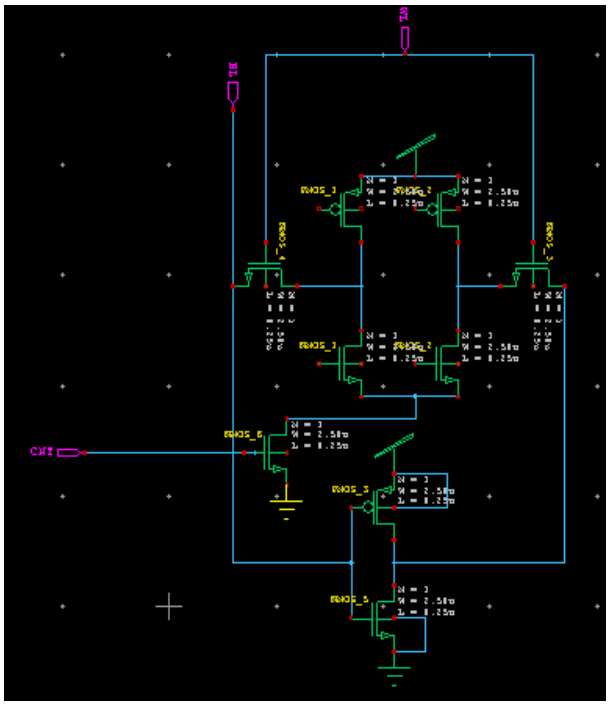

Fig. 4: 9T SRAM cell

SIMULATION RESULTS OF SRAM CELLS

6T SRAM CELL

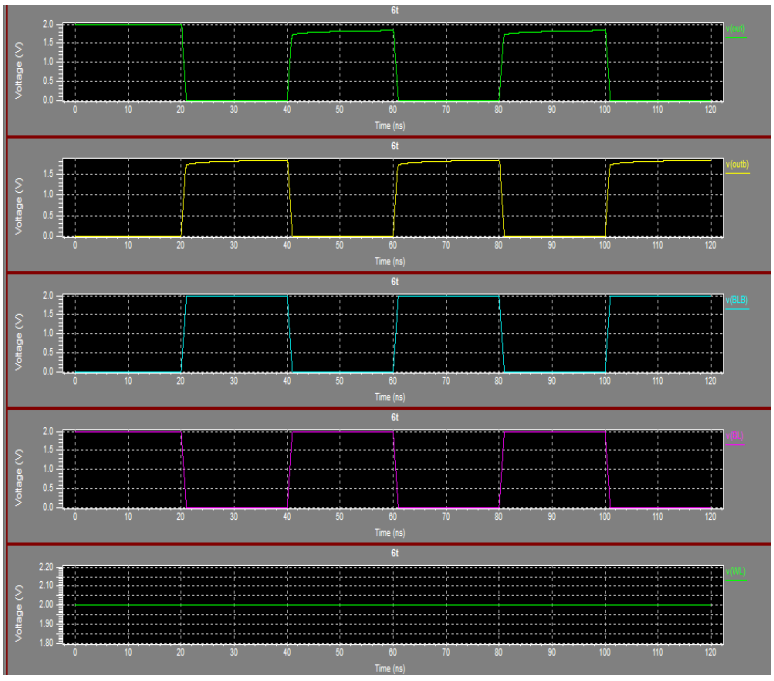

Fig. 5: Simulation result of 6T SRAM cell

8T SRAM CELL

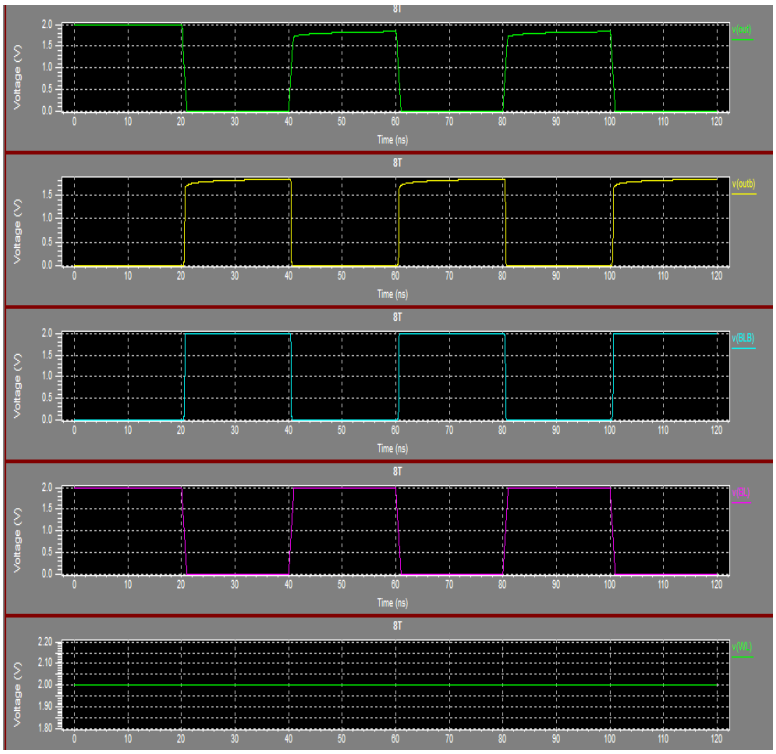

Fig. 6: Simulation result of 8T SRAM cell

9T SRAM CELL

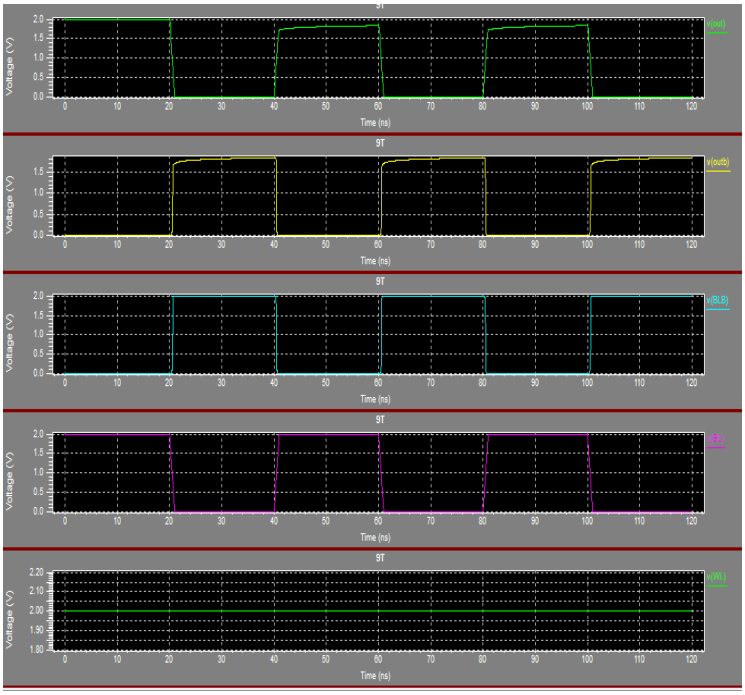

Fig. 7: Simulation result of 9T SRAM cell

Table 1: Values Of Power Consumption And Propogation Delay Of Different Cell

SRAM cell	Power Consumption (in nW)	Propagation Delay (in ns)
6T	63.05	0.06
8T	80.35	0.17
9T	31.45	1.02

CONCLUSION

The simulation work for 6T, 8T and 9T memory cell is done using the Tanner SPICE tool in 90nm technology. From the results it is observed that the propagation delay of the memory cells is increased as the number of transistors is increased also the area is increased. Power consumption of 9T cell is half of the 6T cell. 8T and 9T cells are more stable than 6T cell as read and write operation is entirely decoupled from each other. The trade-offs between different configurations of SRAM cells cannot be avoided so we choose appropriate technology as per the application.

REFERENCES

[1] Deepak Aggarwal, Praveen kaushik and Narender Gujran, "A Comparative Study of 6T, 8T and 9T SRAM Cell" International Journal of Latest Trends in Engineering and Technology (IJLTET), Vol. 1 Issue 2 July 2012.

[2] Paridhi Athe S. Dasgupta "A Comparative Study of 6T, 8T and 9T Decanano SRAM cell" *2009 IEEE Symposium on Industrial Electonics and Applications (ISIEA 2009)*, October 4-6, 2009.

[3] Kaur Simran, and Kumar Ashwani, "Analysis of Low Power SRAM Memory Cell using Tanner Tool," *IJECT International Journal Of Electronics & Communication Technologies, V*ol. 3, Issue 1, Jan.–Mar. 2012, pp. 80-84.

[4] Ashish Siwach, Rahul Rishi," Asymmetric SRAM- Power Dissipation and Delay" IJCEM International Journal of Computational Engineering & Management Vol.11, pp.28-31, january 2011.

[5] A. Q. Ansari, "Multiple Valued Logic Versus Binary Logic," *C. S. I. Communications*, India, Vol.20, No.5, pp.30 – 31, November 1996.

[6] M Ayoub Khan, A Q Ansari, "*A Journey from Computer Networks to Networks-on-Chip*". IEEE Beacon, Vol. 31, No. 1, pp. 71-77, March 2012.

[7] M. A. Khan, A. Q. Ansari, "n-Bit Multiple Read and Write FIFO Memory Model for Network-on-Chip," *Proc. World Congress on Information and Communication Technology* (WICT 2012), Mumbai, pp. 1322 – 1327, Dec. 2011,

[8] A. Q. Ansari, Neeraj Gupta, "MIPS-NF Instructions for Fourth Generation Processor," *Proc. 2nd IEEE Conf. on Comp., Control, and Comm.*, Pakistan, pp. 01 – 05, February 2009.

[9] Anwar Jamil, A. Q. Ansari, and Ranjit Biswas, "A Proposal for a New Generation of Computers," *Proc. International Conference on Fuzzy Theory and Technology*, U.S.A., pp. 97 – 100, March 2002.

[10] A. Q. Ansari, "Development of a Switch-Level Simulator for Ternary Logic Circuits," *Proc. National Conference on Technology Convergence for Information, Communication, and Entertainment* (NICE'2001), IETE, Cochin, India, pp.141-144, February 23 –24, 2001.