CMOS upconversion mixer with filterless carrier feedthrough
cancellation and output power tuning

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A B S T R A C T

The synthesis, design and implementation of a CMOS upconversion mixer that both can adjust, by means of a DC voltage control, its output power and that cancels the carrier feedthrough is presented. Aiming at very low cost medical implant applications, a prototype of the architecture was implemented in a double poly, three metal layers, 0.5 µm CMOS technology. For a range between one half and one fifth of the supply voltage, the circuit can decrease in a quadratic form the power delivered to the load until one forth of its maximum value by varying the DC component at the baseband signal. In addition, a large IIP3 is attained since the closest high order intermodulation product present in the spectrum of the signal is far from the vicinity of the component of interest.

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1. Introduction

Direct-up transmitters are the architecture of choice in diverse wireless communication technologies such as GSM/DCS/PCS/EDGE, Wi-Fi, HiperLAN, Bluetooth, UWB, ZigBee, CDMA/WCDMA/AMPS/GPS, WiMAX and MedRadio, to name a few [1,2]. Frequency translation of the baseband (BB) spectrum to the RF frequency in direct-up transmitters is performed in one step by an upconversion mixer (UCM). In general terms, the usual metrics to evaluate the performance of mixers are: conversion factor, noise figure, isolation among the ports, linearity and power consumption [3]. From those, port isolation and noise requirements are of major interest in downconversion mixers and more relaxed for UCMs. Nevertheless, linearity in UCMs is important since these are on the transmission path and the linearity of the overall transmitter is one of the most stringent demands to satisfy [4]. Consequently, UCMs are preferable to produce as few distortion as possible. Moreover, carrier feedthrough is also a relevant issue in UCMs; this phenomenon occurs when a DC component in the BB is mixed with the fundamental frequency of the local oscillator (LO). Both linearity and carrier feedthrough can be minimized by using UCMs based on passive topologies [5].

In addition, differential architectures improve the linearity of the UCM by canceling the even-order harmonic components.

A UCM usually precedes a power amplifier (PA) in the transmitter chain. Key aspects in the UCM should be then delivering a sufficient power level to drive the PA and controlling the conduction angle of its output waveform. Instead, the concerns entailed by the interface of UCMs and PAs are mainly focused in the ability of the UCM for driving the input capacitance of the PA, and the conversion of the differential waveforms from the mixer into a single-ended signal at the input of the amplifier. Such practice is appropriate in wireless transmitters where the output power requirement is high inasmuch as whenever it is necessary to add up more power gain, the use of a PA driver as the interceder between the UCM and the PA can be established. However, some other wirelesss technologies demand a smaller output power, and thus, the UCM drives directly the PA or even the antenna [6], involving the inclusion of output power regulation and conduction angle adjustment within the Figures of Merit (FOMs) of the mixer.

This paper is organized as follows: a CMOS UCM that can adjust by means of a DC voltage control the pulse width of the waveform at its output port and that can regulate both, its output power and power consumption, is introduced in Section 2. Section 3 describes a circuit implementation of the proposed CMOS UCM in a double poly, three metal layers, 0.5 µm CMOS technology: this implementation aims at very low cost applications in medical implants and satisfies the performance demands of the Medical Implant.
2. CMOS UCM with LO cancelation and output power tuning

There are basically two ways to accomplish frequency translation of a baseband signal. The first method is by means of a non-linear circuit whose non-linearities generate harmonics and intermodulation (IM) products. The second possibility is with the use of a time variant circuit. Time variant circuits undergo response variation with a strong dependence on time, such as switched circuits. The use of hard switching yields a wide spectrum, composed of mixing products of the baseband signal with all harmonics of the switching signal. Switched circuits, also known as harmonic mixers, are used in transceivers to down convert and up convert the RF and BB signals [5]. Since harmonic mixers possess a low self-mixing DC offset, these are attractive for zero-IF transmitters, with the drawback of a typically low conversion gain [1]. The starting point in the synthesis of a CMOS UCM with ideally suppressed carrier feedthrough is therefore based on time variant circuits.

Fig. 1 depicts a simple CMOS circuit with two load capacitors, \( C_L \), and four transistor, \( M_{N1}, M_{N2}, M_{P1}, \) and \( M_{P2} \), driven like switches. The circuit has similarities with the H-Bridge ring mixer in [7], except that the LO in [7] is provided as a common mode signal for the two symmetrical parts of the circuit in Fig. 1 whereas in the current work the BB is provided differentially to the source of the PMOS devices. The square wave \( V_{LO}(t) \) is generated by a local oscillator (LO) and controls the action of all the switches such that when \( V_{LO}(t) \) is at a low logic value, both \( M_{P1} \) and \( M_{P2} \) behave like open switches whereas \( M_{N1} \) and \( M_{N2} \) act like closed switches leading to the charge of capacitors \( C_L \) at voltages \( V_{o+} = V_o + V_P \cos(\omega_{bb} t) \) and \( V_{o-} = V_o - V_P \cos(\omega_{bb} t) \). Where \( V_o \) is a DC voltage and the cosine waves are BB signals. On the other hand, when \( V_{LO}(t) \) is at a high logic value, the switches \( M_{P1} \) and \( M_{P2} \) are opened as the switches \( M_{N1} \) and \( M_{N2} \) are closed and consequently the capacitors \( C_L \) are discharged. This action can be mathematically described by

\[
\begin{align*}
V_{o+} &= [V_o + V_P \cos(\omega_{bb} t)](1 - V_{LO}(t)) \\
V_{o-} &= [V_o - V_P \cos(\omega_{bb} t)](1 - V_{LO}(t)) \\
V_{LO}(t) &= \begin{cases} 
0 & \text{for } 0 < t < T_{LO} / 2 \\
1 & \text{for } T_{LO} / 2 < t < T_{LO}
\end{cases}
\end{align*}
\]  

and \( T_{LO} \) is the period of the LO. For simplicity reasons, we assume a 50% duty cycle of the LO square wave.

If we expand \( V_{LO}(t) \) into its Fourier series, then the term \( 1 - V_{LO}(t) \) in expression (1) can be rewritten as [8]

\[
1 - V_{LO}(t) = \frac{1}{2} + \sum_{n=0}^{\infty} \frac{\sin([2(n+1)] \omega_{bb} t]}{(2n+1)\pi} \]  

(3)

By taking the output voltage of the circuit as the difference between \( V_o \), and \( V_{0-} \), i.e. \( V_{out} = V_o - V_{0-} \), and employing expression (3),

\[
V_{out} = V_P \cos(\omega_{bb} t) + \sum_{n=0}^{\infty} \left\{ \frac{V_P \sin([2(n+1)] \omega_{bb} t]}{(2n+1)\pi} \right\}
\]  

(4)

Consequently, the spectrum of the output voltage contains the BB, the component of interest \( (\omega_{bb} + \omega_{LO}) \), its image \( (\omega_{bb} - \omega_{LO}) \), and the high order intermodulation (IM) odd products. Fig. 2 shows the input and output waveforms of the switched CMOS circuit in both time and frequency domain, for the case of an LO signal 10 times faster than the BB. It is concluded that the circuit of Fig. 1 exhibits the behavior of an UCM without carrier feedthrough. Further cancelation of the image can be performed by at least three methods: using a bandpass filter to select the upper-sideband; by means of a Weaver transmitter (TX) architecture, where the inputs are in quadrature and afterwards the upconversion the signals are combined to produce a single-sideband spectrum [5]; or dividing the upconverter into a polyphase multipath system like the one proposed in [6], where image components are always canceled.

Linearity can be easily estimated with the aid of (4). If we take the difference of power \( (\Delta P) \) between the component of interest, \( (\omega_{bb} + \omega_{LO}) \), and the closest high order IM product, which in this case is \( (3\omega_{bb} - \omega_{LO}) \), the input third intercept point (IIP3) is expressed as [5]

\[
IIP_3 = \frac{\Delta P_{dB}}{2} + P_{in dBm}
\]  

(5)

where \( P_{in} \) is the input power of the BB.

On the other hand, considering the rms value of the cosine waves at base band frequency (BB), the average energy stored on each load capacitor, \( C_L \), during half period of the LO, is given by \( C_L \left(V_o^2 + V_P^2/2 \right)/2 \) [9]. Thus, in a complete switching cycle of the LO, the average power delivered to both load capacitors, \( P_{out} \), is expressed as [10]

\[
P_{out} = f_{LO} C_L \left(V_o^2 + V_P^2/2 \right)
\]  

(6)

where \( f_{LO} \) is the fundamental frequency of the LO.

In a similar way, it can be proved that the average power provided by the BB sources, \( P_{in} \), is given by

\[
P_{in} = f_{LO} 2C_L \left(V_o^2 + V_P^2/2 \right)
\]  

(7)

Combining (5) and (6), the conversion factor (CF) defined as the ratio between the output and input power, results in

\[
CF = \frac{P_{out}}{P_{in}} \approx -3 \, dB
\]  

(8)

Therefore, just half the input power is translated to the output port of the mixer. When PMOS and NMOS transistors are interconnected and driven like an inverter logic gate, just like those in Fig. 1, the power delivered by the power supply is dissipated.
dynamically. The leakage power contributes only in a small portion to the total power consumption and the short-circuit dissipation becomes smaller when the load capacitances increases [11]. Hence, the average dynamic power dissipated in differential form, $P_D$, is

$$P_D = f_{LO} 2C_L \left( V_b^2 + \frac{V_P^2}{2} \right)$$  \hspace{1cm} (9)

and consequently, the efficiency ($\eta_D$) of the circuit [12]

$$\eta_D = \frac{P_{out}}{P_D} = 50\%$$  \hspace{1cm} (10)

Thus, $\eta_D$ of the proposed upconverter is similar to that of a class A PA [12].

3. Circuit implementation example

Fig. 3 shows the block diagram of the MICS [13]. As can be appreciated, the transceiver (TRX) in the medical implant (right hand side) establishes a link with the base station at both frequency bands, 2.45 GHz and 400 MHz. The higher frequency link sets up a wake-up process to save power since MICS systems spend most of their time asleep and, periodically, the implant should scan for an external programmer which wants to begin communication [14]. On the other hand, the 400 MHz link is used to monitoring activity of the implant. Such RF frequency is well suited for this service because of the signal propagation characteristics in the human body and its international availability [14–16]. Some of the most salient features of the MICS are summarized in Table 1 [15]. Besides data transmission reliability, typically expressed in a robust bit error rate (BER), a TX intended for being used in the MICS must exhibit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency band</td>
<td>402–405 MHz</td>
</tr>
<tr>
<td>Channel bandwidth</td>
<td>300 kHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>&gt;250 Kbps</td>
</tr>
<tr>
<td>Modulation scheme</td>
<td>FSK</td>
</tr>
<tr>
<td>Transmit power</td>
<td>25 µW (−16 dBm)</td>
</tr>
<tr>
<td>Range</td>
<td>~2m</td>
</tr>
</tbody>
</table>

**Table 1**

MICS specifications.
a very low power consumption, to be highly integrated with minimal external components for small form factor, and to have channel selectivity within the 402–405 MHz band [2]. Therefore, the UCM introduced in the previous section can be employed as a power upconverter in the 400 MHz RF section of the MICS TX of Fig. 3 since its high order IM products and, by an appropriate selection of the BB frequency, the image component are far from the RF band. In addition, the output power of the proposed circuit as well as its power consumption can be modulated by the $V_b$ DC voltage.

The CMOS power upconverter of Fig. 4 was designed and implemented in a double poly, three metal layers, 0.5 $\mu$m CMOS technology from MOSIS foundry to verify the performance and effectiveness of the introduced UCM. With a unity-gain frequency, $f_1$, of $\sim$2.4 GHz, this technology is fast enough to satisfy the RF frequency demand of the MICS. Some other RF designs have been successfully accomplished, in recent years, in 0.5 $\mu$m CMOS technology, such as the case of those reported in [17–20]. The presented results in those publications demonstrate the feasibility of the 0.5 $\mu$m CMOS technology as well as its validity in the realization of RF-IC. To maximize the experimental flexibility, a chain of inverters built up with transistors $M_{PB1}$-$M_{NB1}$ to $M_{PB8}$-$M_{NB8}$ was employed to compose a pair of buffers which convert the sinusoidal input, $V_{LO}(t)$, from the RF signal generator into the driving square wave, in our test chip, of the differential mixer formed by the switched transistors $M_{P1}$, $M_{P2}$, $M_{N1}$ and $M_{N2}$ along with the devices $M_{S1}$ and $M_{S2}$, biased to operate as modulated resistors in the linear region. The balun between the antenna (a 50 $\Omega$ resistive load) and the UCM is an external wideband RF transformer with 1:1 impedance ratio.

Dimensioning of the circuit, especially the mixer, was done considering the fulfillment of the RF band of the MICS and in order to have more experimental freedom the power upconverter was sized to achieve output power beyond the limit allowed by the MICS specifications. However, it is important to remark the fact that the key aim of the chip was to demonstrate the feasibility of the UCM core. Wide switch transistors are beneficial to reduce the static power dissipation in the switches but require more power in the driver buffers. Those tradeoffs are important factors to determine the size of the switches. On the other hand, it is beneficial to choose the size of $M_{S1}$ and $M_{S2}$ roughly large to have small resistance values and hence to maximize the voltage swing at nodes $V_{o1}$ and $V_{o2}$. The ($W/L$) ratios used for the devices in the buffers were obtained following the exponential-horn design guideline, these were $(19.8/0.6)$, $(53.4/0.6)$, $(144.0/0.6)$ and $(388.8/0.6)$ for the transistors $M_{PB4.5}$, $M_{PB3.6}$, $M_{PB2.7}$ and $M_{PB1.8}$, respectively; whereas the ratios for the transistors $M_{NB4.5}$, $M_{NB3.6}$, $M_{NB2.7}$ and $M_{NB1.8}$ were $(6.6/0.6)$, $(18/0.6)$, $(48.6/0.6)$ and $(131.4/0.6)$, respectively. For the case of the switches in the mixer, the ratios occupied were $(180/0.6)$ for transistors $M_{P1,2}$ and $(540/0.6)$ for transistors $M_{N1,2}$. Finally, the ratio of transistors $M_{S1,2}$ was $(480/0.6)$.

In our experimental setup, the BBs and the LO voltages were generated off-chip. Since the BBs are at much lower frequency compared to the LO, it was easier to achieve sufficient phase accuracy between the differential waveforms and no tuning was required on our BB signal-generation board. Another important design consideration were the DC voltages occupied, $V_b$ and $V_{dd}$, which were chosen as low as possible, but still large enough to keep transistors $M_{B1}$ and $M_{B2}$ in strong inversion and in the Ohmic region for the full signal swing of the BBs. This avoids the distortion introduced by the devices if they were biased in saturation and improves the headroom at the output of the UCM.

4. Experimental results

Following all the considerations described in the previous section, a prototype of the power upconverter was implemented in a double poly, three metal layers, 0.5 $\mu$m CMOS technology from MOSIS foundry, aiming at very low cost medical implants supported by the MICS. The prototype area is $1964.5 \mu m \times 686.5 \mu m$. The die photo is shown in Fig. 5.

The die of the prototype was mounted to an evaluation test board, see Fig. 6. Two SMA connectors were used to feed the BB signals and a single SMA connector was used for the LO. Also, an SMA connector was employed to measure the output signal. During evaluation, the LO frequency at which the circuit was tested was chosen at 393.5 MHz with a voltage swing of 1.65 $V_p$ while the BBs were set at 10 MHz ($\sim$40 times smaller than the LO) with an
amplitude of 660mVp (one-fifth of Vdd) and a DC offset ranging from 660 mV to 1.64 V. The DC offset variation from the BB signal was the control voltage which allowed to change the output power.

Fig. 7 shows the measured output spectrum. As anticipated in the analysis, it contains the BB (at 10 MHz), the component of interest (ωLO + ωbb)t (at 403.5 MHz), its image (ωLO − ωbb)t (at 383.5 MHz), and the odd high order IM products. Zooming on the vicinity of the (ωLO ± ωbb)t components, the LO feedthrough component (at 393.5 MHz), appears to be 24 dB under the upper and lower sidebands level. The presence of this small component of the carrier is due to the mismatch between the LO at input of each inverter in the mixer. Therefore, a careful layout of the overall TX must done to keep the LO as balanced as possible at the input of the mixer.

Linearity of the prototype was characterized by means of a two-tone test. Fig. 8 depicts the corresponding plot; an IIP3 of −28 dBm was attained. This makes sense since the IIP3 is compound of both, ΔP and Pin, and ΔP is large in [4].

Fig. 9 shows the plot of the output power is a function of the DC voltage, Vb, when the peak voltage of the BB signal, Vbb, is one-fifth of the maximum supply voltage allowed by the technology, Vdd. It can be seen that as Vb ranges from 1.64 V to 660 mV the output power falls ~5 dB from its maximum value, i.e. for a DC voltage range between 0.5Vdd and 0.2Vdd, the circuit has the ability to decrease, approximately, in a quadratic form the power delivered to the load until one forth of its maximum value. Therefore, by varying the DC component at the BB signal the circuit can modulate its output power. This result is independent of the value of fLO or CL.

Table 2 summarizes the most important features of the prototype. It is important to remark that some of the results achieved by the prototype depend on the parameters of the technology employed, most notably, the power consumption, the frequency range, and active area. In our case, a double poly, three metal layers, 0.5 μm CMOS technology from MOSIS foundry was used. By using deep submicron CMOS technologies, both figures of merit can be reduced, and additionally, incrementing the frequency at which the up converter can work. However, the fLO of the used technology is fast enough to satisfy the RF frequency demand of the MICS, which served as a design example to demonstrate the functionality of the proposed UCM.

Table 3 presents the performance parameters of several published mixers compared with the proposed upconverter. In terms of linearity, our approach exhibits the best fulfillment at the expense of a low conversion factor. Nevertheless, it is important to mention that no de-embedding was applied to the measured data, and hence, losses introduced by the experimental set up are present, which may explain the difference between the measured conversion factor (−55 dB) and the theoretical number (−3 dB). Regarding power consumption, the number is not so good if we look at the ultra low power mixer of [26]. Yet, the UCM design suggested in the current work for the MICS was just a circuit implementation example, and design aspects for dropping the consumption were not made. The pursued goal focused on verifying the functionality of the architecture and not to designing a building block at the cutting edge of the MICS. Certainly, the CMOS process employed is far from the leading deep submicron technologies. Regardless, with a unity-gain frequency, fL, of ~2.4 GHz, this technology is fast enough to satisfy the RF frequency demand of the MICS.
### Table 3
Summary of measurement results and performance comparison.

| Mixer                  | Tech. (µm) | IIP3 (dBm) | CF (dB) | Power C. (mW) | Applic. | \( |f_{Mixer} + f_{Mixer}| (GHz) |
|------------------------|------------|------------|---------|---------------|---------|-------------------|
| gm/lo [21]             | 0.18\(^a\) | 1.5        | +5      | 20            | GSM     | 1.4               |
| S. pumped UCM [22]     | 0.18\(^b\) | 11         | +14.5   | 19.4          | WCDMA   | 2.0               |
| Passive mixer [23]     | 0.25\(^c\) | 20         | -2.9    | NA            | UMTS    | 1.92–1.98         |
| PA driver [24]         | 0.18\(^b\) | NA         | NA      | 19.1          | NPS\(^e\) | 3.06              |
| S. pumped UCM [25]     | 0.18\(^b\) | NA         | 0       | 3             | NPS\(^e\) | 60                |
| Ultra low-power [26]   | 0.18\(^b\) | -6.08      | 21.6    | 1.83          | MICS    | 0.402–0.406       |
| Current driven [27]    | 0.065\(^d\)| 0.25       | -10.7   | 36            | NPS\(^e\) | 2                 |
| Low-noise mixer [28]   | 0.18\(^b\) | 10.5       | 4       | 18            | NPS\(^e\) | 0.9               |
| ECG TXR [29]           | 0.18\(^b\) | NA         | NA      | 8.88\(^d\)    | ZiqBee  | 2.4               |
| Single sideband [30]   | 0.25\(^b\) | NA\(^c\)   | NA      | 204           | NPS\(^e\) | 8–10              |
| Low-power mixer [31]   | 0.09\(^b\) | -2.15      | 2.15    | 8.83          | NPS\(^e\) | 57.1–62.1         |
| This work              | 0.5\(^c\) | 28         | -5      | 23.1          | MICS    | 0.402–0.406       |

\(^a\) CMOS.  
\(^b\) SiGe BiCMOS.  
\(^c\) Sideband suppression \(-45\) dB.  
\(^d\) Complete transceiver.  
\(^e\) NPS = no particular standard.

## 5. Conclusion

The synthesis, design and implementation of a CMOS upconversion mixer capable to adjust, by means of a DC voltage control, its output power as well as canceling the carrier feedthrough in its output port, have been presented. Aiming at low cost applications in the ISM band, a prototype of the architecture was implemented in a double poly, three metal layers, 0.5 µm CMOS technology as a design example. The results obtained in the characterization of the prototype show that, the odd upper and lower sidebands, i.e. \((2n+1)\)oLO ± \(2n\)dB, with \(n = 0, 1, 2, \ldots\) are present in the spectrum of the output waveform. LO feedthrough is mainly due to circuit unbalances. For the current design, LO feedthrough is \(-24\) dB.

The circuit’s IIP3 is \(-28\) dBm was attained, which is state of the art number. Furthermore, for a DC voltage range between 0.5VLO and 0.2VLLO, the circuit can decrease, approximately, in a quadratic form the power delivered to the load until one forth of its maximum value, which can be used to modulate its output power. The output power of the prototype was tunable between \(-12.5\) dBm and \(-18\) dBm.

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