A NOVEL ULTRA-LOW POWER RESET/READ-OUT TECHNIQUE FOR MEGAPIXELS CURRENT-MODE CMOS IMAGERS

Farid Boussaid*, Amine Bermak† and Abdesselam Bouzerdoum*

*Edith Cowan University, School of Engineering and Mathematics, Perth, 6027, WA, Australia
†The Hong Kong University of Science and Technology, Electrical and Electronic Engineering Department, Kowloon, Hong Kong
f.boussaid@ecu.edu.au

ABSTRACT

A novel reset/read-out technique is presented for current-mode ultra-low power Megapixels CMOS imagers. In the proposed technique, the reset and read-out phases occur simultaneously: as a single pixel is being read-out another pixel is being reset. Such a strategy is shown to result in a significant reduction in power consumption. Furthermore, power consumption becomes independent of both read-out speed and imager array size, while still allowing for on-read-out FPN correction along with external electronic shutter control. Its potential integration into CMOS imagers, is demonstrated through the full custom design of a programmable 32×32 current-mode CMOS imager in AMIS CMOS 0.35µm technology.

1. INTRODUCTION

The unique concept of CMOS imagers, i.e., camera-on-a-chip imaging systems, offers the opportunity to integrate photonic array and signal processing circuitry on a single chip, enabling the development of a new generation of smart mobile imaging systems [1][2]. The use of currents as output signals, (i.e. current-mode imagers) greatly simplifies on-chip signal processing integration [2][3]. For instance, summation and subtraction can easily be achieved by simple wire connections. Other potential advantages of current-mode CMOS imagers include increased dynamic range, silicon area savings, operation at high read-out speed and low supply voltages as well as relative insensitivity to the fluctuation of the latter [2][3]. A major obstacle to the development of current-mode CMOS imagers is their typically large fixed pattern noise (FPN). Most proposed FPN correction circuits do compensate for part of the FPN but this comes at the expense of an increased operation complexity with fewer control signals [2].

An excellent trade-off between FPN correction and operation complexity can be found in the current-mode integrating pixel proposed by McIlrath [5]. With only two control signals for reset and read-out, this pixel can achieve on-read-out FPN correction and can compensate for variations in threshold voltages [5]. However, it results in a substantial increase in power consumption, constituting a major obstacle to the development of high performance Megapixels imagers [5]. To alleviate this obstacle, we propose in this paper a novel reset/read-out strategy to achieve ultra-low power consumption regardless of the size of the imager array or the read-out speed. The proposed strategy does not require any additional control signals, keeping the imager operation simple. Moreover, only a single address decoder is required to achieve ultra-low power operation, resulting in a marginal increase in silicon area.

In the next section, the architecture and operation of a conventional current-mode integrating pixel, are reviewed and analyzed. Section 3 presents the proposed novel ultra-low power reset/read-out strategy for this pixel. Section 4 describes its VLSI implementation through the full custom design of a 0.35µm CMOS imager prototype. Finally, concluding remarks are given in Section 5.

2. CURRENT-MODE INTEGRATING PIXEL

A current–mode integrating pixel (Fig. 1) is simply a dynamic current mirror (M1, M2) in series with a select switch M3 [5]. It is a current-reset, current output pixel. The select transistor M3 is enabled for both reset and read-out operations.

During reset, transistors M1, M3 and Mn are turned on so that a known reference current Iref can flow through the diode-connected active transistor M2 and set its gate voltage to the value necessary to sink the reference current.
Using equations (2) and (4) yields

\[ t_2 = t_1 + T \]

where \( T \) is the clock period.

After an integration time \( T_{int} \), the output current decreases almost quadratically with the voltage \( V \), which is a function of the photocurrent \( I_{ph} \) and the selected integration time \( T_{int} \)

\[ V_{ref} = \sqrt{\frac{2I_{ref}}{\beta}} + V_{a2} \]  

\( V_{ref} \) will be the voltage stored on the active gate capacitance at the start of the integration, i.e. when reset transistor M1 is turned off. As incident photons are sensed, generated electron-hole pairs are collected decreasing the voltage at the sensing node by \( \Delta V \), which is a function of the photocurrent \( I_{ph} \) and the selected integration time \( T_{int} \)

\[ V_{gs2} = V_{ref} - \Delta V \]

After an integration time \( T_{int} \), non-destructive read-out can be achieved by closing switch M3 to connect the selected pixel to its column bus. Two read-out modes are then possible with the column reference current source enabled (difference mode) or disabled (direct mode). In the latter mode, the current sunk from the column bus is

\[ I_{dc} = \frac{1}{2} \beta (V_{ref} - \Delta V - V_{a2})^2 \]  

In difference mode, the column current source is enabled so that the current \( I_{diff} \) flowing out from the column bus is

\[ I_{diff} = I_{ref} - I_{dc} \]

Using equations (2) and (4) yields

\[ I_{diff} = \sqrt{2I_{ref}}\beta\Delta V - \frac{1}{2} \beta\Delta V^2 \]  

This result shows that, in difference mode, the output current decreases almost quadratically with the voltage drop \( \Delta V \) at the sensing node. It can also be seen that in difference mode the output current \( I_{diff} \) is independent, to the first order, of the threshold voltage of the active transistor M2 [5]. As a result, difference mode is the preferred operation mode as it compensates for variations in active transistor threshold voltage. Fixed pattern noise (FPN) correction is achieved on read-out. However, this comes at the expense of higher power consumption since a current source is required for each pixel to be reset and each pixel to be read-out [5]. Because of the single reference current source available per column, it follows that, at any given time, only a single pixel can be selected per column whether for reset or read-out. Thus, neither all array pixels can be reset in one operation nor can two different rows be selected simultaneously for two different operations, i.e. reset and read-out.

To address the problem, McIlrath et al proposed to toggle the row address between the row to be reset and the row to be read-out [5]. This strategy is illustrated in Fig. 2, where an array of six columns and three rows R1–R3 is considered; \( t_1 \) corresponds to a time reference and \( t_2 \) is \( t_1 + T \), where \( T \) is the clock period. \( Cs \) represents the column current source array while NOP stands for no operation. During Phase 1, reset is carried out in one operation for an entire row (R2 in Fig. 2a), enabling the entire current source array \( Cs \) during that phase. Subsequently, individual pixel read-out is achieved for an entire row (R1 in Fig. 2a) during phase 2. Note that in the conventional reset/read-out strategy, the entire current source array (Fig. 2a) is enabled for both the reset and read-out phases, resulting in high power consumption if the imager is to be operated in the difference mode, the only mode for which FPN correction can be carried-out.

![Fig. 2. Reset/read-out strategy for: a) conventional approach [5] and b) proposed approach.](image)

3. A NOVEL RESET/READ-OUT STRATEGY

In the conventional reset/read-out strategy, power consumption is directly proportional to the pixel array size as the entire current source array \( Cs \) is enabled during read-out as well as reset [5]. This constitutes a major obstacle to the fabrication of low power high performance Megapixels current-mode CMOS imagers. Note also that the reset of an entire row is achieved in one clock cycle, while read-out requires \( c \) clock cycles, where \( c \) is the number of columns. The result is that integration time, i.e. time between pixel reset and pixel read-out, will not be the same for all pixels of the read-out row. Fig. 2b illustrates a novel reset/read-out strategy that alleviates all of the above limitations.

In the proposed approach, reset and read-out phases occur simultaneously: a single pixel is being reset while a selected pixel is being read-out. As both reset and read-out phases require the use of the single available column current source, pixels selected for reset and read-out do not belong to the same column (Fig. 2b). Only two current sources are enabled at any given time, making power consumption independent of the size of the imager array or the read-out speed. In the described approach, the integration time will be a function of the relative position of the read-out and reset pixels. In Fig. 2b, the reset and read-out pixels are seen to be located on adjacent columns and adjacent rows. The integration time \( T_r \), i.e. the time separating pixel reset from pixel read-out, is the time required to read-out all pixels in a row but one (Fig. 2b). It can be made larger if the selected reset and read-out pixels do not belong to adjacent rows.
The imager operation is summarized in Fig. 4, where only one extra transistor, pixel (M4, M5) replaces the selection transistor. In the new pixel (inset), the parallel combination allowing for simultaneous reset and read-out operations.

seen in, the imager uses a new pixel architecture photodiode chosen for its high quantum efficiency. As register. The photo-sensing element is an Ndiff/Psub array, column/row counter-address decoders, a 5-bit adder Modulo 32, a reset address decoder and a 5-bit register. The proposed technique not only allows for low power operation but also for external electronic shutter control (more in next section).

4. VLSI IMPLEMENTATION

A 32×32 CMOS imager, integrating the proposed ultra-low power operating technique, was designed in AMIS CMOS 0.35μm technology. Its architecture, given in Fig. 3, comprises a 32×32 pixel array, a 1×32 current source array, column/row counter-address decoders, a 5-bit adder Modulo 32, a reset address decoder and a 5-bit register. The photo-sensing element is an Ndiff/Psub photodiode chosen for its high quantum efficiency. As seen in Fig. 3, the imager uses a new pixel architecture allowing for simultaneous reset and read-out operations. In the new pixel (inset Fig. 3), the parallel combination of transistors (M4, M5) replaces the selection transistor M3 of the conventional current-mode integrating pixel architecture (Fig. 1). With only one extra transistor, pixel fill-factor remains high.

The imager operation is summarized in Fig. 4, where \( P_{ij} \) refers to a pixel located on row \( i \) and column \( j \) of the photosensitive array; \( I_j \) is the current source associated with a column bus \( Col_j \). \( S_i \) and \( I_j \) correspond respectively to the column selection signal and current source associated to column bus \( Col_j \). At any given time, only two pixels are selected: one for reset and the other for read-out. The two pixels are always chosen to belong to adjacent columns. This is achieved by

- Enabling a given current source \( I_j \) if its column \( Col_j \) is selected for read-out (\( S_{ij} = 1 \)) OR if it is selected for reset, i.e. next column selected for read-out (\( S_{ij+1} = 1 \)). The logical function (\( S_i \) OR \( S_{ij+1} \)) is implemented by simply introducing a 2-input OR gate in each column, as seen in Fig. 3.
- Resetting a given pixel \( P_{ij} \) if its row is selected for reset (\( Ri = 1 \)) AND if its next adjacent column \( Col_{ij+1} \) is selected (\( S_{ij+1} = 1 \)) for read-out. The logical function (\( Ri \) AND \( S_{ij+1} \)) is implemented, at the pixel level, via transistors in series M1 and M5, as seen in Fig. 3.
- Reading-out a given pixel \( P_{ij} \) if its column and row are selected. The logical function (\( S_i \) AND \( S_{ij} \)) is implemented by 2 switches: transistor M4 at the pixel level and the column switch, as seen in Fig. 3.

Fig. 4 shows that if the register value is \( n \) and pixel \( P_{ij} \) is selected for read-out then pixel \( P_{ij+1} \) is simultaneously selected for reset. The latter is achieved by adding the register value to the row counter outputs. The adder outputs are used by an address decoder to generate the reset signals \( Ri \). In this manner, integration time can be set externally to \( nT_r \), where \( T_r \) is the time required to read-out all pixels in a row but one. The CMOS imager prototype can be operated in two different modes. In Mode 1 (\( SM = 1 \) in Fig. 3), each column bus is connected to a current mirror so that the pixel current signal is buffered before being read-out through voltage \( V_{out} \). In Mode 2 (\( SM = 0 \)), there is no column circuit. Column
buses are simply connected to the output bus through a set of column switches.

Fig. 4. Reset/Read-out sequence implemented in the imager prototype.

A tunable active current mirror [6] is used to clamp the output node voltage so that the pixel current signal can be readout with acceptable delay through voltage $V_{out2}$ (Fig. 3). Because of the typically large output bus parasitic capacitance, the operation in Mode 2 will be restricted to high scene illumination levels with output current level control achieved by choosing $V_{G1} \neq V_{G2}$ [6]. On the other hand, operation in Mode 1 targets lower scene illumination levels. However, the latter does introduce additional column fixed pattern noise (FPN) because of the presence of a column current mirror. In Mode 2 (SM=0 in Fig. 3), there is no column circuit which significantly limit column FPN.

With this novel reset/read-out strategy, power consumption becomes independent of the size of the imager array size or read-out speed as only 2 current sources are enabled at any given time. For Megapixels imagers, power consumption is reduced by over 2 orders of magnitude (Fig. 5) while still allowing for on-read-out FPN correction. The proposed ultra-low power reset/read-out technique targets high performance Megapixels CMOS imagers.

5. SUMMARY

In this paper, an ultra-low power reset/readout technique is proposed for Megapixels current-mode CMOS imagers. The reset and read-out operations are carried out simultaneously such that, at any given time, only two current sources are enabled so that a single pixel is being reset while a selected pixel is being read-out. With this novel approach, FPN correction is achieved on read-out while imager power consumption becomes independent of both pixel array size and read-out speed. For Megapixels imagers, power consumption is reduced by over 2 orders of magnitude. Moreover, the proposed reset/readout technique only requires a single additional address decoder to generate the reset signals while still allowing for external electronic shutter control.

6. ACKNOWLEDGEMENTS

This work was supported in part by a grant from the Australian Research Council.

7. REFERENCES


![Fig. 5. Power reduction in reset/read-out operations as a function of the imager array width.](image-url)