COMPARATOR FOR HIGH SPEED LOW POWER ULTRA WIDEBAND A/D CONVERTER

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ABSTRACT

This paper presents the design and implementation of a high speed low power Complementary Metal Oxide Semiconductor (CMOS) Comparator as part of an ultra fast reconfigurable Flash Analog to Digital Converter (ADC) for a Direct Sequence – Spread Spectrum (DS-SS) based Ultra Wide Band (UWB) Radio receiver. The comparator was implemented in 180 nanometre CMOS Technology. The switching speed of the comparator is 2 Giga Samples per second for a 1GHz input bandwidth. The comparator operates on a 1.8V power supply. The total input referred offset of the comparator (@1 GHz) is 37.5 mV which is less than 0.6 LSB for a 4 bit flash converter. No offset averaging techniques have been used to minimise the comparator offsets. The comparator has a low gain and low swing which is crucial for its high speed and low power operation.

KEYWORDS

Comparator, UWB, ADC, DS-CDMA, CMOS

1.0 INTRODUCTION

Ultra Wideband as a means of communication has been around for decades. It has enormous potential for very high speed and low power communications. The deregulation of the 3.1 to 10.6 GHz spectrum by the Federal Communications Commission (FCC) and subsequently other countries has given a major boost to its potential use in commercial applications [1, 2]. The FCC order and report defines a typical UWB signal as that which has a fractional bandwidth of $B/f_c \geq 20\%$ (where B is the transmitting bandwidth and f_c the centre frequency) or an absolute bandwidth greater than 500 MHz. Moreover the UWB signalling scheme has to correspond to a transmitting power ceiling as mentioned and depicted in [1]. The scheme highlights a typical bandwidth of 7.5 GHz for a UWB system meaning that data rates of the order of Gigabits per second are possible. The attractiveness of UWB is further enhanced by its ability to have low complexity and low cost systems, resistance to multi-path fading and jamming and low energy density. UWB technology is based on transmission and reception of sub-nanosecond pulses, such that the overall signal is spread over a very large frequency range [3].

The paper is broken down into the following sections. Section 2.0 describes UWB receiver architecture, along with the type of ADC and corresponding specifications. Section 3.0 details out the comparator design and Section 4.0 discusses the results of the implementation.

2.0 ULTRAWIDEBAND RECEIVER

As UWB systems operate over a large frequency range covering other narrow band technologies, the overall transmitting and receiving power is very low. This is a precaution so that a UWB system does not interfere with other narrowband radio systems. Therefore as discussed in [4] this requires the use of finite spread spectrum technologies. The different spread spectrum methods like the time hopping and direct sequence have been looked into for UWB systems in [4]. This paper focuses on direct sequence spread spectrum transceiver architecture for a UWB system.

An ideal direct sequence UWB receiver architecture is shown in Figure 1.0

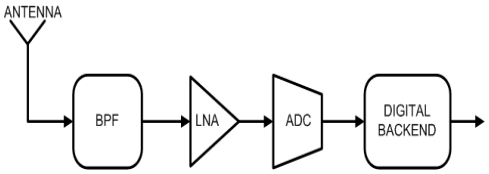

Figure 1.0 Ideal Digital Receiver

It consists of a Band Pass Filter (BPF), Low Noise Amplifier (LNA), Analog to Digital Converter and the Digital Backend. This architecture enables moving the ADC almost up to the receiving antenna thereby reducing the overall complexity of the system, lowering power consumption and allowing the digital backend to deal with most of the signal processing work.

The ability of this receiver is underscored by the capability of the ADC to sample and quantise very high frequency signals which requires a sampling rate (based on Nyquist Criterion) of several Giga Samples per second. The UWB methodology emphasises a low power and low complexity solution however the inherent ADC creates a bottleneck to this realisation. This can be demonstrated by a simple analysis based on

power, speed and resolution. Considering that a signal of 5 GHz needs to be sampled and quantised, the system requires an ADC which operates at 10 Giga-Samples per second. The fastest converter to date is the flash topology and is the pre-eminent choice for UWB receivers [5]. The power consumption of a flash converter is determined by the number of comparators used, typically 2^N -1, where N is the resolution or number of bits. A typical formula for the total power consumed by the comparator (neglecting comparison clock period) is shown in equation (1)

$$P_T = 2^{N-2} \cdot (f_{CLK} \cdot V_{REF} \cdot C_S + V_{DC} \cdot I_{DC}) \ldots (1)$$

where N = resolution of ADC or number or bits,
f_{CLK} = Comparator sampling/clocking frequency,
V_{REF} = ADC reference voltage,
C_S = Comparator Switched Capacitance,
V_{DC} = DC Supply Voltage,
I_{DC} = DC Current from V_{DC}

A simplistic estimation leads to a power consumption of hundreds of milliwatts to a few watts, depending on the resolution. The requisite of the UWB - ADC is further increased by its need to resolve signals less than 0.5 LSB, which becomes harder with increased resolutions. Also for an ADC to sample at a rate of 10 GHz requires a comparator to have a clocking frequency of the same order, which results in a preamplifier having a Gain Bandwidth of 220 GHz. Such a design is out of the purview of current sub-micron CMOS technologies.

An alternative to a fully digital design as depicted in Figure 1.0 is to employ a down-conversion mechanism before the ADC so as to relax the requirements on the ADC. This type of receiver architecture is shown in Figure 2.0.

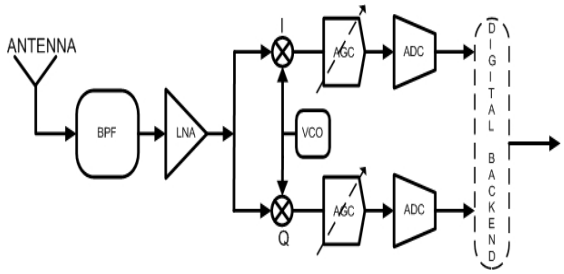

Figure 2.0 Down-Converted UWB Receiver

A signal having a bandwidth of 1 GHz is input into the receiver, which lies in the low band of a DS-UWB scheme, ranging from 3.1 to 5 GHz. The signal is then down-converted by a combination of a Voltage Controlled Oscillator (VCO) and MIXER (I and Q), resulting in a 0 to 1 GHz bandwidth signal at the input of the ADC.

This therefore requires the ADC to operate at a minimum sampling rate of 2 GHz. Therefore, requirement of an ADC to sample a signal at 2 Giga Samples per second is much more relaxed than having to sample a signal at 10 Giga Samples per second, and is in the purview of existing sub-micron CMOS technologies [6-7].

The idea of sampling a signal at high sampling rates brings into focus the type of ADC architectures that can be used. The obvious choice is of course the Flash architecture. A typical flash ADC has 2^N -1 comparators and outputs N logic levels per sample [8-10].

The parallel nature of this ADC architecture enables the prospect of sampling a signal at Giga Samples per second. The number of bits to be output by a Flash architecture depends on the requirement for an UWB ADC. An estimation based on [11] allows us to calculate for a typical UWB receiver architecture, the number of bits required. It was determined that for a signal bandwidth of 1 GHz, a sampling rate of 2 Giga-samples per second was more that sufficient along with a maximum of 4 bit sampling resolution. The heart of a Flash design is the inherent comparator. For a UWB ADC the comparator performance limits the performance of the entire ADC. Therefore this design is required to have a comparator with a switching time of not greater than 500 picoseconds. The comparator also needs to resolve voltages in millivolts. The following section details out the design of the comparator for use in an UWB ADC.

3.0 COMPARATOR

As mentioned before the comparator is the heart of the ADC. The comparator in this design consists of 4 stages comprising of an Input Preamplifier and 3 successive latching stages as shown in Figure 3.0.

3.1 PREAMPLIFIER STAGE

The input preamplifier is shown in Figure 4.0. The preamplifier is designed as a low voltage low gain fully differential amplifier. The idea of using differential signalling is to reduce supply noise and also to provide sufficient immunity from feedback noise. The preamplifier was sized so as to meet the speed and gain bandwidth requirements for the ADC. The lengths of the input transistors were kept at minimum so as to obtain the required speed. The widths of the input transistors of the preamplifier were sized so as to obtain a good gain bandwidth product. The sizing of the widths however has significant influence on the input offset of the preamplifier. The input referred offset for the preamplifier is given in equation (2);

$$V_{os} = \left[\frac{\Delta L_{N-i}}{L_{N-i}} + \ldots + \frac{\Delta L_i}{L_i} + \frac{\Delta W_{N-i}}{LW_i} + \ldots + \frac{\Delta W_i}{W_i} \right] + V_T \quad \ldots. \quad (2)$$

where V_{OS} = Input referred offset, V_T = NMOS input pair threshold voltage, W = Transistor widths, L = Transistor length.

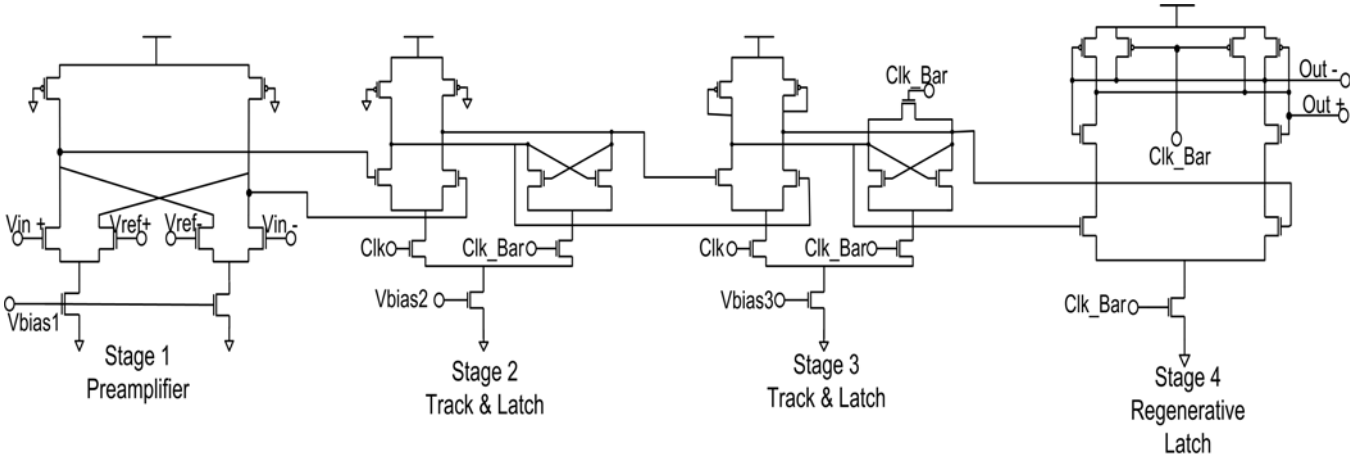

Figure 3.0 Circuit Diagram of High Speed Comparator

The preamplifier is loaded with MOSFET only loads. The type of MOSFET load was chosen to satisfy the common-mode, output swing and input bandwidth. The Triode-connected load was chosen because the variations in common-mode are not large enough to affect the output of the preamplifier and can be tolerated. The preamplifier was biased to get a very low swing of about 0.2V. Consequently the triode loads were sized accordingly so as to have enough mismatch tolerance and good overdrive recovery. The overdrive recovery was chosen as V_{dd} - V_T for the PMOS transistors and is sufficient for the grounded-gate transistors. Upon simulations it was seen that the contribution of these loads to input referred offset was very small considering that the input transistors have a sufficiently large transconductance (g_m) so as to isolate the output nodes effectively. The preamplifier design is different to that shown in [12] because a resistor load would require larger headroom and consume more area than a typical MOS transistor. Also unlike [12] the preamplifier uses no reset switch as it has enough overdrive voltage from the previous stage.

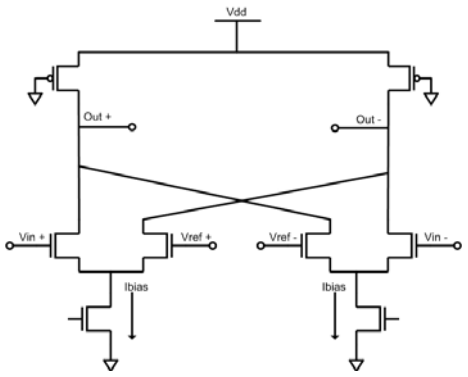

Figure 4.0 Input Preamplifier

3.2 LATCHING STAGE

The subsequent 3 stages of the comparator are all latched comparator stages. It consists of 2 classic track and latch stages and a regenerative latch.

Figure 5.0 shows a simple track and latch comparator stage. This type of latched comparator was used due to its considerations for speed and performance [13, 14]. The comparator operates based on a clocking scheme and has limited bias. It consists of an input differential amplifier which turns on and tracks the input when the clock is high and a latching stage that turns on, providing slight amplification and executes positive feedback when the clock (CLK) is low. The offset of this stage is dependent on both the input amplifiers and the latching stage.

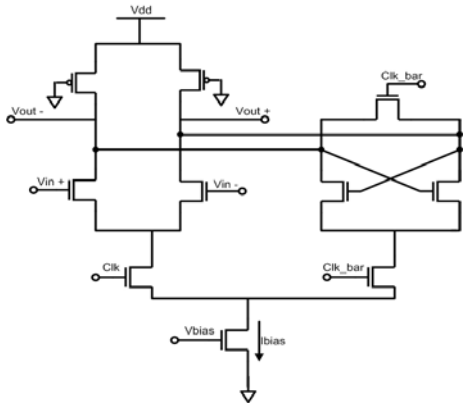

Figure 5.0 Track and Latch

The comparator uses a triode load with a clocked reset switch in the latching stage to override any large previous decisions. The speed advantage of this comparator comes from its low swing and high tolerance to meta-stability error. The bias current and the triode loads determine the output swing, with reduced swing requiring lesser charging and discharging time. The common-mode level for the output has been set to half the supply, thereby allowing faster settling time. The main comparator uses two stages of this form of track and latch pair so as to provide the requisite gain. The second latching stage is different to the first latch in that the load for the latch is a diode based load and not a triode load. This was done so as to get an improved swing of 0.5V in the output such that the final regenerative latch could provide precise output levels.

The final stage of this comparator consists of a regenerative latch (Figure 6.0). The regenerative latch, although not advantageous for speed, however can be used to generate rail to rail logic levels. In this design meta-stability of this latch is not a major problem due to the previous stage providing enough swing. The latch works by enabling the 2 NMOS input transistors N1 & N2 when the Clk_Bar signal goes high. The output is pre-charged to high when Clk_Bar goes low. The feedback mechanism of the latch helps to take the output logic levels to supply and ground, with the help of different charging times for the output transistor capacitances. Due to the very high operating speed of the latch the output has a reduced slew rate as compared to the previous stages to enable a rail to rail transition. The interesting feature of this latch is that since it has no external biasing transistors, unlike the previous two stages, the overall power consumption is reduced [15].

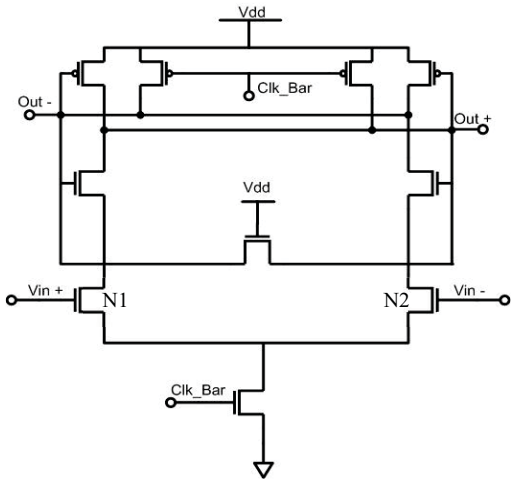

Figure 5.0 Regenerative Latch

4.0 RESULTS

The comparator has been designed and simulated using TSMC 0.18µm CMOS technology. Table 1.0 shows the results of the implemented comparator. The performance of the comparator is in line with the requirements for a Direct Sequence UWB ADC. The total input referred offset of the comparator was estimated using equation (3) [16] and is in line with simulated results as shown in table 1.0.

$$V_{os,\,Total} = V_{os,\,Stage1} + \frac{V_{os,\,Stage2}}{A_1} + \ldots + \frac{V_{os,\,StageN}}{A_1 A_2 \ldots A_N} \qquad \ldots(3)$$

where A = Gain of the succeeding stages

The comparator was tested for the different trip points (Figure 6.0) from 1 LSB to 15 LSB corresponding to a 4 bit Flash ADC. The comparator exhibits good overdrive recovery for a small input of 65mV immediately after 15 LSB. The overall output delay is kept to within 1 clock cycle. The rate of slew for the output is much slower than previous stages due to the final regenerative latch.

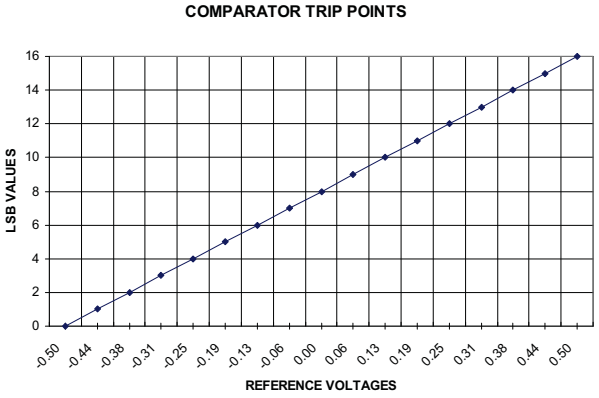

Figure 6.0 Comparator Trip Points

The switching time for the comparator at 15 LSB occurs within one-half of the rise time of the succeeding clock cycle. It is assumed that the digital backend of the receiver will compensate for this delay. The output offset versus the input operating frequency range of the comparator is shown in Figure 7.0. Figure 8.0 shows one iteration of the comparator. No output buffer was used as the required logic levels were obtained. Table 1.0 shows the results for two separate input frequencies.

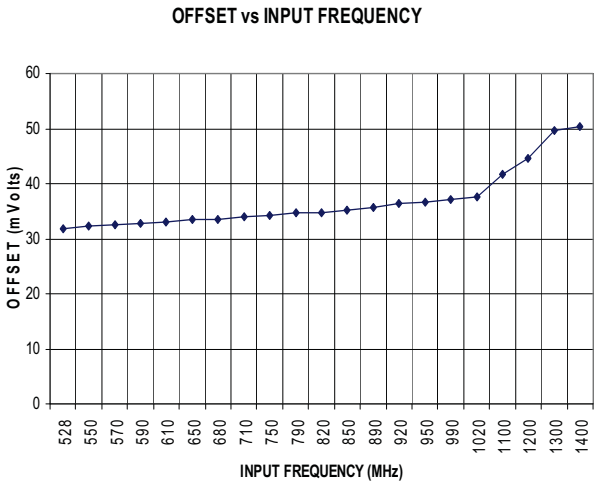

Figure 7.0 Output Offset versus Input Frequency Range

Input Frequency Range	1020 MHz	528 MHz
Maximum Sampling Rate	2 GS/s	2 GS/s
Output Offset	37.5 mV (0.6 LSB)	32.7 mV (0.5 LSB)
Input Range	1 V peak-to-peak	
Reference Voltage	1 V	
Resolution	63 mV	62.4 mV
Power Consumption	2.7 mWatts	1.15 mWatts
Technology	TSMC 0.18µm CMOS	

Table 1.0 Comparator Performance Comparison

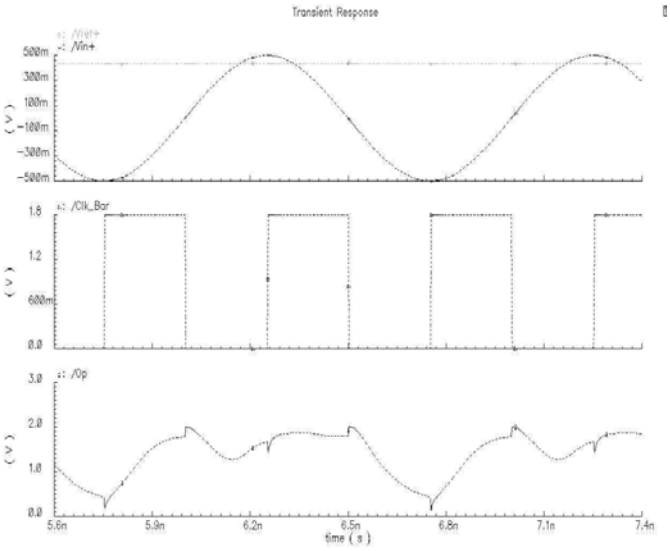

Figure 8.0 Simulation Output

5.0 CONCLUSION

This paper presented a dynamic high speed CMOS comparator for a 4 bit Flash UWB ADC. The comparator exhibits good performance at a sampling rate of 2 Gsps, with accuracy of 0.6 LSB. An optimal balance between technology and architecture was used to obtain the required high speed and low power. The comparator uses no power hungry offset calibration techniques.

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