A Digital Multiplier Architecture using Urdhva Tiryakbhyam Sutra of Vedic Mathematics

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***Abstract*— Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discusses a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly.**

***Index Terms*— Vedic mathematics, Urdhva Tiryakbhyam, binary multiplication, hardware design, array multiplier.**

I. Introduction

VEDIC mathematics [1] is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirtha (1884-1960) after his eight years of research on Vedas [1]. According to his research, Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to a very simple ones [2]. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. This paper discusses a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers [3].

Digital multipliers are indispensable in the hardware implementation of many important functions such as fast Fourier transforms (FFTs) and multiply accumulate (MAC). This has made them the core components of all the digital signal processors (DSPs). Two most common multiplication algorithms followed in the math coprocessor are array multiplication algorithm and booth multiplication algorithm [4]. The array multipliers take less computation time because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array.

Booth multiplication is another important multiplication algorithm [5]. Large Booth arrays having large partial sum and partial carry registers are required for high speed multiplication and exponential operations. Multiplication of two n bit operands using a radix-4 Booth recording multiplier requires approximately $n/(2m)$ clock cycles to generate the least significant half of the final product, where m is the number of Booth recoder adder stages. Thus, a large propagation delay is associated with this case.

This paper presents a simple digital multiplier architecture [3] based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India. In [6], this Sutra is shown to be a much more efficient multiplication algorithm as compared to the conventional counterparts. We apply this Sutra to binary systems to make it useful in digital hardware. In particular, we propose a digital multiplier that calculates the partial products in parallel and hence the computation time involved is less. It should be noted that the architecture of the proposed Vedic multiplier comes out to be very similar to that of the popular array multiplier. Thus, Vedic mathematics provide a much simpler derivation of the array multiplier than the conventional mathematics.

This paper is organized as follows. In Section 2, a brief overview of the Vedic mathematics is provided and the Vedic multiplication algorithm is discussed in detail. Section 3 provides the hardware architecture of the proposed Vedic multiplier. The paper is concluded in Section 4 by summerizing the importance of the Vedic mathematics in the field of engineering.

II. Vedic Multiplication Algorithm

A. The Vedic Sutras

Vedic mathematics is based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic,

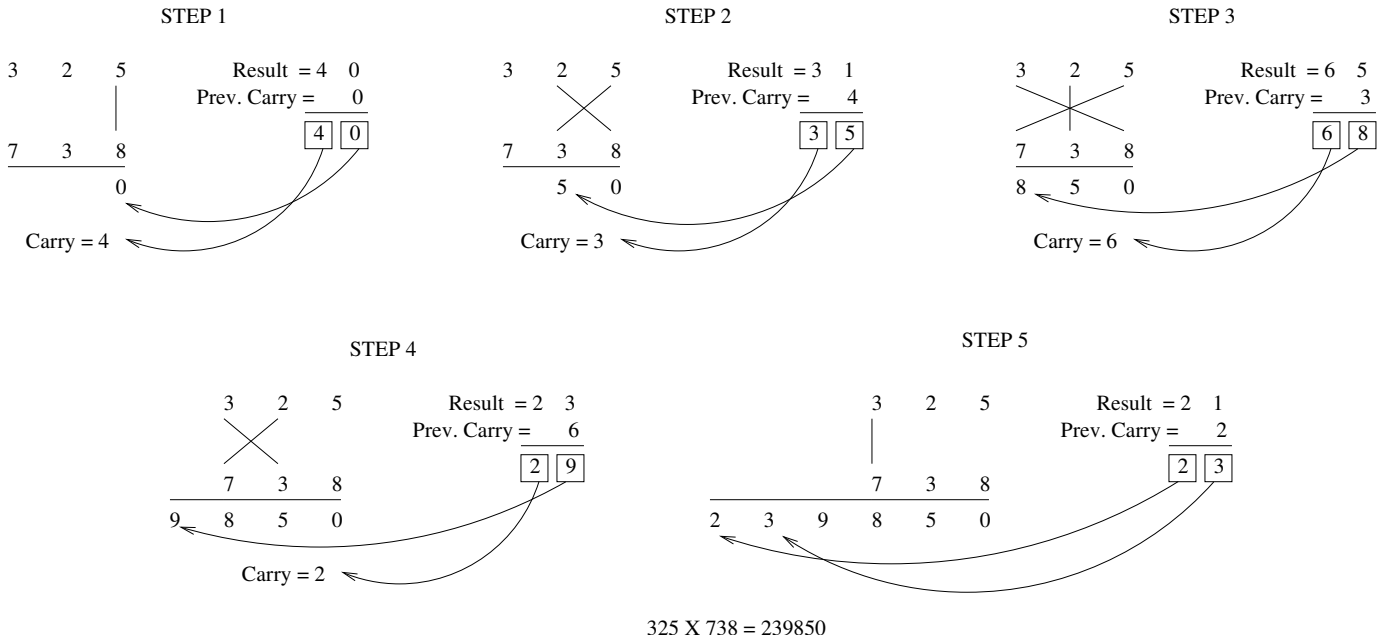

Fig. 1. Multiplication of two decimal numbers by Urdhva Tiryakbhyam Sutra.

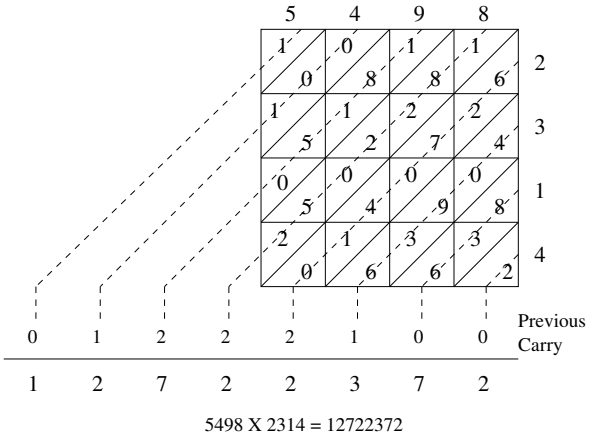

Fig. 2. Alternative way of multiplication by Urdhva Tiryakbhyam Sutra.

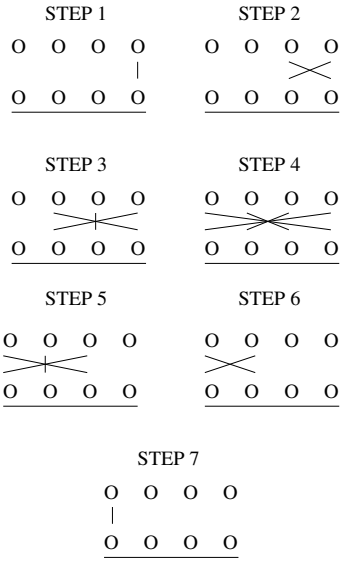

Fig. 3. Line diagram for multiplication of two 4-bit numbers.

algebra, geometry etc. [7]. These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena – By one more than the previous one.
4) Ekanyunena Purvena – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or non-completion.
10) Sankalana-vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-Tiryagbyham – Vertically and crosswise.
15) Vyashtisamanstih – Part and Whole.
16) Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of

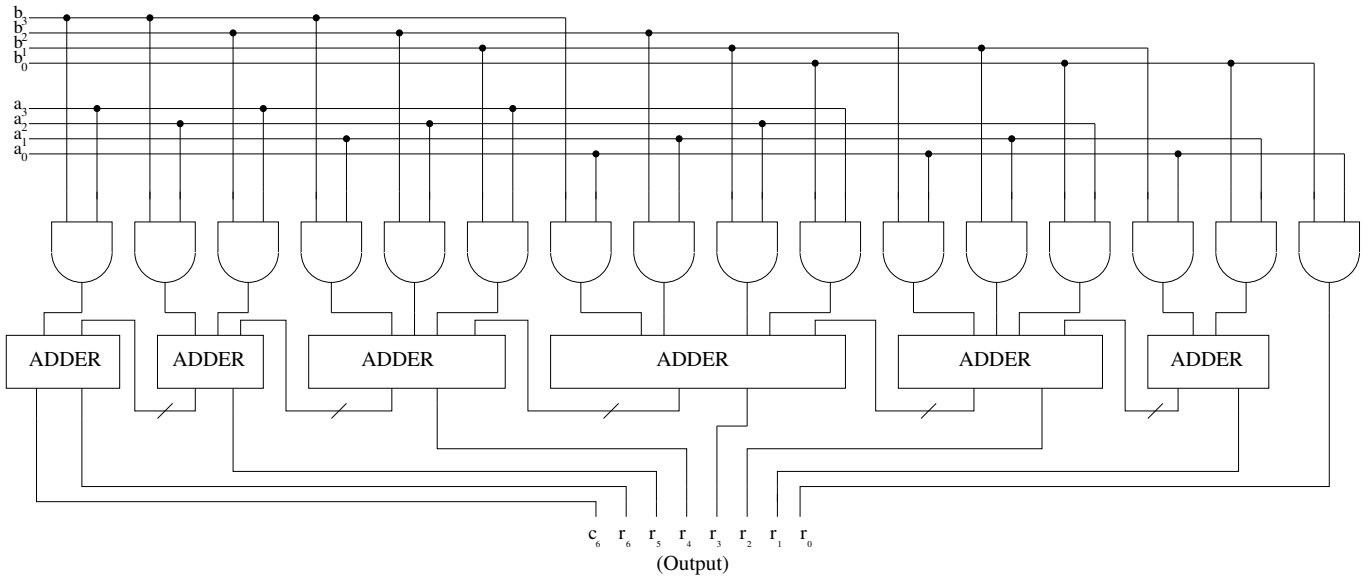

Fig. 4. Hardware Architecture of the proposed Vedic Multiplier.

various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century by Sri Bharati Krsna Tirtha. Many Sub-sutras were also discovered at the same time which are not discussed here.

B. The Proposed Vedic Multiplier

One of the mentioned Sutras in the last subsection, Urdhva Tiryakbhyam (Vertically and Crosswise), deals with the multiplication of numbers. This Sutra has been traditionally used for the multiplication of two numbers in the decimal number system. In this paper, we apply the same idea to the binary number system to make it compatible with the digital hardware. Let us first illustrate this Sutra with the help of an example in which two decimal numbers are multiplied.

Line diagram for the multiplication of two numbers (325×728) is shown in Fig. 1. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be zero.

An alternative method of multiplication using Urdhva-Tiryak Sutra is shown in Fig. 2. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

We now extend this Vedic multiplication algorithm to binary number system with the preliminary knowledge that the multiplication of two bits a_0 and b_0 is just an AND operation and can be implemented using simple AND gate. To illustrate this multiplication scheme in binary number system, let us consider the multiplication of two binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. As the result of this multiplication would be more than 4 bits, we express it as $...r_3r_2r_1r_0$. Line diagram for multiplication of two 4-bit numbers is shown in Fig. 3 which is nothing but the mapping of the Fig. 1 in binary system. For the sake of simplicity, each bit is represented by a circle. Least significant bit r_0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier. The process is followed according to the steps shown in Fig. 3. As in the last case, the digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result (r_n) and a carry (say c_n). This carry is added in the next step and hence the process goes on. If more than one lines are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all the other bits act as carry. For example, if in some intermediate step, we get 110, then 0 will act as result bit and 11 as the carry (refered to as c_n in this text). It should be clearly noted that c_n may be a multi-bit number. Thus we get the following expressions:

$$r_0 = a_0b_0, \quad (1)$$
$$c_1r_1 = a_1b_0 + a_0b_1, \quad (2)$$
$$c_2r_2 = c_1 + a_2b_0 + a_1b_1 + a_0b_2, \quad (3)$$
$$c_3r_3 = c_2 + a_3b_0 + a_2b_1 + a_1b_2 + a_0b_3, \quad (4)$$
$$c_4r_4 = c_3 + a_3b_1 + a_2b_2 + a_1b_3, \quad (5)$$
$$c_5r_5 = c_4 + a_3b_2 + a_2b_3, \quad (6)$$
$$c_6r_6 = c_5 + a_3b_3 \quad (7)$$

with $c_6r_6r_5r_4r_3r_2r_1r_0$ being the final product. Partial products are calculated in parallel and hence the delay involved is just the time it takes for the signal to propagate through the gates.

III. Hardware Architecture

The main advantage of the vedic multiplication algorithm (Urdhva-Tiryak Sutra) stems from the fact that it can be easily realized in hardware. The hardware realization of a 4-bit multiplier using this Sutra is shown in Fig. 4. This hardware design is very similar to that of the famous array multiplier where an array of adders is requited to arrive at the final product. All the partial products are calculated in parallel and the delay associated is mainly the time taken by the carry to propagate through the adders which form the multiplication array.

IV. Conclusion

Ancient Indian system of mathematics, known as Vedic mathematics, can be applied to various branches of engineering to have a deeper insight into the working of various formulae. The algorithms based on conventional mathematics can be simplified and even optimized by the use of Vedic Sutras. We have discussed one such possible application of Vedic mathematics to digital signal processing. A simple Vedic multiplier architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra of Vedic mathematics has been presented. The hardware architecture of the Vedic multiplier is also depicted and is found to be very similar to that of the so called array multiplier. This is just one of the many possible applications of the Vedic Mathematics to Engineering and some serious efforts are required to fully utilize the potential of this interesting field for the advancement of Engineering and Technology.

Although, Vedic mathematics provides many interesting Sutras, but their application to the field of engineering is not yet fully studied. Knowingly or unknowingly we always use Vedic Sutras in everyday world of technology. As an example, whenever we use $i \leftarrow i+1$ or $i \leftarrow i-1$ in software routines, we use 'Ekadhikina Purvena' and 'Ekanyunena Purvena' Sutras respectively. Similarly the Vedic algorithms can be directly applied to solve many problems of trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. Hence, the vast potential of this interesting field should be exploited to solve the real world problems efficiently.

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