Design Methodology for Fault Tolerant ASICs

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Abstract—The sensitivity of application specific integrated circuits (ASICs) to the single event effects (SEE) can induce failures of the systems which are exposed to increased radiation levels in the space and on the ground. This paper presents a design methodology for a full fault tolerant ASIC that is immune to the single event upsets (SEU) in sequential logic, the single event transients (SET) in combinational logic and the single event latchup (SEL). The dual modular redundancy (DMR) and a SEL power-switch (SPS) are the basis for a modified ASIC design flow. Measurement results have proven the correct functionality of DMR and SPS circuits, as well as a high fault tolerance of implemented ASICs along with moderate overhead in respect of power consumption and occupied silicon area.

Keywords- Single event effect, fault tolerance, dual modular redundancy, power switch, ASIC design methodology

I. INTRODUCTION

Malfunctions of electronic devices due to the single event effects, being an effect of radiation, are observed not only in cosmic and airborne equipment, but also in mainstream applications. Together with the progressing integration and scaling of the electronic chips their susceptibility to errors increases. The current space microelectronics development and high energy physics research require shorter design time and cheaper solutions for the radiation and fault tolerant designs. The main idea in this work was how to use known technologies in the radiation environment without losing the functionality of the system based on an ASIC chip and how to provide more reliability with the few more steps in the design process.

As the fault tolerant SRAM based FPGA has become increasingly more common in the space-based computing, the space microelectronics industry and scientific research in the nuclear physics area still need high complexity integrated circuits based on ASIC technology [1]-[3]. There are different design methodologies based on automated mitigation techniques for the protection of digital ASIC in radiation environment [4], [5].

A cosmic particle strike may induce a single event effect (SEE). Three common types of SEE are known: single event upset (SEU), single event transient (SET) and single event latchup (SEL). The single event latchup, compared to SEU and SET, is a potentially destructive state [6]. We can clearly separate the known protection techniques into two categories: design level techniques [7] (hardened-cell design [4], triple modular redundancy (TMR) [8], dual modular redundancy (DMR) [9], and error detection and correction for memories [10]) and layout level techniques [11] (enclosed layout transistor, guard rings and trench isolation). There are also the mitigation techniques based on expensive technology changes [11].

This paper presents a modified design flow for fault tolerant ASIC that is based on reduced redundant circuit architecture. Dual modular redundancy has been chosen instead of triple modular redundancy in order to reduce the required redundant area still keeping the system protected against SEU effects in sequential logic and SET effects in combinational logic. The second important reason for using dual modular redundancy is a simpler system protection against SEL effects. Namely, the DMR architecture needs two SEL power-switch (SPS) cells while TMR deploys three SPS cells. The modified design flow starts with the standard synthesis without any change. An extra step, compared to the standard design flow, is based on a netlist modification and provides a new redundant netlist containing the voters.

The paper is organised in three sections. The first section describes a DMR circuit and a fault injection model. The second section presents a SEL power-switch. The modified ASIC design flow and implemented circuits are described in the third section.

II. REDUNDANT CIRCUIT AND FAULT INJECTION MODEL

Redundancy is always required for any fault tolerant design. If the redundancy level is higher, the higher is generally the protection level but the larger is also the chip area, power consumption, and cost. Therefore we have to trade-off between the redundancy level and the dependability requirements with respect to the intended application. In order to reduce the hardware overflow produced by the TMR approach and to keep the design reliability high, we have used the DMR approach with self-voting. Self-voting is based on a 3-input majority voter that is configured to vote on two external inputs taking into account the state of its own output. Figure 1 shows the aforementioned DMR architecture.

In order to verify our approach on a system level, we have synthesized a DMR 1000-bit shift register including a fault injection model [12]. The fault injection model covers two types of the single event effects: single event upset and single event transient. The mentioned DMR fault injection model is
presented in Figure 2. The SEU fault injection mechanism is based on flipping the saved state in the flip-flop during a clock cycle by using XOR logic. Starting from the nature of the SEU effect, the model of a flip-flop should change the saved value in the chosen moment within the clock cycle. In the new clock cycle, the flip-flop should continue with normal behaviour. The activation of a SEU effect is done by setting the logic high level on the SEU input (Figure 2). From the other side, the SET effect is caused by a short impulse on the output of combinational logic. In case that a combinational output is set to the high logic level, the SET effect provides the inverted value during transient time. A SET fault is possible to inject by using the SET input of the second XOR logic (Figure 2). As the SET period and the moment when SET occurs are not related to the clock, both values are taken from the randomly generated libraries of SET timings.

The analysis of the DMR 1000-bit shift register design simulations for the IHP 250 nm CMOS technology has shown a moderate overhead of power consumption (in total 21.3 mW) and used silicon area (in total 0.451 mm²).

III. SEL POWER-SWITCH

The system protection against the single event latchup effect requires design of a special power-switch cell. The SEL power-switch cells are used together with the latchup sensors and switches of the logic which is affected. The SPS cell is designed, characterised and verified as any other standard cell of the IHP library [13]. The SPS cells are placed exactly under the power-stripes/cell-rows crossover points instead of the filler (empty) cells. The power-stripes and power-rows are connected only through the SPS cells. A SPS cell has one output, the controlled logic is disconnected from the VDD1 power supply line. The latchup sensor is a specially designed transistor for fast reaction in the latchup handling process.

The SPS cells placed on the supply lines of a DMR design are shown in Figure 4. When the latchup occurs on VDD1, Sensor 1 detects much higher current than usual and, at the same time the drain voltage of the S11 switch decreases to the ground level. Therefore, the S11 switch is off and the S12 switch is on. In this period, until the S11 switch is off, the controlled logic is disconnected from the VDD1 power supply line. The latchup sensor is a specially designed transistor for fast reaction in the latchup handling process.

Figure 4. SEL power-switch cells in a DMR design

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Figure 5. The parasitic PNPN structure
The logic affected by the latchup should be disconnected from the main supply line for a period of time defined by the control logic (timer) in order to stop the extremely high current through the parasitic PNPN structure that can destroy a CMOS integrated circuit (Figure 5). The redundant circuits are connected to the separated power supply lines or power domains. As shown in Figure 4, the SPS cells work in such a way that the SPS cell connected to one power domain (VDD1) always controls the other power domain (VDD2). This scheme provides for the SPS cell self-protection from the latchup. The SPS control logic needs to have a continuous and independent power supply in order to control the power supply lines of the logic suffering the latchup conditions. SPS must quickly react and simply disconnect the harmed part of the system.

A simplified SPS cell schematic is presented in Figure 6. Timing measurements are done in order to characterise and use the SPS cell in an automated design flow. The measurements are carried out by using a special latchup generator. It is important to note that in case of permanent short circuit on the Vdd1 output pin, the SPS cell will automatically be in the protection mode. It is also possible to control the activity of the SPS cell by the Poff pin.

Maximal current tests are based on the longer shortcut time and measurements when the output transistor of the power-switch cell is destroyed. The burn off test (the shortcut between the drain of driving transistor and the ground) for the output PMOS transistor (T5) is performed to prove its resistivity to the high latchup current. Figure 7 presents the simulation results of the drain voltage and drain current for the T5 transistor in the moment of latchup occurrence.

The latchup ramp voltage controls an input of the switch used for the simulation purposes. The switch changes the resistance on its outputs depending on the voltage level applied on the control input. The outputs of the voltage controlled switch are connected between the drain of the T5 transistor (Vdd1 in Figure 6) and the ground. The response time of the SPS cell is visible in Figure 7.

The simulated worst-case power consumption of the SPS cell is 750 μW in normal conditions and 3.16 mW in latchup mode. However, the measured power consumption is about 500 μW in normal conditions and goes up to 1.25 mW when the stimulated latchup occurs. The difference between power consumptions in normal and latchup modes is due to the pull-down resistor presented in Figure 6.

IV. MODIFIED ASIC DESIGN FLOW

The work described in this paper is based on use of the standard design tools and an enhancement of the standard ASIC design flow in order to provide the higher reliability of digital ASICs. The major advantage of a novel design strategy is fast and easy design of a radiation-tolerant (SEU, SET and SEL immune) ASIC. An extra step compared to the standard design flow is necessary to provide a new redundant netlist including the self-voters.

Duplication of the generated netlist is performed by the parser script, which can be later included in the synthesis script as an optional subprogram for generating the redundant netlist. Parsing is done by the Flex-Bison tool [14]. The script for the netlist modification provides the following:

a) The names of instances in the netlist are unique. As the complete system is supplied by two separate power domains, the names have marks to indicate which power supply domain is used for the given cell.

b) Flip-flops as standard storage elements are replaced by the modified DMR fault tolerant (DMRFT) storage elements.

c) The voter has two inputs connected with both redundant flip-flops and a third input connected to the own output as presented in Figure 2.

d) Memories must be generated with the extra protection bits (parity, Hamming code, etc.) and also attached to the EDAC logic to handle SEUs.

For the SEL protection, memories and EDACs are duplicated [15]. The design simulation after synthesis is done using the same test bench (written to test the original non-redundant design). This step is capable of testing only the SEU and SET (but not SEL) protection of the appropriate fault injection modelled combinational and sequential logic. As the SPS cell is a mixed-signal circuit, the SEL simulations need the analogue simulators. As known, after the DRC and LVS checks, simulation can take a lot of time and, therefore, we use the SEL power-switch cell as a standard library cell.

In the layout process it is important that the standard cell power supply lines (depending on the technology – in our case “Metal 1”) of the two power supply domains are placed in alternated order. This is a very important step as preparation for the DMR placement. A simple modification of the technology file provides the required redefinition of the power domains. When the power planning is finished, the designer
performs the placement of SEL power-switch (SPS) cells. The SPS cells are placed under the crossover points of the power stripes and power rows (power rows - power supply lines for standard cells). In the global connection process, a SPS cell is connected to the specified power domain. The redundant logic 1 is connected to the power supply 1 and the redundant logic 2 to the power supply 2. SPS cells need not to be placed under each and every crossover point. The designer should calculate the maximal current for given control section and compare with the SPS maximal output current. After the SPS cells are placed and connected with the specified power domains, the design flow continues with the standard steps: standard cell placement, clock tree synthesis (CTS) and routing with all required timing optimizations. The designer needs to prepare all the technology files necessary for the DRC and LVS checks.

In order to prove the SEL protection, we have designed a small test circuit which consists of the SPS cell and DMR circuit (Figure 8). Figure 9 presents a layout of the mentioned circuit.

V. CONCLUSION

The standard design flow has been modified to provide the protection of digital ASIC against the known single event effects occurring in radiation environment. The results, based on the 1000-bit shift register simulations and measurements, have shown that use of the DMR with self-voting reduces the power consumption and silicon area overheads. The analysis has also shown an appropriate trade-off between the required reliability and the physical chip characteristics. The tests of the SPS cell integrated with a simple DMR circuit have proved the correct circuit behaviour in the presence of latchup effect, what justifies the use of the proposed modifications in the fault tolerant ASIC design flow.

During the tests, we have noticed a problem based on the transient effect in the voter logic near the active clock edge of the next flip-flop. The proposed DMR circuit cannot repair the error if a transient pulse changes the flip-flop input value during the active clock edge. In this case, both flip-flop outputs switch to the wrong state. Our future work will be focused on the DMR circuit modifications targeted to handle the described effect correctly.

Further development of the redundant netlist generators and automated placement of the SPS cells in the layout phase is foreseen. Testing of more complex test structures and other technologies (IHP25RH and IHP13) is planned for near future.

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