A 0.7-V 100-µW Audio Delta-Sigma Modulator with 92-dB DR in 0.13-µm CMOS

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Abstract- A low-voltage fourth-order audio ∆Σ modulator is designed with a single-loop single-bit feedforward structure. A 2-tap FIR filter is inserted in the feedback loop to effectively attenuate the high frequency quantization noise, resulting in a 22% reduction in the maximum integration step of the first integrator and relaxing the slew rate requirement for the OTA to 9.5 V/µsec (diff). The summation of feedforward paths is embedded in a multi-input quantizer to minimize power and area. Implemented in a 0.13-µm CMOS technology and clocked at 4 MHz, the modulator achieves 87.0 dB SNDR and 91.8 dB DR for a 20-kHz signal bandwidth while consuming 99.7 µW from a 0.7-V supply.

I. INTRODUCTION

Input feedforward structure has gained popularity in sub-1V supply voltage ∆Σ data converter designs due to its advantage of small signal swing in the loop filter. Discrete-time (DT) ∆Σ modulator seems to be the preferred choice over continuous-time (CT) counterpart for audio applications due to high dynamic range (DR) requirement, which is challenging for CT modulators, especially for DR over 90 dB. However, DT modulator suffers from stringent settling time requirements for the integrators. Particularly, the settling in the first stage of modulator is crucial. Poor settling in the first stage leads to an increase in the noise floor, hence degrades the performance of modulators. It is challenging to achieve a high dynamic range of more than 90 dB if power consumption is capped under 100 µW [1-4].

In this paper we show that it is possible to achieve a dynamic range of more than 90 dB under sub-1V supply voltage and within 100 µW power budget through both architecture and circuit level optimization. We explore the influence of the settling of the first stage on the quantization noise leakage, and demonstrate the approach with measured results from a fabricated chip.

The paper is organized as follows: Section II describes choice of the system architecture. Section III discusses settling issue related to the quantization noise leakage and circuit design of the analog building blocks. Section IV reports the measurement results, and the conclusion is drawn in Section V.

II. ARCHITECTURE DESIGN

Single-loop single-bit ∆Σ modulator is a preferred choice for both power consumption and performance reasons in sub-1V design [1-4]. The investigation of filter order and oversampling ratio (OSR) is essential in achieving high DR for a single-loop single-bit feedforward structure. Fig. 1 shows the achievable signal-to-quantization-noise ratio (SQNR) versus input amplitude and OSR, for loop filter orders of 3, 4, and 5, respectively. It can be seen that to achieve more than 90 dB DR, the OSR needs to be reasonably high. For a third-order filter, an OSR of 120 leads to the SQNR of 100 dB. Increasing the loop filter order to 4, the SQNR improves by as much as 15 dB at the same OSR while consumes 5% more power if the capacitor scaling is employed for the last stage according to simulation. Further increase in filter order, i.e. 5th order, leads to only 8 dB improvement of SQNR, but the modulator suffers from stability problem when input amplitude exceeds -4 dB as well as further increase in power consumption. A fourth-order loop filter is therefore a promising choice to achieve a high DR and maintain good power efficiency.

The minimum supply voltage of the modulator is mainly determined by the opamp. Without using special low-voltage techniques such as body input, most low-voltage low-power opamps in deep-submicron CMOS technologies require the supply voltage to be higher than 0.5 V. As for the technology we used (VTHN+|VTHP| ≥ 0.4V), it is possible to reduce the
supply voltage to 0.7 V and guarantee the performance of opamps. The reference voltage is set to 0.7 V as well. To determine the size of sampling capacitors and the OSR, we simulate the signal-to-noise ratio (SNR) versus the sampling capacitor size for different OSRs based on MATLAB behavioral model, as shown in Fig. 2. The noise simulated covers thermal noise and quantization noise. It can be seen that the SNR increases more rapidly when the capacitor is small. When it is below 3 pF, the net improvement of the SNR versus the net incremental of capacitance, i.e. $\Delta \text{SNR}/\Delta C$, is 2.1 dB/pF. When it is above 3 pF, the $\Delta \text{SNR}/\Delta C$ reduces to 0.75 dB/pF. In order to achieve 95 dB SNR, we choose the sampling capacitor size of 3 pF and the OSR of 100 for the modulator.

To minimize the power, the integration step of the first stage should be as small as possible since the first integrator usually consumes more than 60% of total power [1, 3]. However, the level of the integration step is closely related to the quantization error. One effective way to attenuate the high frequency quantization error is to insert a FIR filter into the feedback loop [5]. This method does not incur any non-linearity from the feedback DAC and requires no DEM circuits. Furthermore, the residual error at the input of the first stage is suppressed, leading to reduced integration step, which is illustrated in Fig. 3. The integration step declined dramatically with increase of the length of the filter, as shown in Fig. 4. Increasing the length to 4 reduces the integration step by more than 50%, but the minimum compensation coefficient, which is 0.001, is too small to implement. Thus, a 2-tap FIR filter is adopted in the design. The overall modulator structure is shown in Fig. 5. Behavioral simulation result shows that the maximum integration step is reduced by 22% and the accumulated integration step is only 58% of that without the filter.

Prediction of leakage of the quantization noise is important for achieving desired performance in low-voltage low-power ΔΣ modulator design. Existing behavioral simulation does not provide a good prediction on the noise leakage while full transistor level simulation prolongs entire design process. To address this issue, we use a mixed-mode simulation for leakage prediction, which is flexible and less time consuming. Under the mixed-mode simulation, all building blocks are based on transistor level design, except for opamps which are modeled by small signal models. For the first stage, the opamp is modeled as a fully differential one by voltage-control-current-sources and resistors. For opamps in the downstream stages, they are modeled by voltage-control-voltage-sources to save simulation time since non-idealities of the downstream integrators have little effect on the leakage.

In order to estimate the quantization noise leakage, we separate the unshaped quantization noise from the shaped one for evaluating the leakage power. The leakage power is evaluated by accumulating the quantization noise spectrum within a half of signal band, i.e. 10 kHz, under different gain bandwidth (GBW) settings of the first stage opamp. Fig. 6 shows the percentage of noise leakage over total inband quantization noise versus the first opamp’s GBW, where the DC gain is fixed at 35 dB. It can be seen that the noise leakage due to the opamp bandwidth contributes more than 30% to the
the total inband quantization noise when the GBW is below 6 MHz. When the GBW is above 25 MHz the noise leakage declines slowly and occupies less than 12 % of the total. It is clear that the noise leakage degrades SQNR by more than 5 dB when the GBW is reduced from 25 MHz to 6 MHz.

The DC gain does not have clear influence on the leakage. When the GBW is fixed at 25 MHz, the leakage is almost constant when DC gain increases from 29 dB to 41 dB. For achieving a better SNR, it is desirable to let GBW of the first opamp reasonably high so that the noise leakage can be minimized.

### III. CIRCUIT IMPLEMENTATION

The schematic of the switch level design is shown in Fig.7. All switches are implemented with bootstrapped switches to increase linearity in a low-voltage environment. Two non-overlapped signals are generated from the on-chip clock generator.

#### A. 2-tap FIR DAC

Fig.8 shows the signal timing diagram of the feedback signal and the first stage output. The quantizer resolves a comparison at the end of $\Phi_2$. Within one clock period, the integration of the first stage occurs twice in both $\Phi_1$ and $\Phi_2$, respectively. According to the time domain, at the end of $\Phi_1$,

$$V_o(n) = V_o(n-1) + X(n-1) - \beta(n-2) + 0.1.$$  \hspace{1cm} (1)

At the end of $\Phi_2$,

$$V_o(n) = V_o(n-1) + X(n-1) - \beta(n) + 0.1.$$  \hspace{1cm} (2)

where $V_o(n)$ is the output of the first stage, $X(n)$ is the input signal, $\beta(n)$ is the feedback signal. Adding (1) to (2) and taking $z$-transfer transform on the sum, we have

$$V_o(z) = V_o(z)z^{-1} + X(z)z^{-1} - 0.2 + \beta(z)z^{-1} + \frac{1}{2}.$$  \hspace{1cm} (3)

It is clear from (3) that the feedback signal has been filtered.

#### B. Power-efficient Rail-to-rail Amplifier

Fully differential opamps, such as gain-enhanced current mirror opamp [1], are selected for our design as they provide better settling, common mode rejection ratio and charge injection immunity. NMOS input differential pairs are used to increase the transconductance efficiency while their geometric sizes are carefully determined to suppress the flicker noise. Special care has been taken to keep same effective load capacitance in both phases for the first stage. Full transistor level simulation shows that with DC gain of 41 dB and GBW of 30 MHz the quantization noise leakage occupies less than 20 % of total inband quantization noise.
C. Multi-Input Quantizer

Conventionally, the summation of the feedforward paths is realized by switched-capacitor summation circuits, which requires \(2 \times (N+1)\) capacitors and extra switches for an \(N\)-th order loop filter. In this work, the summation function is embedded in the quantizer to simplify the summation circuits [6]. The quantizer consists of a multi-input comparator and a SR latch. The feedforward paths are implemented by directly feeding the output of each integrator to the comparator. The ratio \((W/L)\) of the input pairs of the multi-input comparator is used to realize the feedforward coefficients.

IV. MEASUREMENT RESULTS

The prototype fourth-order feedforward \(\Delta\Sigma\) modulator is fabricated in a 1P8M 0.13-\(\mu\)m CMOS process with MIM capacitor. All references are externally buffered. Fig. 10 shows the chip micrograph. Fig. 11 shows the measured 64k-points output spectrum for a 2.33-kHz sinusoidal input. The measured SNR and SNDR versus input amplitude is presented in Fig. 12. The measured performance is summarized in Table I. Table II compares the proposed \(\Delta\Sigma\) modulator with other published sub-1V \(\Delta\Sigma\) modulators. The modulator achieves the best FOM, where FOM is defined as

\[
DR + 10\log_{10}(BW/Power).
\]

Table I: Performance Summary

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<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
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<tr>
<td>Supply Voltage</td>
<td>0.7 V</td>
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<tr>
<td>Sampling Frequency</td>
<td>4 MHz</td>
</tr>
<tr>
<td>References</td>
<td>0 V, 0.7 V</td>
</tr>
<tr>
<td>Full scale input range</td>
<td>1.4 (V_{pp})</td>
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<tr>
<td>Signal Bandwidth</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>68.2 (analog)+31.5 (digital)= 99.7 (\mu)W</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>91.8 dB</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>91.4 dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>87.0 dB</td>
</tr>
<tr>
<td>Core Area</td>
<td>1.27 mm x 0.55 mm</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13 (\mu)m CMOS</td>
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Table II: Performance comparison with state-of-the-art low-power low-voltage \(\Delta\Sigma\) audio modulators

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<tr>
<td>[1]'04</td>
<td>1.0</td>
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<td>81</td>
<td>88</td>
<td>140</td>
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<tr>
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<td>83</td>
<td>60</td>
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<td>20</td>
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<tr>
<td>This work</td>
<td>0.7</td>
<td>20</td>
<td>87.0</td>
<td>91.8</td>
<td>99.7</td>
<td>174.8</td>
</tr>
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</table>

V. CONCLUSION

A 0.7 V \(\Delta\Sigma\) modulator with a peak SNDR of 87.0 dB is presented in this paper. By employing input feedforward structure and FIR filter, the integration step for the first stage as well as slewing requirement is reduced. In addition, the circuit implementation is simplified with embedded feedforward path summation. The measurement results show that the inband noise power is as low as desired and the modulator has achieved a peak DR of 91.8 dB under 100-\(\mu\)W power budget.

ACKNOWLEDGMENT

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REFERENCES