Blue-Noise Sigma-Delta Modulator: Improving Substrate Noise and Nonlinear Amplifier Gain Effects

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Abstract— This paper presents a method to reduce the effects of substrate noise and nonlinear amplifier gain on sigma-delta (ΣΔ) modulators through the use of blue-noise modulation. In addition to reducing the effects of substrate noise and nonlinear amplifier gain, the proposed architecture also suppresses the effects of integrator opamp non-idealities, such as 1/f noise and DC offset, and DAC DC offset and even-order nonlinearities. The architecture proposed herein is referred to as the blue-noise ΣΔ modulator. An example utilizing a third-order blue-noise ΣΔ modulator with a 1-bit quantizer is presented. Additionally, a method to generate the required blue-noise modulation sequence is proposed. Simulation results demonstrate that this architecture achieves an 8.8dB improvement in SNDR over the traditional third-order ΣΔ modulator.

I. INTRODUCTION

As CMOS technology scaling continues to reduce feature size, chip designers will be integrating more and more analog and digital circuitry together on the same die in an effort to reduce cost. However, as pointed out in [1] and [2], integration of systems-on-a-chip (SoC) requiring the placement of noise-sensitive analog blocks and noisy digital signal processing blocks together on a common substrate will most likely continue to increase the effect of substrate noise generated by the digital circuitry. In particular, mixed-signal designs such as ΣΔ ADCs, where the analog and digital components cannot necessarily be placed far from each other, will see significant performance degradations due to substrate noise. According to [3], the SNDR of a ΣΔ modulator may decrease by over 20dB in the presence of noisy digital circuitry such as toggling inverters.

ΣΔ modulator performance is also adversely affected by non-ideal integrator opamp DC gain factors, in particular finite DC gain and nonlinear DC gain. The effect of finite DC gain on ΣΔ modulator performance has been well documented in literature to produce integrator leakage in which only a fraction of the previous output sample is added to the current input sample. This affects the extent to which the ΣΔ modulator shapes low-frequency quantization noise [4]. However, the effects of nonlinear DC gain on ΣΔ modulator performance have been largely overlooked until recently [5]. According to [5], nonlinear DC gain introduces harmonic distortions into the modulator output spectrum and also increases the in-band noise floor. This is further examined in Section II.

It is well known that ΣΔ ADCs are suitable for high resolution and low-to-moderate bandwidth applications. However, when circuit nonidealities such as substrate noise and nonlinear amplifier gain are introduced into the ΣΔ modulator, dynamic range is sacrificed. To remedy this, the blue-noise ΣΔ modulator architecture presented herein utilizes blue-noise modulation, whereby a signal with blue-noise spectral characteristics, used as a chopper modulation signal, eliminates the substrate noise and nonlinear amplifier gain spectral peaks by spreading them as noise across the entire modulator spectrum. This noise, along with the resulting quantization noise, is then shaped away from the baseband input signal to high frequency as is typical for oversampling ΣΔ modulators. The proposed method eliminates the strong distortion component near DC created by harmonics of the digital sampling clock and the even-order harmonics produced by the nonlinear amplifier gain.

II. NONLINEAR AMPLIFIER DC GAIN

Finite integrator amplifier DC gain results in integrator leakage, whereby only a fraction of the previous output sample is added to the current input sample. The transfer function representing a leaky integrator is given in Eq. (1), where $\alpha = 1-A_0^{-1}$ is defined as the integrator leakage factor ($A_0$ is the amplifier DC gain).

$$H(z) = \frac{1}{1-\alpha z^{-1}}$$

(1)

However, the amplifier DC gain does not remain constant over the range of all amplifier output values due to the change in the output transistors’ output resistance [5]. In reality where large-signal swings are common at the amplifier output, the amplifier DC gain is a function of the amplifier output voltage, $v_{out}$.
In particular, an amplifier with an NMOS common-source output stage will have higher DC gain for lower amplifier output voltages, and the DC gain will decrease as the amplifier output voltage increases. This was verified through simulation of a two-stage amplifier utilizing an NMOS common-source output stage with a PMOS active load. The resulting DC gain as a function of the output voltage for the two-stage amplifier is shown in Figure 1. The amplifier nonlinear DC gain characteristic causes the overall integrator gain and corresponding pole to constantly change as a function of the output voltage value [5]. Since the integrator gain is a function of the output value and the output value depends on the previous input signal samples (i.e., integrator's gain depends on the input signal), the integrator exhibits non-linear behavior and harmonic distortions are introduced into the modulator output.

Figure 2. Traditional third-order ΣΔ modulator.

III. BLUE-NOISE ΣΔ MODULATOR DESIGN

The blue-noise ΣΔ modulator is obtained by placing pairs of blue-noise multipliers before and after each non-delayed integrator in a traditional ΣΔ modulator, such as the one shown in Figure 2. In the case of a sample-delayed integrator, the integrator is first separated into a non-delayed integrator followed by the delay element, as shown by the final integrator in the cascade of integrators with feedback structure depicted in Figure 2. The multiplying sequence, \( e[n] \), used to modulate the signals throughout the blue-noise ΣΔ modulator is a sequence of 1’s and -1’s that has blue-noise spectral characteristics (i.e., the spectrum has a low frequency deficiency).

Blue-noise multipliers receiving identical blue-noise sequences are introduced into the modulator structure in pairs. Since each multiplier in the pair is provided the same sequence of 1 and -1 they effectively perform multiplication by 1, leaving the overall modulator function unchanged. Once the blue-noise multipliers are inserted, as shown in Figure 3a, one multiplier from each pair is moved through the modulator to produce the blue-noise ΣΔ modulator structure shown in Figure 3c. Figure 3b shows the intermediate stage in rearranging the blue-noise multipliers to create the blue-noise ΣΔ modulator.

Figure 3. (a) Third-order ΣΔ modulator with blue-noise multiplier pairs added. (b) Third-order ΣΔ modulator with blue-noise multipliers rearranged. (c) Third-order blue-noise modulated ΣΔ modulator.
The dashed arrows in Figures 3a and 3b depict the direction in which a particular blue-noise multiplier is moved. When the blue-noise modulation signal, \( e[n] \), is pushed through the delay element, \( z^{-1} \), the resulting modulation signal is the delayed blue-noise sequence, \( e[n-1] \). The structural transformation described here may be applied to any traditional \( \Sigma \Delta \) modulator to create a blue-noise \( \Sigma \Delta \) modulator.

The blue-noise \( \Sigma \Delta \) modulator architecture presented in Figure 3c incorporates the non-delayed blue-noise modulated (BNM) integrator and the sample-delayed BNM integrator structures. These structures take on the same architecture as the mirrored integrator structures proposed in [6]. A distinct advantage of the proposed blue-noise \( \Sigma \Delta \) modulator is that it is not a major design digression from mature \( \Sigma \Delta \) modulator technology.

In addition to spreading substrate noise and nonlinear amplifier gain spectral peaks, blue-noise modulation also negates the effects of integrator opamp and DAC nonidealities (1/f noise, DC offset, and even-order nonlinearities). The blue-noise \( \Sigma \Delta \) modulator shapes the input signal about the Nyquist frequency before it sees the nonidealities from the integrator opamps and DAC and shapes the quantization noise toward low frequency. Traditional \( \Sigma \Delta \) modulators shape the quantization noise toward high frequency while leaving the low frequency input signal unchanged. The input sinusoidal signal spectra before and after blue-noise modulation are shown in Figure 4. The undesirable circuit noise contributions will remain at low frequency where the quantization noise is shaped by the blue-noise \( \Sigma \Delta \) modulator. When the output signal experiences the final blue-noise modulation, the input signal is returned to baseband, while the quantization noise along with the low frequency circuit nonidealities are shaped toward high frequency. This procedure is much like that described in [7] for the mirrored-integrator \( \Sigma \Delta \) ADC.

**IV. BLUE-NOISE SEQUENCE GENERATION**

The spectrum of a blue-noise sequence consists of low frequency deficiencies and uncorrelated high-frequency fluctuations that are classified as high-frequency white noise [8]. The spectrum of a typical blue-noise sequence is shown in Figure 5.

The binary blue-noise sequence necessary for blue-noise modulation can be generated using an all-digital \( \Sigma \Delta \) modulator. Replacing the integrators from a traditional \( \Sigma \Delta \) modulator with accumulators produces the all-digital \( \Sigma \Delta \) architecture, which is shown in Figure 6. Since the blue-noise sequence used in the blue-noise \( \Sigma \Delta \) modulator consists only of 1’s and –1’s, the quantizer in the all-digital \( \Sigma \Delta \) modulator needs to resolve \( B = 1 \) bit. Similar algorithms that produce blue-noise sequences have been proposed for fractional-N PLL applications [9] and for DAC dynamic-element matching in multi-bit \( \Sigma \Delta \) ADC applications [10].

**V. SIMULATION RESULTS**

The behavioral simulation results presented here were obtained from Matlab/Simulink models of a third-order, 1-bit \( \Sigma \Delta \) modulator. The input used for the simulations was a sinusoidal signal with frequency \( f_{in} = 4.1 \) kHz lying within a 32.8 kHz bandwidth. The OSR was selected to be 128, resulting in a sampling frequency of \( f_s = 8.397 \) MHz. The substrate coupling noise used for the simulations was obtained in the lab from Maxim IC’s MAX1403 18-bit \( \Sigma \Delta \) ADC. The measured noise, which contained the digital sampling clock and several strong higher harmonics and subharmonics, was imported into Matlab for the simulations and
injected into the first integrator in the ΣΔ modulator. Additionally, the nonlinear amplifier DC gain results presented in Section II are included in the model for the first integrator. In order to provide realistic simulations, non-ideal amplifier models were used for the integrators. The simulations were performed assuming room temperature, a finite amplifier gain (63dB), finite gain-bandwidth (150MHz), slew rate (20V/µs), and saturation. In addition to the amplifier non-idealities, clock jitter was also taken into account.

The output spectrum of a typical third-order 1-bit ΣΔ modulator is shown in Figure 7. The output spectrum clearly depicts the modulator’s vulnerability to low-frequency noise as well as even- and odd-order harmonics from the nonlinear amplifier gain, which limits the SNDR to 76.6dB in simulation. The output spectrum of the blue-noise ΣΔ modulator, shown in Figure 8, reveals that this architecture suppresses the low-frequency distortions near DC as well as the even-order harmonics created by the nonlinear amplifier gain. The resulting SNDR for the blue-noise modulated architecture using the same parameters as the simulation without blue-noise modulation is 85.4dB. The proposed architecture demonstrates an 8.8dB improvement in SNDR from the traditional ΣΔ modulator design, which translates to an increase in effective resolution of 1.2 bits.

VI. CONCLUSION

The blue-noise ΣΔ modulator has been proposed and described. The proposed design is not a major design digression from mature conventional ΣΔ modulator topology. Simulations of this architecture have proven the ability to suppress the effects of substrate noise generated by noisy digital blocks placed on the same die as sensitive analog circuits and nonlinear amplifier gain created by nonsymmetrical device properties. In addition to attenuating substrate noise and even-order nonlinear amplifier gain spectral peaks, the proposed design eliminates 1/f noise, DC offset, and even order non-linearities. For the 1-bit, third-order blue-noise ΣΔ modulator with an OSR of 128, an overall improvement in SNDR of 8.8dB has been demonstrated. In an ongoing effort, we plan to demonstrate the effectiveness of the blue-noise modulation in higher-order low-pass and band-pass ΣΔ modulator prototypes.

REFERENCES