A Novel Multiprocessor Architecture For Massively Parallel System

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Abstract—Multiprocessor architecture is the main resource to speed up applications by incorporating parallelism among various processing elements. The success of multiprocessor system depends how much efficiently the concurrent processes are managed on the system. This paper proposes a novel multiprocessor architecture which is less complex, easily extensible and inherits most of the desirable topological properties. The proposed system is capable to manage the distributing of parallel tasks efficiently when appropriate scheduling schemes are implemented on it. The comparative study shows that the proposed architecture could be used effectively in various multi-processing applications.

Keywords- multiprocessor network; parallel system; scalability; Task scheduling; diameter.

I. INTRODUCTION

A suitable multiprocessor architecture is a core component of parallel systems. The system consists of various processing elements known as nodes. These multiprocessor architectures are evaluated in terms of good topological properties such as low degree, small diameter, lesser complexity and cost. Several multiprocessor topologies have been proposed and studied in the literature [1] [2]. The binary n-cube is known as a hypercube and it is well-known network because it possesses quite a few desirable features. These properties include regularity, symmetry, small diameter, strong connectivity and relatively small link complexity [3] [4] [5]. Also variations of hypercube topology have been proposed to further improve some of its features. It is usually needed that the size of the network in terms of the number of nodes can be increased with minimum or virtually no alternation in the existing configuration. Furthermore, the increase in the size should never degrade the overall performance of the final system [6] [7]. A large number of hypercube variant have been reported, most notably crossed cube (CQ) [8], Exchange Hypercube (EH) [9], Extended Crossed cube (ECQ) [10], Star graph S(n) [11], Star Cube (SC) [12] and Star Crossed Cube (SCQ) [13] etc. A CQ is derived from an HC by changing the way of connections of some HC links. The diameter of a CQ is almost half of that of its corresponding HC and equal to [(n+1)/2] where as the diameter of an n-dimensional HC is n. However, the CQ makes no improvement in the hardware cost compared to the HC. An n-dimensional HC is composed of 2^n nodes and has n links per node. The number of links of an HC, which is directly related to the hardware cost, grows more drastically than the number of processors. This leads to rapid increase of the hardware cost as an HC scales up [14]. EH is an excellent topology with the lower hardware cost [9]. An EH is based on link removal from an HC, which makes the network more cost-effective as it scales up. Unfortunately, the availability of rich connectivity in the EH is reduced [9]. Though EH offers lesser cost compared to the HC, but there is no improvement over the diameter of the EH. The demand for reduction of the diameter of the HC as well as its hardware cost motivates our investigation in proposing a new interconnection network.

Another class of multiprocessor architecture is the Star graph has been widely used as an alternative to hypercube [11] [15]. The important feature of star graph are fault tolerance, partition ability and easy routing and broadcasting. The major drawback of S(n) is increasing with higher value to the next higher dimension. For the improvement of star graph, another variation of star graph is introduced called Star Cube (n,m). When compared with star S(n), the growth of S(n,m) is comparatively small and smallest possible structure contains twenty four number of processor with node degree four. It is very suitable for variable node size architectures. The experts have never reported any linear extensible network with lesser diameter. Hypercube architecture, that may be the best possible one for parallel computing is commercially accepted unfortunately its expansion is exponential (2^n). In recent times a Linear Extensible Cube (LEC) network has been reported [16] employing lesser number of processing elements and smaller diameter. A dynamic scheduling scheme i.e. Two Round Scheduling Scheme (TRS) has been implemented on LEC to show that LEC is the much better organizational multiprocessor model with lesser number of nodes [17].

In this paper a new topology is designed to make the system less complex, cost-effective and scalable. The proposed topology has been designed in the line of LEC which combines the advantage of hypercube and LEC. To evaluate the performance of proposed architecture, a standard dynamic scheduling namely Minimum Distance Scheme (MDS) has been implicated to show the performance of the proposed network in term of load imbalance and the load balancing time. MDS operate on the principle of minimum distance property which schedules the incoming tasks on directly connected nodes. This feature is incorporated with the help of adjacency matrix at the time of implementation.

The rest of the paper is organized as follows: Section 2 presents the architectural details of similar multiprocessor...
architectures with their topological properties. The proposed multiprocessor architecture is presented and discussed in section 3. The performance of the proposed network is evaluated by implementing standard dynamic scheduling scheme on it and simulation results are discussed in Section 4. Finally the paper is concluded in section 5.

II. ARCHITECTURAL BACKGROUND

This section explains the topological features of the similar architecture to give a background of the proposed topology. It includes Crossed Cube (CQ), Star Crossed Cube (SCQ) and Linearly Extensible Cube (LEC). The above said interconnection network topologies are expressed using graph theoretical terminologies and notations. These topologies are discussed in order to compare the architectural features.

A. Crossed Cube (CQ)

The Crossed Cube CQ (n) is derived from the hypercube by changing the way of connection of some hypercube links. The CQ (n) is a regular graph of 2ⁿ nodes. All nodes in the CQ (n) are identified by a unique binary string of length n.

Definition 1 The Two binary strings of length two, P= p₁p₂ and Q= q₁q₀ are said to be pair related, if and only if.

\[(P, Q) \in \{(00, 00), (10, 10), (01, 11), (11, 01)\}\]

Definition 2 The Crossed Cube of n-dimensional, denoted by a CQ (n). The CQ (n) is the complete graph with two vertices on level 0 and 1. For n>1, the CQ (n) contains CQ₀ \text{ and } CQ¹ \text{, joined according to the following rule: the node } u= 0 \text{ u₀……..u₀ from CQ ¹ₙ₋₁, } if

1) \text{ uₙ₋₂ = vₙ₋₂, if n is even, and}

2) \text{ For } 0< = i < \text{ (n-1) /2}, \text{ u₂i+1 u₂i } \sim v₂i+1 v₂i

Figure 1 shows the crossed cube of dimension n=3 and n=4.

![Crossed Cube of 3 & 4 dimensions](image)

In CQ (n), every node with a leading 0 bit has exactly one neighbor with a leading 1 bit and vice versa. The CQ (n) is a connected, regular graph of degree n with 2ⁿ nodes.

B. Star Crossed Cube

Definition The Star crossed cube SCQ (m, n) is derived from CQ (n) and the star graph S(m). In S (m), each vertex is replaced with a CQ (n). The node address of each vertex in the resulting graph will have two parts.

1) \text{ xₘ₋₁, xₘ₋₂… x₀}

2) \text{ y₀, y₁………..yₙ₋₁}

Where the xₙ represent the CQ part and yᵣ represent the star part.

Each node will have two types of neighbors, namely the CQ part neighbors and star part neighbors with node addresses.

1) \text{ < xₘ₋₁, xₘ₋₂…x₁ x₀, y₀, y₁ ………yₙ₋₁>}

2) \text{ < xₘ₋₁, xₘ₋₂…, x₁ x₀, y₁, y₁-₁ ………yₙ₋₁>}

The SCQ (3, 3), along with the sub modules, is shown in Figure 2(a), 2(b) and 2(c), respectively. In figure 2(a), the first sub module with the star part labeled as 123 and the corresponding labels of the CQ (n) are shown. Similarly, Figure 2(b) shows the second sub module of the SCQ (3, 3) with 213 as their star part level.

![The SCQ: (123) and corresponding CQ](image)

Figure 2. (a) The SCQ: (123) and corresponding CQ

![The SCQ: (3,3)](image)

Figure 2. (b) The SCQ: (3,3)

C. Linearly Extensible Cube (LEC)

Definition Let Q be a set of N identical processors, represented as \text{ Q’ = \{P0,P1,P2,……..PN-1\} }
The number of processors \( N \) in the network is given by \( 2^n \) for 
\( n=1, 2, 3, \ldots, d \) where \( d \) is the depth of the network. For different 
depths, server having 2, 4, 6, 8, 10 \( \ldots \) processors are possible.

In order to define the link functions we denote each processor in 
the set \( Q \) as \( P_{ij} \), \( j \) being the level in the architecture where 
the processor \( P_i \) resides. As per extension policy, only two processors 
exist at level \( j \). Thus at level 0, \( P_0 \) and \( P_1 \) exist and it may be re-
designated as \( P_{00} \) and \( P_{10} \), and so on. The arrangement of 
processors is below.

\[
\begin{array}{cccc}
P_{00} & P_{10} \\
P_{21} & P_{31} \\
P_{42} & P_{52} \\
\cdots & \cdots \\
\end{array}
\]

Arrangement of processors in LEC

The diameter of LEC architecture is \( \sqrt{N} \) and it has a constant 
node degree four as shown in Figure 3.

Let \( q \) be the set of designated processor of \( Q \) thus, 
\( q = \{P_i\}, 0 \leq i \leq N-1 \)

The Link functions \( E_1 \) and \( E_2 \) define the mapping from \( q \) to \( Q \) as.
\[
E_1 (P_i) = P((i+2) \mod N) ; \quad \forall P_i \in q
\]
\[
E_2 (P_i) = P((i+3) \mod N)
\]
The two functions \( E_1 \) and \( E_2 \) indicate the links between various 
processors in the network. Figure 4 shows the proposed linear 
arquitectural network with eight processors.

B. Topological Properties

The following are the various topological properties of the 
proposed linear architecture network.

**Theorem 1:** The total number of nodes in the proposed 
linear architecture is \( \sum_{i=0}^{N} K \).

**Proof:** The total number of nodes in \( CQ (n) \) is \( 2^n \) nodes. The 
proposed linear architecture is an undirected graph, where the 
total number of nodes is given below:
\[
N = \sum_{i=1}^{K} K \quad \text{e.g. } \{1, 3, 6, 15, 21 \ldots \}
\]
It shows that the network grows linearly, where \( 1 \leq K \leq n \), \( n \) is the 
level number up to which the network is designed.

**Theorem 2:** The degree of nodes of proposed linear 
arquitectural architecture is 4.

**Proof:** In \( CQ (n) \), the degree of nodes is defined as the total 
number of edges \((n-1) \) incident on each vertex. Hence, the degree of 
each vertex in the proposed linear architecture is remain 
constant i.e. 4 irrespective of the depth of network. The behavior 
is shown in Table 1.

III. PROPOSED TOPOLOGY

This Section describes the architectural details of the proposed 
interconnection network. In the first part architecture is 
defined where as in the second part its topological properties 
are explained. These properties are also compared with other 
standard networks.

A. Proposed Architecture

**Definition** The Proposed linear architecture is undirected graph 
and grows linearly in cube like shape.

Let \( Z \) be a set of \( N \) identical processors, represented as 
\( Z = \{P_0, P_1, P_2 \ldots, P_{N-1}\} \)
The Total number of processor in the network is given by
\[
N = \sum_{i=0}^{N-1} K
\]
Where \( n \) is the depth of the network. For different depth, network 
having 1, 3, 6, 10, 15, 21 \ldots processors are possible.

In order to define the link functions, we denote each processor in 
a set \( K \) as \( P_{in} \), \( n \) being the level/depth in proposed linear 
arquitectural where, the processor \( P_i \) resides. As per the proposed 
linear architecture extension policy, one and two processors exist 
at level/ depth \( n \). Thus at level 1 \( P_0 \) and \( P_1 \) exit and at level 2 \( P_2 
and \( P_3 \) as shown in Figure 4.
Table 1: Diameter and Degree of Linear Architecture

<table>
<thead>
<tr>
<th>Level</th>
<th>Number of processors</th>
<th>Diameter</th>
<th>Degree</th>
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<td>0</td>
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<td>5</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>36</td>
<td>6</td>
<td>4</td>
</tr>
</tbody>
</table>

Theorem 3: The diameter of the proposed linear architecture is \( (\sqrt{N}) \).

Proof: The diameter of network is the maximum eccentricity of any node in the network. It is the greatest distance between any pair of nodes. In proposed linear architecture, it is observed that the diameter does not always increase with the addition of a layer of processors. It may be highlighted that the diameter of proposed linear architecture shows a maximum value of 20 for 120 processors. The behavior is shown in Table 1.

Theorem 4: The extensibility of proposed linear architecture is \((n+1)\).

Proof: In the proposed linear architecture, the extension complexity increases linearly, the network may be extended in a layer of one node or two nodes as shown in Figure 5. It is major advantage of Proposed linear architecture network, can increase with even number of processors and as well as odd number of processors with same extensibility of network. Figure 5 (a) and Figure 5 (b) shows the extensibility of proposed linear architecture.

Figure 5. Linear architecture Extension

IV. COMPARATIVE STUDY

To make a general conclusion on architecture comparative study is carried out. We consider three important parameters namely, number of processor, diameter and degree. The curves are plotted for each of the parameters for proposed linear architecture, LEC and HC. The HC is increasing number of processors at various level of architecture. An exponential expansion is obtained in all the case as shown in Figure 6. However, it attains larger numerical values even at lesser number of levels. In LEC, the number of processor is increases exponentially. On the other hand proposed linear architecture (LA) shows better results from the other networks and the number of processor increases linearly with an addition of even or odd processors at each level of architecture.

Figure 6. Number of processor of various multiprocessor architectures

Figure 7. Diameter of various multiprocessor architectures

The result shows that all the networks are having comparable values of the node degree while considering equal number of nodes. The degree defines the largest degree of all the vertices in its graph representation. In particular, the LEC is having lesser values of the node degree as compare to HC and this trend is shown in Figure 8. So, the degree of proposed linear architecture remains always constant.

Figure 8. Node degree of various multiprocessor architectures
V. PERFORMANCE ANALYSIS

To map the task on network of nodes the important concepts widely used called the scheduling of tasks. Several scheduling schemes have been reported that manage the distribution of load on a multiprocessor network dynamically and efficiently [16] [17] [18] [19] [20]. In the proposed work we have tested the performance of proposed linear architecture by applying a simple scheduling algorithm known as Minimum Distance scheduling scheme (MDS) [18]. This algorithm is based on the principle of minimum distance feature. For load balancing, the above mentioned (MDS) scheme calculates the value of Ideal Load (IL) at each stage of the load. IL is the load a processor is having when the network is fully balanced. The algorithm identifies the under loaded (acceptor) and overloaded processors (donors). Each donor processor, during balancing, selects tasks for migration to the various connected and underloaded processors. Migration of tasks can take place between donor and acceptor processors only based on the value of IL.

The Load imbalance factor for ith level, denoted as LIFi, is defined as:

\[ LIF_i = \left( \frac{\text{load}_i(P_k) - (\text{ideal load})_i}{(\text{ideal load})_i} \right) \]

where,

\[ (\text{ideal load})_i = \left( \frac{\text{load}_0(P_0) + \text{load}_1(P_1) + \ldots + \text{load}_{i-1}(P_{N-1})}{N} \right) \]

and max (load, (Pi)) denotes the maximum load pertaining to level i on a processor Pi, 0 ≤ i ≤ N-1, and loadi(Pi) stands for the load on processor Pi due to ith level.

For the purpose of comparison the same algorithm is also applied on LEC & HC networks. For simulation we assume a simple problem characterization in which the load is partitioned in to a number of tasks. All tasks are independent and many be executed on any processor in any sequence. The performance has been by simulating artificial dynamic load on the different networks. The simulation run consist of generating uniform load mapping it on various nodes of the system and finally imbalance is obtained for various stages of the tasks structures and the curves are plotted as the average percent imbalance against the load for different stages shown in Figure 9.

VI. CONCLUSION

In this paper a new network topology known as linear architecture for multiprocessor systems has been proposed. The attempt is to combine the desirable features of linearly extensible structures and the standard hypercube architectures. The proposed architecture exhibits better connectivity lesser number of nodes, lesser diameter and extension of even or odd nodes at each level of architecture. The performance of linear architecture has been tested by implementing standard dynamic scheduling scheme onto it as well as on other similar network architectures. The comparative simulation study shows that the proposed linear architecture producing better results in terms of managing the tasks as compared to other similar multiprocessor networks. The architecture is low cost and posses the desirable topological properties. The performance of proposed linear architecture may further be improved by designing specific scheduling scheme with lesser complexity.

REFERENCES


