Impact of On-Chip Interconnect Frequency-Dependent $R(f)L(f)$ on Digital and RF Design

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Abstract

On-chip interconnect exhibits clear frequency-dependence in both resistance and inductance. A compact ladder circuit model is developed to capture this behavior, and we examine its impact on digital and RF circuit design. It is demonstrated that the use of DC values for $R$ and $L$ is sufficient for delay analysis, but RL frequency dependence is critical for the analysis of signal integrity, shield line insertion, power supply stability, and RF inductor performance.

1. Introduction

Wide interconnects are often used in modern VLSI circuits for global signal lines, clock distribution, power supply, and RF spiral inductors. As chip operating frequencies have surpassed 1GHz, the depth of current penetrating into the metal (skin depth) becomes comparable to or even smaller than the cross-sectional dimensions of a global interconnect. For example, the skin depth of Cu is 2µm at 1GHz and decreases proportionally to the square root of frequency. Therefore, the conventional representation of an on-chip interconnect by a constant $R$ and $L$ (DC RL) is no longer applicable due to the strong frequency-dependence of metal impedance.

Although the phenomenon of frequency-dependent $R$ and $L$ (FD RL) has previously been a concern only for package and microwave design due to their large wire sizes, it has migrated to on-chip interconnect as the chip operating frequency increases into the 10GHz regime [1]. Using the partial-element-equivalent-circuit (PEEC) [2] based RLC extraction tool Raphael, Fig. 1(a) illustrates the cross-sectional current density distribution for three parallel lines. The thickness of the Cu lines is 1.2µm and the same technology is used throughout this work. As the frequency rises, the current segregates to the surface of the wire and moves further away from neighboring lines conducting current in the same direction. Referred to as the “skin effect” for a single-line case and the “proximity effect” when neighboring lines are inductively coupled, this non-uniform current distribution leads to significantly larger resistance at higher frequency, as shown in Fig. 1(b) (note that line inductance drops only slightly and eventually saturates).

2. Compact Ladder Circuit Model

Although PEEC is highly accurate in FD RL prediction, it requires significant computational resources. To improve the efficiency of PEEC while retaining the simulation accuracy of FD RL, we use a compact ladder circuit representation to model the current distribution inside the conductor that is affected by the magnetic field around the metal line (Fig. 2) [3]. In addition to $R_0$ and $L_0$, $R_1$ and $L_1$ are used to model the current conduction within different cross-sectional layers of metal [4]. Then, $L_m$ is added to capture the influence of outer magnetic
fields on the inner current distribution of metal. Finally, for multiple lines the DC mutual inductance is applied between the L_0 terms. Analytical formulas for each element are derived as follows:

(a) Generated from a simplified PEEC circuit model and empirical fitting with Raphael, R(f) of a single line is captured as:

$$ R_w(f) = R_{dc} \cdot \frac{1 + 100w^2t^2f^2}{1 + [L_{dc}/(10R_{dc})]^2f^2} $$

Here \( t \) and \( w \) are line thickness and width respectively. Fig. 3 verifies the accuracy of Eqn. (1) over a range of dimensions. From circuit theory, a ladder model also provides similar dependence on frequency. Thus, by matching the coefficients of \( f \), we obtain two constraints to solve for the elements of the ladder circuit.

(b) As \( R_0L_0 \) and \( R_1L_1 \) represent the partition between metal layers, their relation to is approximated to be linear [4]:

$$ L_0/L_1 = 0.315 \cdot R_1/R_0 $$

(c) DC R, L, and L_m between lines are calculated based on the closed-form equations in [6].

The resulting formulas are summarized in Table 1. The accuracy of this ladder model is demonstrated in Fig. 4. Compared with PEEC, our model provides a fast, reliable, and SPICE-compatible tool for experimental studies of FD RL. In the following sections, we use this new model to investigate the impact of FD RL in high-speed designs.

### 3. Impact on Digital Design

#### A. Signal Delay: DC RL is sufficient

Global interconnect delay is an important performance bottleneck in high performance microprocessor design. To accurately analyze the RLC interconnect with frequency dependent R and L, previous publications have proposed to use either the high frequency RL [7] or predetermined loop RL [8] values for timing estimation in the GHz regime, increasing the extraction complexity. However, a waveform comparison between DC RL and FD RL shows that the difference in predicted delay is smaller than 1%: in Fig. 5a, for a projected 0.10um CMOS technology [9], five signal lines are switched together by a 20ps ramp input, which represents the worst delay case for inductively coupled lines. The delay and rise times found using the DC RL model match well with those given by the FD RL model, as shown in Fig. 5b. This is because the inductive impedance \( \omega L \) dominates the voltage response at the fast-rising edge, and L is relatively independent of frequency (Fig. 1b). After the rising edge, the output signal slows down and resistance domi-
nates in the overshoot and ringing portions of the waveforms, so that there are significant differences in amplitude and period of ringing.

Furthermore, Fig. 5b also shows that although the approach in [8], which neglects coupling capacitance in generating loop inductances, may be suitable for well-shielded structures (e.g., clocks), ignoring multiple current return paths underestimates the inductive effects in general global interconnect structures. In conclusion, the use of DC RLC parasitics is sufficiently accurate for delay analysis.

**B. Noise Shielding: FD RL is required**

In the GHz regime, controlling crosstalk noise between coupled lines is crucial for correct logic activity and accurate signal delay. The presence of inductive coupling leads to enhanced noise as a result of fast signal transitions and the uncertainty of inductive current return loops.

For crosstalk noise reduction between RLC lines and improved control of inductive current return paths, V_{dd}/GND lines are typically inserted as shields, particularly in wide data busses and global clock distribution. Although this shielding technique can eliminate short-range capacitive coupling, it has somewhat limited impact on long-range inductive coupling [10][11]. Fig. 6a shows six parallel signal lines with V_{dd}/GND lines inserted for every three lines. When all three lines in the right region are actively switching in phase, the peak noise injected across the shielded region is not negligible, as seen in Fig. 6b. In contrast to the RC case where wider shield lines always reduce noise, Fig. 6b reveals a non-monotonic dependence of noise on shield line width due to inductance-induced signal ringing. Since high-frequency resistance dominates the voltage overshoot and signal ringing (Fig. 5b), different noise predictions are obtained from DC and FD RL models, as illustrated in Fig. 6b. Thus, depending on the shielding criteria, consideration of FD RL may lead to different shield line configurations, resulting in different area cost. As an example, if we choose V_{noise} < 10% of V_{dd} as the shielding criteria (Fig. 6b), FD RL requires 7.7% wider shield lines; meanwhile, if we use the width predicted by DC RL, the actual peak noise increases to 15% of V_{dd}, which can cause logic failure or propagating signal glitches. Therefore, the inclusion of FD RL is important for accurate analysis and effective shielding of noise.

**C. Power Supply: FD RL benefits stability**

Due to the scaling trends of lower power supplies and smaller transistor threshold voltages, more stringent requirements on power supply stability are anticipated for future IC design. Furthermore, mixed-signal designs often rely on separate power/ground grids to reduce power supply noise in sensitive analog circuit blocks. In such a design, extra modeling attention should be paid to power supply noise since signals traveling between circuits on different power grids may be particularly problematic [12]. We investigate the impact of FD RL on power supply noise using the simplified logic switching model in Fig. 7. Identical V_{dd} and GND lines are assumed (w=50µm, length=500µm). The logic block between them is modeled as a ramped current source (rise time=20ps, V_{dd}=1V for 0.10µm technology). The decoupling capacitor is added in order to reduce the noise on V_{dd} and GND.
Induced noise on ground is shown in Fig. 8. As a result of the larger resistance at higher frequency, L(di/dt) noise is suppressed. FD RL predicts smaller peak and faster damping (Fig. 8). This implies that less decoupling capacitance is required to stabilize the power supply when considering the frequency-dependence of metal impedance. In our example, to reduce the peak noise below 10% of $V_{dd}$, DC RL predicts 134pF of decoupling capacitance is required while FD RL predicts 115pF. By modeling the frequency dependence, more than 15% area can be saved. This effect can be significant since the increasing need for power supply stability has led to rapidly rising area costs of decoupling capacitors; the area required for sufficient decoupling capacitance in microprocessors can be comparable to that of the entire microprocessor core [13]. Thus, correct consideration of FD RL can help alleviate such concerns while providing sufficient power supply stability.

4. Impact on RF Inductor Design

In silicon-based radio-frequency (RF) ICs, on-chip spiral inductors are widely used due to their low cost and ease of process integration. On the other hand, in current technology, on-chip spiral inductor suffers from the significant energy loss in the conductive silicon substrate that leads to poor quality factor (Q).

The quality factor is usually defined as:

$$ Q = -\frac{\operatorname{Im}(Y_{ii})}{\operatorname{Re}(Y_{ii})} $$

(3)

To enhance the Q value, considering that at low frequency, Q can be approximated as:

$$ Q \approx \frac{\omega L}{R} $$

(4)

designers prefer to use wide metal lines to reduce R. However, since RF operating frequencies are usually in the multiple GHz regime, the strong frequency dependence of R significantly degrades the peak Q value and is critical for inductor performance prediction. This necessity is demonstrated in a single-turn inductor structure design, as shown in Fig. 9. To enable efficient simulation and quality factor extraction, we adopt the single-Π circuit model of the inductor as shown in Fig. 10 [14]. In the conventional single-Π structure, DC RL is used to represent the metal line. We replace these with FD RL to capture the high frequency characteristics.

Fig. 11 shows the simulation results. Compared with the computationally expensive full PEEC model, the ladder FD RL model accurately predicts Q over a wide range of frequencies and significantly improves the simulation efficiency. DC RL overestimates the peak Q by up to 69%, which is unacceptable in RF applications [15]. In conclusion, FD RL is necessary for correct RF spiral inductor design and optimization. As the ladder model is physical and scalable, it facilitates fast and accurate inductor performance analysis, and is capable of supporting wide-band RF design [3].
5. Summary

For the first time, the design impact of frequency-dependent impedance of on-chip interconnect is examined by using a compact ladder circuit representation. The ladder model accurately captures FD phenomena and is implementable in SPICE as it contains only frequency-independent parameters. In digital design, while DC RL is sufficient for timing analysis, FD RL is shown to be crucial for correct analysis of signal integrity and shield line insertion. Consideration of FD RL also leads to more accurate estimation of power supply stability. Finally, for RF inductor design and performance analysis, an accurate FD RL model is very important as well.

References