Design and scalability analysis of optical phased-array $1 \times N$ switch on planar lightwave circuit

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Abstract: We derive explicit design rules of optical phased-array planar $1 \times N$ switch to achieve small insertion loss, large extinction ratio, and non-dispersive waveguide structure required for wavelength-independent broadband operation. The minimum number of phase shifters and slab lengths were studied as a function of $N$ and the optimized array shape was derived to minimize the optical path length. We show that the length depends nonlinearly on $N$, and may become significantly shorter compared with that of a tree-structured switch under certain conditions.

Keywords: optical switch, optical packet switching, photonic integrated circuit, optical interconnects, planar lightwave circuit

Classification: Photonics devices, circuits, and systems

References

1 Introduction

Large-scale $1 \times N$ switch with fast reconfiguration time and broad optical bandwidth will be the essential building block for constructing future photonic switching routers, optical buffers, and high-speed optical interconnects [1]. In particular, integrated electro-optic switches on planar lightwave circuit based on III-V semiconductor (e.g., InP, GaAs) [2, 3, 4] or ferroelectric materials (e.g., LiNbO$_3$, ((Pb,La)(Zr,Ti)O$_3$) [5, 6] are attractive owing to small footprints, fast response time below nanosecond, and low power consumption. Most conventional planar $1 \times N$ switches have employed either the broadcast-and-select scheme [2] or cascade of $1 \times 2$ switches in tree or crossbar architecture [3, 4, 5, 6]. However, while the former must cope with problems of nonlinear crosstalks inside semiconductor-optical-amplifier gate switches as well as signal-to-noise ratio degradation for large $N$, the latter suffers from increasing switch length and optical insertion loss, which grow at log $N$ or faster. Recently, novel type of integrated $1 \times N$ switch based on optical phased array has been demonstrated by several groups [7, 8, 9]. Since $1 \times N$ switching is achieved in a simple structure using a single phase modulating stage, the scheme is expected to have potential advantage in terms of device length and insertion loss when scaling to large $N$. However, the design theory of phased-array switch has not been studied in detail to our knowledge and its scalability is left unclear.

In this Letter, we derive explicit design procedure to realize a compact
optical phased-array $1 \times N$ switch with wavelength-independent structure and investigate its scalability against the increase of output port count $N$. We show that the required number of phase shifters scales linearly with $N$. The optical path length, on the other hand, grows nonlinearly with $N$, and may become significantly shorter compared with that of conventional tree-structured switches under realistic conditions.

2 Design and Scalability Analysis

The structure of an optical-phased-array $1 \times N$ switch is shown in Fig. 1 (a). Input light is dispersed spatially at Slab 1 and directed to arrayed phase shifters, where the optical phase is controlled individually. By changing the phase linearly (with modulo $2\pi$) across the array, we can dynamically control the focusing position of light at Slab 2. A strictly non-blocking $N \times N$ switch can be constructed by using $2N$ of these $1 \times N$ switches in Spanke architecture [10].

![Fig. 1. Definition of parameters used in the calculation.](image)

2.1 Derivation of Required Number of Phase Shifters

In order to achieve high extinction ratio and low insertion loss, we need to have sufficient number of phase shifters. We first derive the minimum number of arrayed waveguides $M$ required for a given output port count $N$. Ignoring the propagation loss and excess losses at the phase shifters, the amplitude transmittance to the $n$th output port is expressed as

$$T_n = \sum_{m=1}^{M} \eta(0, \alpha_m) \cdot \eta(\alpha_m, \alpha_n) \cdot \exp(i\phi_m).$$

As shown in Fig. 1 (a), $\alpha_m$ and $\alpha_n$ are the angular coordinates of the phased-array port and output port, respectively and $\phi_m$ is the phase shift applied at the $m$th phase shifter. The function $\eta(\alpha_1, \alpha_2)$ denotes the transmittance of
the slab coupler from the input port angle $\alpha_1$ to the output port angle $\alpha_2$, and expressed under the Fraunhofer approximation as

$$\eta(\alpha_1, \alpha_2) = \sqrt{\frac{k}{2\pi f}} \cdot \int u_1(x) \exp(jkx\alpha_2)dx \cdot \int u_2(x) \exp(jkx\alpha_1)dx \cdot \exp(-jkf\alpha_1\alpha_2), \quad (2)$$

where $k$ is the propagation constant at the slab region, $f$ is the slab length, and $u_1(x)$ and $u_2(x)$ are the mode-field profiles of the radiating and receiving waveguides, respectively [11].

As an example case of interest, we consider an InP switch with the waveguide width of $2 \mu m$, array pitch of $2.5 \mu m$, and effective indices of 3.3 (core) and 3.2 (clad) at the entrance and exit of the slab couplers. By calculating Eq. (1) for various combinations of $N$, $M$, and $f$, we derive the minimum $M$ that is required to realize given switching property. Fig. 2(a) shows the required $M$ to achieve the insertion loss lower than 5 dB and extinction ratio higher than 30 dB for all the output ports. Optimized values of $f$ are also plotted for respective cases. We see that both $M$ and $f$ scale linearly with $N$, which is a general consequence of the fact that the switch relies on linear Fourier optics. The rates are $M \approx N \times 1.6$ and $f \approx N \times 14 \mu m$ for this particular condition. Fig. 2(b) shows the calculated switching characteristics for $N = 16$ ($M = 23$, $f = 200 \mu m$) and $N = 32$ ($M = 44$, $f = 405 \mu m$), indicating that essentially identical characteristics are obtained by scaling $M$.
and $f$ with $N$.

In practice, we should also consider the tolerance against phase errors, which inevitably exist in real devices. On the other hand, further reduction of $M$ would be possible if we adopt appropriate apodization and tapering of the arrayed waveguide structures. These issues are out of scope of this paper and will be discussed in future.

2.2 Optimization of Switch Structure

We next derive the optimized switch shape for the given values of $N$, $M$, and $f$ that minimizes the total light-propagating distance within the switch. Such optimization is relevant since the optical path length directly reflects the device footprint and insertion loss, which is especially important for III-V semiconductor switches, having inevitably large propagation loss.

In order to achieve wavelength-independent operation, we need to design the array shape anti-symmetric as shown in Fig. 1 (a), such that optical path lengths are constant among all arrayed waveguides. This condition can be expressed as

$$\Delta L \equiv L_{m+1} - L_m = \text{const.}, \quad (m = 1, \ldots, M - 1) \quad (3)$$

where $L_m$ denotes the path length of the $m$th waveguide from the Slab 1 output to the phase shifter input and written as

$$L_m = S_m + R_m (\theta + \alpha_m) + S'_m, \quad (4)$$

with the parameters defined in Fig. 1 (b). By attaching the same structure shown in Fig. 1 (b) with 180-degree rotation and phase shifters in-between, we can construct the entire array with constant path length. Two additional conditions are

$$W_m = (f + S_m) \cos(\theta + \alpha_m) + R_m \sin(\theta + \alpha_m) = \text{const.}, \quad (5)$$

$$\Delta D_m \equiv D_{m+1} - D_m = \text{const.}, \quad (6)$$

where

$$D_m = (f + S_m) \sin(\theta + \alpha_m) + R_m [1 - \cos(\theta + \alpha_m)] \quad (7)$$

Eq. (6) insures equal spacing between adjacent phase shifters, where $\Delta D$ is determined by the minimum separation to achieve electric isolation. While Eqs. (3), (5), and (6) provide $(3M - 3)$ conditions, we have $(3M + 2)$ of independent variables \{R_m, S_m, S'_m (m = 1, \ldots, M), \theta, \Delta L\} to be solved. We therefore have five degree of freedom in determining the array shape, within which we derive the optimized condition to give the minimum total path length. Finally, conditions similar to Eqs. (5) and (6) are imposed in designing the waveguide structure at the Slab 2 output.

We assume $\Delta D = 15 \mu$m and the output port separation to be $30 \mu$m, corresponding to the pitch of a recently reported fiber array [12]. The minimum bending-radius is set to $100 \mu$m, which is feasible with double-etching
Fig. 3. Scalability of optical path length for phased-array and tree switches.

(a) Total optical path length within the phased-array (dots) and tree (circle) switches calculated as functions of $N$. The length of phase modulator (or single 1×2 switch) $L_{mod}$ is 0.5, 1, 2, and 4 mm for respective plots.

(b) Optimized switch structures of phased-array and tree switches for increasing $N (L_{mod} = 2$ mm).

Fig. 3. Scalability of optical path length for phased-array and tree switches.
While we have focused on the geometrical path length within the device, superiority of phased-array switch is enhanced if we also take into account the excess losses at the modulators, which is independent on $N$ for a phased-array switch. On the other hand, we should also consider other important factors, such as insertion loss, crosstalk accumulation, power consumption, and so on, to conduct thorough evaluation of scalability. These factors, however, depend significantly on the material as well as modulation scheme we employ, and will be discussed elsewhere.

3 Conclusions

We have derived an explicit design procedure to realize a compact optical phased-array $1 \times N$ switch with wavelength-independent structure. The minimum number of phase shifters and slab lengths were studied as a function of output port count $N$ and the optimized array shape was derived to minimize the optical path length. Since the number of modulating stage does not increase with $N$, the increase in optical length remains relatively slow for a phased-array switch at wide ranges of $N$ under practical conditions. This feature may offer potential advantage over conventional tree or cross-bar switches, particularly for reverse-biased semiconductor or ferroelectric switches, which require relatively long sections for modulation.