Abstract—We present 60GHz OFDM hardware demonstrators developed so far and outline design considerations for future developments. OFDM schemes have been developed to combat multi-path interferences in indoor wireless environments and further optimized for multi-gigabit data transmission in 60GHz-band. RF and IF analogues front-ends (AFEs) have been developed with high-speed SiGe BiCMOS technologies. Future developments on AFE are mainly devoted to one-chip integration of RF and IF components based on a sliding IF architecture. We have already achieved wireless transmission of about 1Gbps in an OFDM demonstrator, which will be continuously upgraded and optimized for higher data transmission with better link adaptability.

I. INTRODUCTION

For a long time, 60GHz-bands have been of great interest due to the availability of several GHz of unlicensed spectrum. Nevertheless, even 5 years ago, there had been few trials to use them in consumer applications due to bulky and expensive 60GHz RF components attributed to III-V semiconductor technologies with high-cost and low-level integration. Recently, silicon-based high-speed circuit technologies have made tremendous progress, and eventually it becomes now possible to make and integrate most of 60GHz RF components with silicon-based semiconductor processes. The availability of these small-size and low-cost silicon-based 60GHz chipsets has stimulated consumer electronics industries to use 60GHz wireless systems for many consumer applications [1].

There is no doubt that high data rate wireless personal area networks (WPAN) would be the first consumer application successfully employing 60GHz wireless systems because they require multi-gigabit wireless transmission but shorter range below 10m. Wireless HDTV video transmission and wireless file-download applications are good examples to show these social demands and trends. To come up with them, there have been several vigorous activities to develop a standard, for instance, IEEE 802.15.3c, Wireless HD, and ECMA.

Besides them, 60GHz wireless systems are now finding new application areas, representatively, gigabit wireless local area networks (WLAN). The IEEE 802.11 VHT (very high throughput) study group which is now investigating next generation of 802.11n standard begins to consider a 60GHz wireless system as one of the candidates for multi-gigabit WLAN. It should be noted that the 60GHz system requirements would be much more stringent than those of WPANs because WLANs have to provide much wider coverage and less susceptibility to multi-path interference.

We have developed 60GHz wireless systems mainly for these multi-gigabit WLAN as well as video distribution applications. For our system approach, orthogonal frequency division multiplexing (OFDM) has been preferred to single carrier modulation since it provides not only higher spectral efficiency but also stronger robustness in multi-path wireless channel environments. However, it requires the 60GHz RF front-end to possess both higher linearity of the power amplifier and lower phase noise of the local oscillators. Moreover, WLAN systems are required to radiate higher transmit power in order to achieve wider coverage compared with WPANs. For these reasons, SiGe BiCMOS technology is believed to be the most promising solution from the viewpoint of cost and performance, therefore it has been used for our 60GHz analogue RF front-ends.

This paper introduces our developed 60GHz OFDM hardware demonstrator and describes design considerations for future development. Section II is dedicated to the introduction to each part of the developed demonstrator, baseband OFDM physical layers, analogue front-ends and wireless demonstration results. In Section III, we briefly describe our design approaches for next-generation 60GHz OFDM demonstrators with primary emphasis on analogue front-ends. Finally, this paper ends with summary and conclusions.

II. DEVELOPED 60GHz OFDM DEMONSTRATOR

The architecture of developed 60GHz OFDM demonstrator is schematically illustrated in Fig. 1. It consists of 60GHz
analogue front-ends, 5GHz IF blocks and OFDM baseband processors. In this demonstrator, we employed a super-heterodyne transceiver with 5GHz IF because less than 1GHz bandwidth from 60.5 to 61.5GHz was used for 60GHz transmission [3]. The RF and IF transceiver chipsets were fabricated in 0.25μm SiGe:C BiCMOS technologies with 1μm of 200GHz. The baseband OFDM processor hardware was realized with high-speed FPGA board in conjunction with DAC/ADC add-on modules.

A. OFDM baseband parameters

Table 1 summarizes the key parameters for baseband OFDM processors which have been used for our 60GHz demonstrator. Basically, these OFDM schemes have been derived from the IEEE 802.11a 5GHz-band WLAN standard. They have two kinds of transmission schemes, a narrowband scheme using a bandwidth of 330MHz and a wideband scheme using 650MHz. Each scheme supports different transmission rates with modulations from BPSK to 64-QAM and standard convolutional coding with optional puncturing. The cyclic prefix of 160ns was decided with consideration of maximum tolerable delay spread in 60GHz wireless indoor channel [3]. In our OFDM demonstrator, we employed a novel preamble structure composed of eleven OFDM symbols for better synchronization and more accurate channel estimation [4].

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT bandwidth</td>
<td>400MHz or 800MHz</td>
</tr>
<tr>
<td>FFT size</td>
<td>256 or 512 points</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>330MHz or 650MHz</td>
</tr>
<tr>
<td>Cyclic prefix time</td>
<td>160 ns</td>
</tr>
<tr>
<td>Total symbol time</td>
<td>800 ns</td>
</tr>
<tr>
<td>Subcarrier spacing</td>
<td>1.5625MHz</td>
</tr>
<tr>
<td>Number of data subcarrier</td>
<td>192 or 384</td>
</tr>
<tr>
<td>Number of pilot subcarrier</td>
<td>16 or 30</td>
</tr>
<tr>
<td>Forward Error Correction</td>
<td>Convolutional coding</td>
</tr>
<tr>
<td>FEC decoding algorithm</td>
<td>Viterbi decoding</td>
</tr>
</tbody>
</table>

B. 60GHz RF front-ends

Fig. 2-(A) schematically shows the developed analogue receiver front-end. It should be noted that only three active components, a low-noise amplifier (LNA), a down-conversion mixer and a 56GHz phase-locked loop (PLL) are integrated into a 60GHz receiver front-end chipset without any passive component, such as RF bandpass filter. It is well-known that one-chip integration with such passive component is still a challenging task in silicon-based integrated circuits because of the high lossy silicon substrate. As an alternative solution, we optimized the LNA to have RF bandpass filtering characteristics by incorporating small inductive microstrip lines and capacitive components [5]. The measured and simulated gain performances of the designed LNA are compared in Fig. 3-(A). It has the measured gain of about 20dB at the centre frequency of 60GHz and the 3dB bandwidth ranging from 56 to 65GHz. We can see that the developed LNA well satisfies the requirement of a RF bandpass filter since the achieved 3dB-bandwidth well covers the 57-64GHz unlicensed frequency bands that the United States and South Korea have opened.

Half of a Gilbert cell was used as a core circuit of the frequency down-conversion mixer. Since this topology has a single-ended RF input and a differential IF output, it is useful to remove the need for any balun or transformer in frequency down-converter. Two- emitter followers were used as an output buffer stage and a shunt inductor of 1.8mH was used at the IF output in order to match to 100 Ohms differential impedance. This inductor makes IF output circuitry to be equivalent to a second-order high-pass filter (HPF). Eventually, the frequency response of IF output port becomes mixture of this HPF characteristic with low-pass filtering behaviours of transistors. This feature can be seen in Fig.3-(B) which shows the measured and simulated conversion gain of the down-conversion mixer when the LO frequency is fixed to 55GHz. The simulated noise figures are 6 and 14dB for the LNA and the mixer, respectively [5].
An RF PLL has been regarded as one of the critical components that significantly affect system performance of OFDM signal transmission. In our RF analogue front-ends, a 56GHz PLL is integrated in both receiver and transmitter. It consists of a voltage-controlled oscillator (VCO) with a differential output, a frequency divider, a charge pump and a loop filter. The 1:512 divider is realized with nine consecutive 1:2 divider stages. A programmable RF PLL would bring on extra components that significantly affect system performance of OFDM signal transmission. In our RF analogue front-ends, a power amplifier is integrated with the PLL in the IF stage. The detailed design of a 56GHz PLL we employed in RF front-ends can be found in [6]. The measurement shows that the PLL has the bandwidth of 4.5MHz and spur level below -55dBc. It consumes 80mA from 3V supply and 60mA from 2.6V. The VCO phase noise at 1MHz offset from the carrier is -90dBc/Hz. Fig. 4-(a) shows the photograph of the 60GHz receiver front-end with LNA, a down-conversion mixer and a 56GHz PLL being integrated into one chip. Fig. 4-(b) shows the board design for 60GHz receiver front-end.

The developed RF transmitter front-end consists of a frequency up-conversion mixer, a preamplifier, an image rejection filter and a power amplifier as shown in Fig. 2-(B). This frequency up-conversion mixer is based on a Gilbert-cell mixer and optimized for high linearity and output power. The simulation results show the output 1dB compression point (1dBCP) of -15dBm. In order to make this output signal strong enough to drive the input of the following power amplifier, a preamplifier with 18dB gain is employed. It is also used in order to compensate high insertion loss caused by the image-rejection filter [6].

The power amplifier features a multi-stage differential cascode topology. One cascode stage provides high gain of around 11dB with IHP SiGe BiCMOS technology, and therefore three cascade stages were employed to get more than 25dB amplification in the power amplifier. It was designed fully differentially for better common-mode noise rejection and robustness. Fig. 5-(A) shows the measured and simulated S-parameters for the power amplifier. Other measurements show the single-ended output 1dBCP of 10.5dBm at 61GHz and saturation power of 14.9dBm. The photograph of 60GHz transmitter chipset, where a power amplifier is integrated with the other RF components, is shown in Fig. 5-(B).

C. 5GHz I/Q modulator/demodulator

After down-conversion from the 60GHz-band into the 5GHz-band with the 60GHz receiver front-end, the IF signals are demodulated with a 5GHz-band I/Q demodulator. As illustrated in Fig.2-(A), it consists of an IF variable gain amplifier (VGA), a wideband quadrature PLL, frequency downconversion mixers, two baseband VGAs, and low-pass filters with tunable cut-off frequency. A 5GHz-band I/Q modulator has similar components except that no baseband VGA is employed.

As previously mentioned, two channels from 60.5GHz to 61.5GHz should be supported in this demonstrator, therefore the PLL in the IF stage was designed to provide 4.75GHz and 5.25GHz I/Q signals. To generate them, a 10GHz VCO in conjunction with bipolar divide-by-two circuit is used. With the help of large internal swing, the improved phase-noise performance of a MOS-VCO was achieved while keeping the low power consumption of SiGe frequency dividers. This I/Q PLL consumes 57mA at 2.5V supply voltage.

A modulator employs an IF VGA cell which is realized as a transadmittance stage followed by a transimpedance stage with internal AC coupling. In case of a demodulator, two cascaded VGA cells are used as an IF VGA stage. The detailed description of the design methodology of I/Q modulator/demodulator can be found in [8]. We observed that the spurious level for the modulator and demodulator was as low as -73dBc despite the large PLL tuning range of approximately 1GHz. The phase noise at 1MHz offset is -112dBc/Hz for modulator/demodulator. Fig. 6 shows the single-tone signal output power of the modulator as a function of input baseband signal amplitudes.
of I/Q baseband signal amplitude. The gain provided by VGA is controlled by the external bias signal of \( V_g \). The output 1dBCP is -7dBm at the maximum gain of modulator. OFDM signal modulation was also tested and the output spectrum observed with a spectrum analyser is shown in Fig. 8.

Fig. 7. Measured OFDM spectrum at the output of 5GHz I/Q modulator

D. Demonstration of OFDM signal transmission

The complete OFDM baseband transmitter was realized in hardware on FPGA basis. An OFDM baseband receiver is currently being implemented on an FPGA as well and its algorithm was realized in software with MATLAB. The first system demonstration was tried with a 60GHz receiver front-end which was not yet optimized to have RF filtering function [2]. In this time, a power amplifier was not integrated. Maximum achieved data-rate was 960Mb/s using Agilent IQ signal generator and analyser with wideband system parameters for 16QAM signals with \( \frac{1}{2} \) coding-rate. Detailed results on demonstrations can be seen in [2]. 64QAM signals with \( \frac{3}{4} \) coding-rate were also successfully transmitted with narrowband system parameters corresponding to a 1.08Gbps transmission. Fig. 8 shows the output constellation diagram of transmitted 64QAM OFDM signals and estimated SNR for individual data subcarriers. Subsequent field trials were performed with an integrated power amplifier. Fig. 9-(A) shows the measurement setup in a lap at IHP. Error-free transmission of QPSK signals with \( \frac{3}{4} \) coding-rate was successfully demonstrated over 5m transmission, which corresponds to 360Mbps data-rate. The constellation diagram of the received signals is shown in Fig. 9-(B).

Fig. 8. (A) Constellation of 3/4-coding 64QAM OFDM signals (B) Signal-to-noise ratio for individual data subcarriers

Fig. 9. (A) experimental setup of 60GHz wireless transmission (B) constellation of 3/4-coding QPSK OFDM signals after 5m transmission

III. DESIGN CONSIDERATIONS FOR NEXT-GEN. 60GHZ SYSTEM

A. Analogue front-end based on sliding IF

For the next-generation of 60GHz demonstrators, we decided to use a sliding IF architecture since it has the potential to eliminate the use of an additional PLL for IF conversion. This results in less power consumption and less complexity while maintaining the advantages of super-heterodyne transceiver. A single 48GHz-band PLL extended with a static \( 1/4 \) frequency divider, also generates the 12GHz-heterodyne transceiver. A single 48GHz-band PLL extended with a static 1/4 frequency divider, also generates the 12GHz-heterodyne transceiver. This results in less power consumption and less complexity while maintaining the advantages of super-heterodyne architecture. Fig. 10 shows the schematic diagram for the sliding-IF receiver.

Fig. 10. Sliding IF architecture for next-generation analogue front-end

We believe that supporting two modes, narrowband and wideband schemes, is still very useful for future WLAN applications because it provides high flexibility of serviceable data rate according to numbers of subscribers. In case of wideband schemes, the proposed centre frequencies are the same as in the IEEE 802.15.3c draft standard [9]: 58.32GHz, 60.48GHz, 62.64GHz and 64.80GHz in order to provide compatibility to IEEE 802.15.3c devices. In our system approach, one wideband channel could be divided into several narrowband channels as long as the centre frequencies of the narrowband channels can be generated with the same PLL architecture.

A new 48GHz-band PLL has been designed to generate 4 different centre frequencies as described above. Since the channel spacing of 2160MHz is an integer multiple of 9.6MHz, a low-cost 19.2MHz crystal oscillator which has
been widely used for CDMA applications, followed by 1:2 frequency divider can be used as a reference clock as shown in Fig. 11. The phase-frequency detector (PFD) compares the 9.6MHz signal from the divided VCO frequency with the divided crystal frequency. The PFD output is connected to a charge pump (CP) and a low-pass filter (LPF) which is connected to the VCO tuning input. Detailed analysis and design of this PLL will be available in [10].

**Fig. 11. 48GHz-band PLL architecture providing the compatibility to IEEE 802.15.3c channelization plan**

Although we did not use any channel selection filter in the previous demonstrator, the future one will be equipped with an IF channel selection filter before the IF VGA stage because we cannot avoid adjacent channel interferences in indoor WLAN application scenarios. This also facilitates to have good co-existence performance with legacy IEEE 802.15.3c WPAN devices. However, the realization of a channel selection filter becomes more difficult in sliding IF architectures since the IF is not fixed. One option is to use a tunable bandpass filter. However, integration of small-size IF bandpass filter with high quality factor is a still challenging task. Therefore, for simplicity, we first use a fixed IF channel selection filter with wider bandwidth than one channel, although it cannot perfectly eliminate adjacent channel signals. This problem can be overcome by rejecting residual adjacent channel signals with a baseband LPF. The IF for the new designed PLL configuration varies from 11.664GHz to 12.96GHz. According to the proposals in 802.15.3c, the 3dB bandwidth of signals is 1.728GHz. Therefore, required 3dB bandwidth of the fixed channel selection filter is 3.024GHz as shown in Fig. 12. We also see that maximum interference in the pass-band of channel selection filter does not exceed 1/3 bandwidth even in the worst case where the 1st channel is used with adjacent channel in the 2nd channel.

**Fig. 12 Illustration for required 3dB bandwidth of IF channel selection filter**

### B. OFDM baseband parameters

We are currently developing new OFDM schemes for both the wideband and narrowband schemes, which support multi-gigabit data transmission. The parameters have not yet been finally fixed due to the lack of channel models in our application scenarios. Hopefully, they will be presented with other physical layer parameters in conference site.

**ACKNOWLEDGMENT**

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### IV. CONCLUSIONS

We have presented Si-based 60GHz OFDM hardware demonstrators capable of transmitting 1Gbps data rate using OFDM modulation. Design considerations for future development were also described. 60GHz RF front-ends and 5GHz I/Q modulator/demodulators were developed using a SiGe BiCMOS technology. Using them, wireless 1Gbps OFDM signal transmission was successfully demonstrated. In future developments, these two components will be integrated into one-chip with sliding IF architecture having a newly designed PLL generating both 48GHz RF and 12GHz IF signals. To reduce adjacent channel interference, an IF channel selection filter will be added. The target data rate of the new version is higher than 2Gbps while allowing for 10m point-to-multipoint links. To achieve this goal in the next generation hardware demonstrator, we will continue to improve physical layer and MAC layer schemes. Future work on analog front-end will be focusing on the realization of higher integration without sacrificing chipset cost.

**REFERENCES**


[9] IEEE 802.15.3c millimeter-wave WPAN task group, (http://iee802.org/15/pub/TPGC3c.html)