Calibration and Self-Test of RF Transceivers

Yaning Zou‡, Christian Münker†, Rainer Stuhlberger‡, and Mikko Valkama‡

*Tampere University of Technology, Finland, mikko.e.valkama@tut.fi
†Munich University of Applied Sciences, Germany
‡DICE GmbH & Co KG, Linz, Austria

Abstract—In the last few years cellular market well exceeded 1.3B cellular mobile devices shipped per year. The ongoing economic-driven shrink in technology towards nanoscale CMOS enables increased functionality in even smaller silicon area, however, technology effects including process variation, variability, temperature effects, flicker noise etc. put stringent challenges on the design and have significant impact on the production yield. Due to the huge volume yield, testing and Automated Test Equipment (ATE) have become a major cost factor in RF production. At the same time integration level and complexity of RF transceivers and SoCs have increased due to huge diversity of mobile communication standards ranging from 2G/3G to 4G, WLAN, BT, and GPS. RF devices are no longer purely RF devices. They integrate RF, analog and digital functions, all working together enabling the device to test and calibrate functions autonomously. This paper summarizes the key developments and trends in RF-BIST, with particular attention to improvements in testing and calibration of PLL loop-gain, second order modulation, and I/Q impairments.

I. INTRODUCTION

Currently, several 2nd- and 3rd-generation digital wireless standards, such as GSM, CDMA2000 and UMTS exist in different parts of the world. Furthermore, new 3.9th and 4th-generation systems are emerging in the coming years. Instead of converging into a single worldwide system, it seems that various different standards will co-exist in the future. The main reason for a multitude of standards, enabled by the introduction of ever-more sophisticated digital data transmission and networking techniques, is the emergence of different wireless services and applications, requiring different data rates and different service quality for the radio interface [1]. This, in turn, calls for flexibility and reconfigurability in future wireless terminals to make these various standards and services accessible using a single user interface and a single low-cost and power-efficient hardware platform.

This paper discusses the design of a novel Digital Front-End (DFE)-based adaptive wireless receiver for multi-mode (GSM/EDGE, CDMA2000, UMTS, Galileo, LTE) operation by sharing digital signal-processing stages for all operation modes and adapting them for minimum power consumption with respect to the channel selection requirements, and integration of sophisticated signal processing for mitigation of analog RF non-idealities. Based on a previous investigations [2]–[5] in which some of the aspects of multi-mode receivers and the enhancement of RF receivers with a DFE have been presented, the current work extends this concept by adding adaptivity not only to support multiple standards but also to reduce power consumption, second-order intermodulation distortion, and I/Q imbalances by sophisticated DSP.

II. IMPACT OF RF IMPAIRMENTS

The three main RF bandwidths, 5 MHz, 10 MHz, and 20 MHz of LTE were then investigated. The randomly generated bits are modulated and after serial/parallel conversion (S/P). Because not all subcarriers are occupied with data, the remaining subcarriers including the DC carrier are set to zero (Zero pad). After IFFT-processing and parallel/serial conversion (P/S), the CP is included depending if a short or long CP is used (Add CP). This signal passes the radio channel which is modeled as an AWGN channel. The data are then degraded by the models of the considered RF impairments as described in [6]. The time synchronization is carried out statically because all chain delays are known. Before the FFT processing, the CP is removed, then the zeros from the unused subcarriers, and finally the reference symbols. After demodulation, the Bit Error Rate (BER) is calculated for the different RF investigations.

The following simulation results were performed for the 3 main RF bandwidths, 5 MHz, 10 MHz, and 20 MHz, and for the modulation schemes QPSK, 16-QAM, and 64-QAM. No equalization is carried out because only an AWGN-channel is used for the following investigations. The signal power is constant at -25 dBm/5 MHz for all simulations performed. This power level could be a possible value for the maximum input test case similar to UMTS [7]. The number of Physical Resource Block (PRB) is 12. To simulate a full loaded system, all PRBs are loaded with data from one user. Furthermore all simulations are performed with ideal floating-point models. With this arrangement, it is possible to investigate only the effects of the RF impairments without any other disturbances.

Figures II display the raw BER degradations for different
values of gain imbalances for a bit-error probability of $P_b = 10^{-4}$. The imbalance is considered static for all simulations; therefore, the performance is independent of the bandwidth used. Higher modulation schemes are more sensitive to both amplitude and phase mismatch than QPSK modulation is. Due to the fact that for LTE no equalization is implemented for these simulations, the performance degradation especially for 64-QAM is pretty high even for small mismatches. This is in contrast to HSDPA, where the LMMSE equalizer is able to almost completely remove the static amplitude and phase mismatches. To achieve almost no degradation in terms of raw BER, the gain imbalance has to be less than 0.2 dB and the phase imbalance less than $\circ$, the performance degradation in terms of raw BER for QPSK modulation and 16-QAM are in a tolerable range. Special attention has to be paid to 64-QAM where the performance degradation is in a critical range and some kind of I/Q impairment correction has to be expected; this topic is addressed in more detail in Section V.

III. SPECTRAL PLL-BUILT-IN SELF-TEST

A BIST approach for autonomous, specification oriented test of RF PLLs in SOCs which are especially hard to test because they are completely embedded. Spectral parameters like frequency response or the level of spurious sidebands have to be guaranteed for wireless applications. The focus of this paper is therefore compact on-chip spectral analysis without disturbing critical RF paths. The BIST blocks have been integrated on an RF transmitter utilizing a sigma-delta modulated fractional-N PLL (Fig. III). This architecture is commonly used for highly integrated RF CMOS transceivers because it is well adapted to CMOS technologies [1] and allows digital data modulation. The BIST functionality is achieved using robust, digital signal processing blocks with little area penalty due to the high integration density in nanoscale CMOS technology.

A. Analysis

On-chip analysis of the modulated PLL signal requires demodulating and digitizing the RF signal which is a narrow-band signal with rail-to-rail amplitude in the device-under-test. A standard down-conversion architecture requires large area, precision analog circuitry like a mixer and a high resolution ADC. Instead, a first order sigma-delta frequency modulator (SDFM) is used which only consists of a high-speed dualmodulus divider (DMD) and a D-flip-flop and delivers a sigma-delta modulated oversampled approximation of the frequency modulating signal.

Instead of implementing a full FFT, a narrowband frequency analysis is performed to estimate the amplitude of frequency components. First, the FSDM output bit stream with the sampling rate $f_S = 26$ MHz is decimated in a second order CIC filter by a factor of $R = 32$. Its magnitude transfer function is given by (1).

$$\frac{|H(f)|}{\sin (N\pi f/f_s)} \approx R^N(\text{sinc}f)^N$$ for $f \ll 1$ (1)

The band of interest is selected with a narrow, programmable bandpass. Here, the damping factor $k_{BW} > 0$ determines the bandwidth, it is implemented as a fixed bitshift. A main advantage of this filter type is its robustness against coefficient truncation: $a = b = k_f$ set the center frequency $f_c$ with only 9 bits wordlength which gives a frequency resolution of 300 Hz without compromising noise performance or stability. Another advantage is that the resonance frequency $f_c$ is set with a single parameter $k_f$ (2).

$$f_c = \frac{f_S R_1}{\pi} \arcsin \frac{k_f}{2} \approx \frac{k_f f_S R_1}{2 \pi}$$ (2)

IV. IM2 CANCELLATION

Modern RF CMOS communication transceivers are complex mixed-signal systems incorporating not only RF/analog functions but also A/D and D/A converters as well as sophisticated DSP blocks. Because they contain digital logic and since digital circuits are inherently free of mismatches, such transceivers are well suited for performing the IP2 auto-calibration task, which comprises on-chip second-order distortion detection and control of the analog mismatch-tuning block.

An example of the IP2 improvement system is shown in Fig. 3. It can be regarded as a mixed-signal embodiment of the adaptive interference cancellation architecture [8]. A mixer equipped with an IP2 tuner downconverts the RF input signal to the differential IF output signal. As a by-product of active device second-order nonlinearities, the common-mode output signal contains second-order distortion [9], which can be detected and correlated with the differential output signal in order to estimate the differential second-order distortion.
The correlation is carried out by a digital block implementing an adaptive algorithm. The IP2 tuner is adjusted in order to minimize the output differential distortion.

Although an additional reference signal path is required, the dynamic range requirements for an auxiliary A/D converter are significantly relaxed compared to compensation schemes. In fact, even a one-bit A/D converter is sufficient, enabling usage of a simple sign-sign least-mean square (SS-LMS) adaptive algorithm. The SS-LMS coefficient update equation has the following form:

\[ w[k + 1] = w[k] - \text{sgn}(e[k]) \text{sgn}(\text{ref}[k]). \]

where \( w[k] \) is the digital tuning code of the IP2 tuner.

The adaptive IP2 calibration approach is a classical trade-off between convergence speed and steady-state behavior, which in this case means achievable IMD2 suppression. Additionally, statistics of the processed signals influence the convergence time. As an illustration, Fig. 4 compares algorithm learning curves for two distinct interferers. The first one is a QPSK modulated signal fed continuously to the mixer input. Another one is a GMSK modulated interferer transmitted in bursts as a single slot of the frame as defined in the GSM standard. The convergence speed is much faster for the QPSK interferer than for the TDMA burst interferer. Generally, interferers having poorly correlated envelopes will result in faster convergence than signals with well-correlated envelopes.

The adaptive IP2 calibration technique has several limitations. First, due to dependence of mixer mismatches on the RF interferer carrier frequency, calibration algorithm converges in general only with a single AM-modulated interferer. Fortunately, in practice, this restriction is true, e.g. in UMTS transceivers, in which transmitter leakage to the receiver input is by far the dominant AM interferer. Another limitation relates to the convergence speed of a given adaptive algorithm. To achieve the required steady-state performance, convergence speed cannot be increased arbitrarily since controlling the step size affects both convergence speed and the steady-state mean-squared error. This means that if the mixer operating conditions change abruptly (e.g. an RF interferer changes its carrier frequency due to a frequency-hopping scheme), linearity specifications might not be met for a significant time interval required to adapt the IP2 tuner to the new conditions.

To achieve faster convergence, more sophisticated adaptive algorithms such as RLS could be used [8], but at the expense of a substantial increase in hardware complexity. Finally, mismatches present within the mixer cause not only conversion of common mode signals to differential mode signals but also differential mode signals to common mode signals. This might cause problems at high levels of the wanted signal, as the calibration loop might try to lock itself according to the wanted signal detected by the common mode sensing circuitry instead of the distortion signal.

The feasibility of the adaptive IP2 calibration system has been demonstrated in [10]. AM modulated out-of-band interferer was fed to the input of the IQ downconverter, along with a weak in-band sine signal. After demodulation and baseband filtering, the interferer level is negligible but the distortion it generates degrades Signal to Noise and Distortion Ratio (SNDR) considerably. The plots demonstrate reduction of distortion in time, without deteriorating the wanted in-band signal.

V. DIGITAL MITIGATION OF IQ IMBALANCES

In this section, a pilot-based compensation algorithm is proposed for coping with system performance degradation due to receiver I/Q imbalance in LTE downlink or any other OFDM modulated transmission link.

1) I/Q Imbalance Models for Direct-Conversion Multi-carrier Receivers: With perfect I/Q balance and within one OFDM symbol interval, the received frequency-domain waveform after cyclic prefix (CP) removal at the k-th bin of FFT output is typically written as

\[ Z(k) = S(k)H(k) + N(k) \]

in which \( S(k) \) refers to the transmitted signal, \( H(k) \) and \( N(k) \) represent the frequency domain baseband equivalents of the transmission channel and additive Gaussian noise, respectively. Here, in the wideband system context, we use the typical frequency-selective I/Q imbalance model from the literature (see [11], [12])

\[ Z_{RX}(k) = G_{1,RX}(k)Z(k) + G_{2,RX}(k)Z^*(-k) \]

where \( Z_{RX}(k) \) represents the amplitude and phase imbalance of the RX quadrature mixing stage and \( G_{RX}(k) \) denotes the I and Q branch frequency-response differences in the receiver.

A. Basic Compensation Principle

In order to mitigate the mirror-frequency interference term depicted in (5), assuming first that the I/Q imbalance properties \( G_{1,RX}(k) \) and \( G_{2,RX}(k) \) of the used radio device used are known. Then digital imbalance compensation can be carried out as

\[ x(k) = a(k)Z_{RX}(k) + b(k)Z_{RX}^*(-k) \]

with the idea of finding the two combination coefficients \( a(k) \) and \( b(k) \) such that the compensator output equals the received...
signal with perfect I/Q balance, i.e., \( x(k) = Z(k) \). Inherently, we have

\[
a(k) = \frac{G^*_1RX(-k)}{G_{1,RX}(k)G^*_1RX(-k) - G_{2,RX}(k)G^*_2RX(-k)} - \frac{G_{2,RX}(k)}{G_{1,RX}(k)G^*_1RX(-k) - G_{2,RX}(k)G^*_2RX(-k)}
\]

\[
b(k) = \frac{G^*_1RX(-k)}{G_{1,RX}(k)G^*_1RX(-k) - G_{2,RX}(k)G^*_2RX(-k)} - \frac{G_{2,RX}(k)}{G_{1,RX}(k)G^*_1RX(-k) - G_{2,RX}(k)G^*_2RX(-k)}
\]

where both \( a(k) \) and \( b(k) \) are only dependent on the I/Q imbalance coefficients at subcarriers \( k \) and \(-k\). Then proper I/Q imbalance estimation is the key to efficient imbalance compensation.

1) Pilot-Based I/Q Imbalance Estimation: Assuming the radio channel \( H(k) \) is time-invariant over a few consecutive symbol intervals, a pilot slot composed of two OFDM pilot symbols is assumed to be transmitted from the base station. With ideal synchronization, the corresponding FFT output samples at subcarriers \( k \) and \(-k\) measured over the two pilot symbol intervals appear as

\[
Z_{RX}(k) = \begin{bmatrix} Z_{RX,(1)}(k) & Z_{RX,(2)}(k) \end{bmatrix} = G_{R1}(k)H(k)
\]

\[
Z^*_{RX}(-k) = \begin{bmatrix} Z^*_{RX,(1)}(-k) & Z^*_{RX,(2)}(-k) \end{bmatrix} = G^*_{R2}(k)H(k)
\]

(7)

and \( S_{P(i)}(k) \), \( i = 1, 2 \) denote the two pilot symbol values at subcarrier \( k \). To emphasize simple implementation, the following pilot construction of the form

\[
S_{P(2)}(k) = jS_{P(1)}(k)
\]

(9)

is proposed here. The corresponding system matrix \( \tilde{H}(k) \) at \( k \)-th subcarrier can be obtained directly as

\[
\tilde{H}(k) = \text{diag} \left( G(k) \begin{bmatrix} 1 & j \\ 1 & -j \end{bmatrix} \right) \begin{bmatrix} 1 & j \\ 1 & -j \end{bmatrix}
\]

(10)

where \( G(k) = Z_{RX}(k) + Z_{RX}(-k) \). With this estimated system matrix \( \tilde{H}(k) \), the actual I/Q imbalance properties at subcarriers \( k \) and \(-k\) can then be obtained as

\[
\tilde{G}_{R1}(k) = \begin{bmatrix} Z_{RX,(1)}(k) & Z_{RX,(2)}(k) \end{bmatrix} \tilde{H}(k)^{-1}
\]

\[
\tilde{G}_{R2}(k) = \begin{bmatrix} Z^*_{RX,(1)}(-k) & Z^*_{RX,(2)}(-k) \end{bmatrix} \tilde{H}(k)^{-1}
\]

(11)

(12)

B. Simulations and Numerical Results

Next, the proposed compensation algorithm is demonstrated using computer simulator conforming to the LTE downlink setup specified in [12]. The used overall signal bandwidth is 20 MHz and 64QAM is deployed as subcarrier modulations. In general, as shown in Figure 5, with a fairly small amount of available pilot data, SER performance approaching the ideal reference system performance can be obtained using the proposed approach.

Fig. 5. Simulated system performance with 2 pilot slots and with pilot-subcarrier spacing J=6. Cubic spline interpolation is used to interpolate channel response as well as compensation parameters for active data subcarriers.

VI. CONCLUSION

This paper has demonstrated that some effects of nonlinearity and other non-idealities produced by the analog RF front-end sections of communications receivers can be tested and calibrated for by advanced digital signal processing techniques for a novel DFE-enhanced direct-conversion receiver design. Critical issues in the proposed test and calibration methods in receiver architectures have been investigated. Our results suggest ways to improve software radios in wireless terminals. We have also discussed certain novel advanced signal-processing techniques that can solve some of the critical problems of non-ideal analog RF circuits, and pave the way towards DSP-based, highly integrated, and highly configurable terminals.

REFERENCES