Viscoelastic Modeling and Reliability Assessment of Microelectronics Packages

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ABSTRACT

Viscoelastic stress relaxation occurs at operating temperature in underfill materials of flip-chip packages with high power devices. Multi-level finite element analysis is performed to study the impact of the viscoelastic relaxation on package reliability. The stress simulations reveal that the relaxation in underfill material leads to higher stress concentration in solder bumps. The failure analysis shows that the induced high stress develops higher crack driving forces. The results demonstrate that the underfill material property such as viscosity can shift failure mode from die corner delamination to near bump delamination. Therefore, the numerical study can be used as a guideline to select underfill material for package reliability improvements.

INTRODUCTION

Flip-chip technology utilizes solder bumps and surrounding underfills to package silicon chip. The chip-package interaction (CPI) is a major reliability concern for flip-chip packages with fragile low-k or ultra low-k dielectrics that are adjacent to the bumps and underfills \cite{1}, \cite{2}. Near bump and die corner delamination are the primary failure modes that are mitigated by selecting bump and underfill materials with lower thermal mismatch stress and higher strength \cite{3}, \cite{4}. As the industry is required to move towards lead-free bumps, the choice of underfill materials needs to be reevaluated. It has been observed that underfill materials exhibit non-negligible viscoelastic stress relaxation at operating temperature for high power devices. Viscoelastic relaxation in the underfill material may lead to stress redistribution and cause overloading and failure in the surrounding structures \cite{5}. While in situ observation is lacking, numerical analysis is necessary to understand the failure mechanisms.

In this study, an advanced process simulator is used for 3D package structure generation and for stress history tracking \cite{6}. The viscoelastic relaxation of underfill material is simulated using Maxwell model and the model parameters are extracted from measured data \cite{5}, \cite{6}. Submodeling technique is employed for global and local stress analyses and the J-integral method is used to calculate strain energy release rate. The simulation results are used to understand the failure mechanisms and to develop strategies for reliability improvements.
NUMERIC SIMULATIONS

Mechanical stress simulations are performed for the package structure shown in Figure 1. The overall dimensions of the structure are 20mm×1.884mm×0.5mm, and it consists of a die, a layer of smear material, a substrate, solder bumps and the underfill material. The smear material represents the BEOL structure on top of the chip, with the mechanical properties of the smear material being derived from the mechanical properties of its constituents. The solder material used in this study does not contain any lead and shows linear deformation over the temperature range studied in this work. The underfill material has a low glass transition temperature ($T_g$) and exhibits rapid stress relaxation at the operational temperature [5], [7]. The underfill material is simulated using the Maxwell viscoelastic model and the material properties are derived from earlier work [5]. Figure 2 shows the stress relaxation in the underfill material as a function of temperature under different strain values.

The residual mechanical stresses generated in the structure from the packaging process are determined for each of the material constituents and the impact of viscoelastic stress relaxation at the operating temperature of 125 °C is assessed. Initial cracks are also introduced at various locations in the structure to assess the reliability implication. Here, all the simulations use boundary conditions that allow movements at the maxima along the $y$ and $z$ directions but constrain displacement at the minima and maxima along the $x$ direction. These boundary conditions represent an elongated structure along the $x$-direction.

RESULTS AND DISCUSSION

Impact of viscoelastic relaxation

The impact of viscoelastic stress relaxation at the operating temperature of 125 °C is assessed for the package structures studied here. Figure 3 A and Figure 3 B show the Von Mises’ effective stress in the $y$-$z$ cross section of the package structure before and after stress relaxation, respectively. Figure 4 shows the effective stress before and after viscoelastic relaxation along a cut-line normal to the $xz$-plane and situated at the center of the solder bumps. Figure 5 A and Figure 5 B show the shear component of the stress, $S_{YZ}$, in the $y$-$z$ cross section of the package before and after stress relaxation, respectively. Figure 6 shows the shear stress ($S_{YZ}$) before and
after viscoelastic relaxation along a cut-line normal to the $xz$-plane and situated at the center of the solder bumps.

**Figure 3:** Von Mises’ Effective Stress (MPa) at 125 °C - (A) Before viscoelastic relaxation; (B) After viscoelastic relaxation

**Figure 4:** Effective stress (MPa) before and after viscoelastic relaxation

**Figure 5:** Shear Stress (MPa) at 125 °C - (A) Before viscoelastic relaxation; (B) After viscoelastic relaxation

**Figure 6:** Shear stress (MPa) before and after viscoelastic relaxation

**Figure 7:** Effective Stress (MPa) – (A) Before viscoelastic relaxation; (B) After viscoelastic relaxation

**Figure 8:** Shear Stress ($S_{YZ}$) (MPa) – (A) Before viscoelastic relaxation; (B) After viscoelastic relaxation

The mechanical stresses at chip edge and the first solder bump are examined in greater detail with refined local analysis. Figure 7 A and Figure 7 B show the effective stress in the first
solder bump and the surrounding region before and after viscoelastic relaxation at 125 °C, respectively. Similarly, Figure 8 A and Figure 8 B show the shear stress $S_{YZ}$ before and after viscoelastic relaxation at 125 °C, respectively. These results illustrate that stress relaxation occurs in underfill materials due to viscoelastic deformation at the operating temperature. However, the stress relaxation in the underfill material leads to the loss of load carrying capability subjecting the solder bumps to higher loading. The induced stress concentrations in the bumps, and surrounding regions on top of the bumps, are highest for the first bump close to the die edge. It is also interesting to note that the stresses are lower at die corner region after viscoelastic stress relaxation. This increased stress concentration at the first bump and reduced stress concentration at die corner indicates a possible shift of greater reliability concerns from the die corner to the first bump.

**Failure analysis**

The package behavior in the presence of defects or cracks, while undergoing viscoelastic relaxation is also examined in this study. Since the first solder bump experiences the largest stress increase, initial cracks are introduced near the first bump. A multi-level multi-scale submodel is derived from the global model and the stresses in the submodel are examined in detail. The submodel consists of the first solder bump and the package regions around the first solder bump. Figure 9 A and Figure 9 B show the effective stress in the submodel in a y-z cross section before and after viscoelastic relaxation at 125 °C, respectively. Figure 10 A and Figure 10 B show the shear stress $S_{YZ}$ in the submodel in a y-z cross section before and after viscoelastic relaxation at 125 °C, respectively. In this case, the initial crack is along the smear/underfill interface and close to the solder bump. Here, the crack spans the entire structure in the x-direction and the length of the crack is 35 µm in the y-direction. The crack location is indicated in these figures.

**Figure 9:** Effective stress (MPa) in the submodel with a near bump crack - (A) before viscoelastic relaxation; (B) after viscoelastic relaxation

**Figure 10:** Shear stress ($S_{YZ}$) (MPa) in the submodel with a near bump crack - (A) before viscoelastic relaxation; (B) after viscoelastic relaxation
Figure 11 A and Figure 11 B show the effective stress in the submodel in a y-z cross section before and after viscoelastic relaxation at 125 °C, respectively. Figure 12 A and Figure 12 B show the shear stress $S_{YZ}$ in the submodel in a y-z cross section before and after viscoelastic relaxation at 125 °C, respectively. In this case, the crack is along the smear/solder interface on top of the solder bump. Here, the crack spans the entire structure in the x-direction and the length of the crack is 35 µm in the y-direction. The crack location is indicated in these figures.

These results clearly indicate that underfill relaxation induced stress increase around solder bumps occurs at the presence of cracks. The increase in the bump stress is significantly large at the bump corner. These high stress regions present high energy release rate which serves as the driving force for local damage initiation and propagation.

The probability of package failure is evaluated using the strain energy release rate at the crack tips. The strain energy release rate is calculated using the J integral [8]. Figure 13 A and
Figure 13 B show the effect of viscoelastic relaxation on the J integral values at the left and right crack tips for the near bump crack and bump top crack, respectively. Here, the J integral values are normalized to the J-integral values calculated before the viscoelastic stress relaxation. These results show that viscoelastic relaxation in the underfill material leads to higher strain energy release rates for these cracks. Higher strain energy release rates essentially increase the failure probability and decrease the mechanical reliability of the structure.

SUMMARY AND CONCLUSIONS

Stress and reliability analysis has been performed for a flip-chip package structure consisting of lead-free solder bumps and low T_g underfill. Process simulation is carried out to build the package structure and to track the stress history. Maxwell model is employed to characterize the viscoelastic relaxation of the underfill material at operating temperature. It is found that the viscoelastic relaxation in the underfill material results in the loss of load carrying capability of the underfill layer. Mechanical load redistribution exposes the solder bump to higher stress. The high stress concentrations in the solder bumps and surrounding regions induce larger strain energy release rates for micro cracks in the regions, and impose greater reliability concerns. The results demonstrate that the underfill material property such as viscosity can shift failure mode from die corner delamination to near bump delamination. This study can serve as a guideline for material selection to improve the reliability and yield for flip-chip packages that employ lead-free solder bumps and low T_g underfill. Further studies can be carried out for flip-chip packages that are made of bump materials with large nonlinear deformations and underfills with high glass transition temperature.

REFERENCES