ABSTRACT
Advancements in IC manufacturing technologies allow for building very large devices with billions of transistors and with complex interactions between them encapsulated in a huge number of design rules. To ease designers’ efforts in dealing with electrical and manufacturing problems, regular layout style seems to be a viable option. In this paper we analyze regular layouts in an IC manufacturability context and define their desired properties. We introduce the OPC-free IC design methodology and study properties of cells designed for this layout style that have various degrees of regularity.

Categories and Subject Descriptors
B.7.1 [Integrated Circuits]: Types and Design Styles – advanced technologies.

General Terms
Performance, design, economics.

Keywords
IC layout regularity, OPC-free, manufacturability, DFM, advanced technology, multiple exposure, design paradigm, VLSI.

1. INTRODUCTION
The Moore’s-law-driven vision of the Information Technology evolution may fade away [9] due to cost increase of IC’s design and manufacturing observed in the last decade [7]. One can argue that there are three fundamental reasons causing such cost trends. First, the rate of minimum feature size decreases has not been accompanied by equivalent lithography wavelength decreases. Second, the rapid introduction of new materials has increased the yield learning difficulty. And billions of mutually dependent components placed in a modern IC pose a huge complexity for IC design and mask-making processes.

One of the avenues that the IC industry has taken to address these challenges is based on heavy investment in developing new Design for Manufacturability (DFM) strategies. In this paper, we introduce one such strategy. The design/manufacturing strategy presented here, unlike other such traditional strategies that attempt to interject a DFM component into a traditional IC design flow, introduces an entirely new IC design style and manufacturing scenario - both constructed with a focus on the design/manufacturing cost containment objective. The proposed strategy uses design regularity as its key cost containment tool.

2. DESIGN REGULARITY
The concept of regular design is as old as microelectronics itself. The most elegant examples of regular IC designs are the memories: DRAMs and SRAMs alike. Almost as regular are some FPGA ICs. Their regularity is achieved by naturally extending a rather obvious concept: an array-like arrangement of a replicated single cell. Today, design regularity in non-memory IC products seems to attract rapidly growing attention [3][5][6][7][8][10][11]. In this section, we will analyze this concept in more detail.

The term regular is typically used to describe an IC layout that has been constructed by repetitive usage of the same set of polygons arranged in a spatially periodic pattern. It is a widely held conviction that the greater the number of instances of the replicated set of polygons, the greater the gain from regular layout. The problem is that defining layout regularity in this way is insufficient to unlock the cost-saving opportunities potentially available via reuse of the prior design and manufacturing investments [8].

The insufficiency of this intuitive definition of regularity stems from the fact that only repetitive use of layout instances with identical neighborhoods may allow for reuse of prior design and manufacturing results. The size of the neighborhood – called here the area of relevance – is determined by the length of the radius of influence equal to the maximum distance between two layout elements with mutually dependent characteristics. One of the major problems of modern IC technology is that minimum feature size becomes a smaller and smaller fraction of the lithographic wavelength. Such a trend increases the relative size of the neighborhood, which must be taken into account in the modeling and analysis of a fraction of an IC layout. Of course, the larger the neighborhoods of two identical layout instances, the greater chance for mismatch between them. The chances for useful reuses may decrease with the progress of technology!

To better illustrate this problem Fig. 1a shows an array of identical squares representing the layout of a large block of vias. Each via is associated with its area of relevance or neighborhood, the size of which is determined by the radius of influence (see Fig. 1b.) All layout elements located inside the area of relevance (see again Fig.1b) will influence the final shape of the center via square’s image that will be exposed on the surface of the photoresist during the litho process. The difference between the ideal and actual shapes can be predicted by solving Maxwell equations for
the entire area of relevance. Then, appropriate layout corrections (OPC) can be applied to minimize discrepancies between the desired and the actual geometries of the processed IC layer. But this correction process becomes very costly when the radius of influence is large. And if is executed less than perfectly, systematic yield losses may occur.

Searching for the OPC results reuse opportunity we need to determine how to divide squares of Fig.1a into subsets such that each square in the subset has the same identical neighborhoods. Let us consider two options beginning with the radius of influence equal to 2. In this case there are three types of neighborhoods (see Fig. 1c):

1. A Corner Squares (CS) neighborhood (replicated in the analyzed bank of vias 4 times).
2. An Edge Squares neighborhood, which is identical for 26 vias located on the edge of the array; and
3. An Inner Squares neighborhood, which is exactly the same for the remaining 40 vias.

Thus, for the radius of influence equal to 2a, one must solve the

![Diagram showing different neighborhoods](image)

Figure 1. Potential benefits of design “regularity”.

OPC problem one time for each type of neighborhood, i.e. in the area at most equal to 3 times 5x5 a². Then, the OPC for remaining vias in the array is determined by reusing results already available. The cost-saving factor in this case is proportional to the ratio of the total area of the patterns, which must be modeled both when regularity is used and when it is ignored. For the above example, this ratio is equal to 75/217. The situation is very different when the radius of influence is increased to 4a (see Fig. 1d). In this case, the number of unique neighborhood patterns is much greater. The only reasonable solution is to calculate OPC for the entire array at once and the seemingly perfect layout regularity will not deliver any cost containment opportunity.

The above simple and very revealing example can be easily generalized. Note that squares in Fig.1 may be seen as outlines of more complex objects of the IC layout placed in a 2-D array with some vertical and horizontal spatial period. They also can be laid down with different sizes and pitches. But in any case these observations about impact of radius of influence and the OPC cost will still be valid.

Hence, one can formulate the following conclusions describing the relationship between layout regularity and potential for the reuse of design and manufacturing results:

1. Potential benefits associated with geometrically regular layouts can be harvested if the radius of influence is substantially less than the size of the analyzed layout array.
2. Benefits of geometrically regular layouts are insignificant if the radius of influence is comparable to half of the smaller dimension of the array of interest.
3. Since the radius of influence is determined by relevant physical phenomena, different processing steps may produce very different radii of influence for the same portion of the layout.
4. For most advanced IC technologies only very large arrays can benefit from layout regularity.
5. A traditional ASIC standard-cell-based design paradigm will not benefit from the improved regularity strategy discussed in the literature.

In reality, any new IC design/manufacturing paradigm must deliver a balance between performance, manufacturing costs, and design complexity. One first possible step towards such an objective is discussed in the reminder of this paper.

3. MINIMALLY IRREGULAR AND OPC-FREE IC

3.1 Lithographer’s Dream Patterns (LDPs)

By following the suggestions presented in the previous section, we quickly realize that the ultimate IC layout should be as close as possible to that which is composed of a wafer-size-collection of evenly spaced parallel strips and/or an array of evenly spaced squares both having the same width, height, and pitch. Better yet would be if all polygons of such patterns were placed on a grid whose period is an appropriate fraction of the wavelength of the light sources used in the lithography process. In addition, it would be desirable for such patterns to be manufactured without masks, i.e. using a mask-less process.

Fig. 2 depicts segments of such patterns with characteristics close to this ultimate goal and which - as we will show later - may be sufficient, with some modifications, to build IC interconnects.

We may ask: How can we create LDPs of both sufficient quality and acceptable cost? The full answer to this question cannot be provided in this paper. The short answer is that there are a number of visions and active research projects geared to producing inexpensive LDPs. Since all these are in a commercially embryonic stage, publicly available information about these projects is scarce [2][4]. One such a vision is that LDPs would be formed using a new type of lithographic scanner that would use a comb of energy beams scanned above the wafer with either...
horizontal or vertical orientations for Ho.1 and Ve.1 patterns, or in both directions for the contact/via pattern.

Figure 2. Lithographer’s dream patterns application.

3.2 Minimally irregular ICs

We will first focus on IC interconnects only. Assume that we have a stack of alternating vertical and horizontal metal layers built as LDPs on the same grid (see Fig. 2). These layers are perfectly regular and obey all design-guiding rules. But this stack of layers is electrically useless! We propose a design/manufacturing paradigm in which all products will use the same stack, referred to as an interconnect mold, and we will apply minimal modifications to it to obtain the needed functionalities. If this could be done, we would have ALMOST perfect regularity, uniform pattern density, huge potential for reuse, etc. We call such an IC design Minimally Irregular. We need to answer the following questions: How to build a perfect mold. How to minimally modify it, and how to understand the word ALMOST.

3.3 Lithography paradigm

A large spectrum of options for building and customizing the mold stack exists. Here we discuss one of them, a modified version of the double exposure lithographic strategy proposed in [1]. The essence of double exposure in [1] is to use, in one lithography step, two masks – one with very regular patterns (like LDPs), which would determine the geometry of all the performance critical edges of the printed layer; followed by a second mask, which would modify the pattern of the first exposure.

The lithographic paradigm proposed here is based on the same idea but we assume that more than two exposures could be applied. There are also very specific limitations imposed on the types of patterns allowed in all the exposures. We assume that for interconnect “mold” only one pattern, the horizontal LDP - is applied, referred to as Ho.1. Ho.1 is used to produce all other horizontal layers – Ho.i patterns – with one single exposure. All vertical LPDs, – Ve.i – patterns are manufactured in the same way by rotating the wafer 90 degrees. All orthogonal patterns Or.i require two exposures for each layer; first, with normal wafer orientation, followed by a second exposure after a 90-degree rotation. We also assume this manufacturing paradigm can be implemented using standard lithography equipment, an e-beam based strategy, and the scanning technique mentioned before.

Note that the back-end of the process, especially the poly layer, could use the same strategy.

For mold customization, we have a relatively large spectrum of options. All of them are based on the same assumption that customization is performed in the last exposure step with the least expensive technology – either using a mask or in a mask-less fashion. This is a very important assumption. It implies that customizing geometry CANNOT include the performance-critical edges of the IC layout. Hence, it can only be used to SUBTRACT from the mold geometry. This way, its imperfection will not affect the IC performance and therefore it can be geometrically sloppy, i.e., inexpensive.

The customization strategy is very flexible in terms of the amount of removed LDPs. In this paper, we consider a spectrum of options ranging from minimum area modification, which uses a minimum number of minimum area cuts in vertical and horizontal interconnect patterns and a fixed array of identical transistors, to removal of all layout geometries that are not absolutely necessary to perform the needed functions.

3.4 Almost regular and OPC-free

Based on the above explanation, one can note that from the lithography standpoint, the proposed design/manufacturing paradigm uses absolutely regular patterns and therefore, it can be perfectly printed without OPC and with the same precisely-tuned process for a large volume of products. However, this is not the case with CMP and etching. Depending upon the adopted pattern removal strategy, discussed later in more detail, we can claim ALMOST perfect regularity for the minimal removed strategy. For other strategies, the term almost may be still appropriate as well, if some extra restrictions on contact/via densities are used.

The bottom line claim is that the resulting design style, defined by the paradigm proposed in this section, can be called OPC-Free and minimally irregular.

4. IMPLEMENTING MINIMALLY IRREGULAR IC

We designed cells in several styles and degrees of layout regularity according to the OPC-free layout rules introduced in Section 3. We assumed a 2-D grid common for all layers. Diffusion patterns were formed horizontally. Every stripe’s width was fixed and the N- to P-diffusions ratio was set to 1:2. Poly gates were laid out as vertical sticks crossing diffusion stripes. Odd-numbered metal layers were vertical; even-numbered layers were horizontal. All vias and contacts were placed on the grid line intersections. The grid dimensions were compatible with minimal features feasible for 130 nm technology.

The cells were customized by introducing necessary metal cuts, vias, or contacts. We experimented on cells with the following degrees of layout regularity:

**Type A:** All cell patterns were on the grid.

**Type B:** All cell patterns were on the grid and all metal cuts were of minimum size.

**Type C:** All cell patterns were on the grid and the number of metal cuts, vias and contacts were minimized and uniformly distributed.

Type A cells were customized regardless of cost and all had patterns on the LDP’s 2-D grid. In type C cells, we took all customization costs under consideration and maintained uniform distribution of metal cuts, vias, and contacts. The degree of
irregularity of $B$ type cells was between Type $A$ and $C$. Fig. 3 shows an inverter constructed according to various layout types.

**Table 1. Different cell structures and regularity types**

<table>
<thead>
<tr>
<th>Struc.</th>
<th>Area</th>
<th>Timing</th>
<th>Power</th>
</tr>
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<tbody>
<tr>
<td>B</td>
<td>1.24</td>
<td>1.12</td>
<td>1.31</td>
</tr>
<tr>
<td>C</td>
<td>1.24</td>
<td>1.12</td>
<td>1.31</td>
</tr>
<tr>
<td>Average</td>
<td>1.24</td>
<td>1.12</td>
<td>1.31</td>
</tr>
</tbody>
</table>

Table 1 shows average performance, area, and power of six functional cells laid out on the LDP grid using different layout types and structures. The performance, area, and power results for Type $B$ and $C$ layouts were normalized to type $A$. Type $A$ cells had the best metric values due to unlimited customization. The areas of type $B$ and type $C$ cells were the same because only minimal metal cuts were removed. The average performance and power of Type $C$ cells were about 30% worse than Type $A$, whereas, for Type $B$, they were only about 12% worse. The delay and power overhead of the Type $B$ layout is caused by extra coupling capacitance introduced by floating wires. The delay and power overhead of the Type $C$ layout are caused by both the extra coupling capacitance of floating wires and the extended wire lengths. Table 1 shows that extended wires have more impact on power and delay than do additional coupling capacitances. These contributed to coupling capacitance, increased connected capacitance and resistance, and affected delay and power. Although having an extremely regular cell (type $C$) has huge performance/power overhead, reducing regularity a little to type $B$ cells can reduce 60% of overhead. The customization cost increase from type $C$ to type $B$ is small because only several extra metal cuts are needed to get rid of the extra connected wires.

To analyze the behavior of cells designed in various structures, we normalized the timing and power results to those of the corresponding $L$-structure cells, which could achieve the best performance and power metrics. The results indicate that among the unit cells, $U2$ had better performance and power than $U1$ due to its better diffusion abutment. However, unit cells with longer lengths may waste area if smaller cells need to be built. Longer unit cells may cause unbalanced rise and fall times due to fixed transistor width and less flexibility. Smaller unit cells had greater regularity and flexibility, but worse performance, area, and power consumption. $U2$ was better than $U1$ because it could realize all cells we experimented with using abutment, save the inverter.

**Table 2. Cell comparisons in different structures**

<table>
<thead>
<tr>
<th>Types</th>
<th>Timing</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1-H</td>
<td>1.275</td>
<td>1.269</td>
</tr>
<tr>
<td>U1-V</td>
<td>1.205</td>
<td>1.208</td>
</tr>
<tr>
<td>U2</td>
<td>1.078</td>
<td>1.043</td>
</tr>
</tbody>
</table>

If larger cells need to be constructed from smaller unit cells, then using $V$ structures will have smaller delay and use less power than $H$ structures due to shorter poly gate sticks and fewer poly contacts needed. The drawback is varying cell heights that may complicate placement and routing.

**5. CONCLUSIONS**

In this paper, based on analysis of IC layout regularity, we have proposed major modifications in the IC design/manufacturing paradigm. They enabled the introduction of a new, OPC-free design methodology for building manufacturing-friendly IC layouts. We described the results of initial assessment of this methodology. We already see performance-regularity tradeoffs, but many more and much larger circuits should be analyzed before final conclusions can be formulated. It is already obvious that conventional ASIC design flows will not be suitable to fully utilize the benefits of the proposed paradigm. Thus, development of a new computer-aided design flow, in addition to the development of multiple exposure lithography, will be the next two important steps towards application of layout regularity in support of Moore’s Law as proposed in this paper.

**6. ACKNOWLEDGMENT**

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**7. REFERENCES**