ASIC Design for Cell Search in 3GPP W-CDMA

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Abstract—This paper deals with an ASIC design and realization for a pipelined cell search algorithm in the 3GPP W-CDMA system. Pipelining three stages of cell search provides preferable performance, but also results in greed for high computing power. The ASIC implementation furnishes this computing power demand with a high-performance, cost-effective, and low-power solution. In the ASIC design, two synchronization code matched correlators are well designed and realized with reduced computing power. A weighted Comma-Free Reed-Solomon decoder is also proposed with superior performance, and realized in cost-effective and low-power architecture. Finally, this cell search chip is designed in a 3.3- to 0.35-μm CMOS technology with 44-um² core area and 1.32 W power dissipation, complying with the 3GPP W-CDMA system specifications.

I. INTRODUCTION

The 3GPP (3rd generation partnership project) W-CDMA (wideband code division multiple access) system recently has been adopted as one of the standards in the IMT-2000 3G (third generation) system family [1]. In 3GPP W-CDMA systems, a mobile procedure of searching for an appropriate base station nearby and synchronizing to its cell-specific downlink scrambling code is the so-called cell search [2][3].

Fig. 1 A downlink receiver in W-CDMA system

In W-CDMA systems, the cell search is carried out through three stages by employing two well-designed synchronization channels and a common pilot channel [2]. In the first stage, the primary synchronization channel (P-SCH) is detected for slot synchronization. After that the secondary synchronization channel (S-SCH) is detected for frame synchronization and code group identification in the second stage. In the third stage, the cell-specific downlink scrambling code is determined by de-scrambling the common pilot channel (CPICH) with all possible scrambling codes in the identified code group.

The execution strategies of three-stage cell search have two main categories: the serial [2] and the pipelined executions [3]. In a serial cell search algorithm, a new search cannot be commenced unless the former goes through the three stages of synchronization step by step. It usually takes more time than the pipelined alternative, in which the three stages of synchronization are concurrently performed so as to reduce its search time. However, the pipelined cell search is sophisticated and results in the demand for high computing power. For fast cell search, an ASIC approach to the pipelined cell search is concerned in this paper. Moreover, the pipelined cell search is performed in a cordless user equipment. After achieving mandated processing capability, the ASIC power consumption and area efficiency are followed with high interest.

This paper presents a cell search ASIC capable of pipelining three-stage functions with reduced computing complexity, cost-effective core area, and low-power consumption. All detailed design features of the ASIC and its performance will be discussed in the paper. The remainder of this paper is organized as the following. Section II describes the pipelined cell search algorithm which is realized in the proposed ASIC. In section III, architecture of each stage function and the whole chip is presented. Implementation results and performance are summarized in section IV. Section V concludes the ASIC design of cell search.

II. PIPELINED CELL SEARCH

In order to clearly explore the pipelined cell search algorithm of W-CDMA systems, this section is divided into three subsections to describe physical channels associated with cell search, three-stage cell search algorithms, and the adopted algorithm parameters in the ASIC realization. They are described as the following.

A. Physical Channels

There are two physical channels used to help cell search in 3GPP W-CDMA systems, i.e. SCH (Synchronization Channel) and CPICH (Common Pilot Channel). The SCH includes P-SCH and S-SCH, Both P-SCH and S-SCH are not scrambled and only transmitted at the first 256 chips of each slot as shown in Fig. 2. Fig. 2 also illustrates that the CPICH is scrambled and always transmitted in each frame.

The P-SCH is dedicated to slot boundary detection in the first stage of cell search. All cells apply the same PSC (Primary Synchronization Code) sequence to their P-SCH, and as a result, only a unique PSC matched correlator is required in mobiles for the slot boundary detection.
The S-SCH is designed for frame boundary and code group identification in the second stage of cell search. In a cell, the S-SCH makes use of 16 SSC (Secondary Synchronization Code, $c_{k}(t)$) sequences to carry the same CFRS (Comma-Free Reed-Solomon) codeword in each frame. A cell’s CFRS codeword stands for its code group to which itself cell-specific downlink scrambling code belongs. The comma-free property of the CFRS codeword helps to detect frame boundary [5]. Accordingly, in order to achieve code group and frame boundary identifications, a mobile has to detect the SSC sequences and decode the received CFRS codeword and its cyclic shift.

The CPICH carries the downlink common pilot symbols and is devoted itself to cell-specific downlink scrambling code determination in the third stage of cell search. Its common pilot symbols are complexly scrambled by the cell-specific downlink scrambling code. After achieving slot and frame synchronization and code group identification with the best cell site, a mobile could make use of CPICH to determine the cell-specific downlink scrambling code among all possible candidates in the identified code group.

### B. Cell Search Algorithms

According to 3GPP W-CDMA standard and several previous researches [2]-[4], the cell search algorithm consists of three stages: 1) slot boundary detection, 2) frame boundary detection and code group identification, and 3) scrambling code determination. The cell search algorithm of three-stage processing is described as following.

1) **Slot boundary detection**: In the first stage, the mobile intends to detect the slot boundary of the best cell by matching PSC in the P-SCH. A specific PSC matched correlator is used to detect the slot boundary. Because of the low signal-to-interference ratio operating condition in W-CDMA system, the PSC matched correlator results have to be non-coherently accumulated over a suitable number of slots for more trustworthy decision statistics. Fig. 3 illustrates the functional block diagram of this stage procedure. After accumulating PSC matched results enough, several maximum results are picked out as slot boundary candidates for the next stage processing.

2) **Frame boundary detection and code group identification**: After slot boundary detection, the S-SCH, which aligns with P-SCH, could be easily received. In this stage, the mobile has to identify which one of 16 possible SSC sequences is used in the S-SCH and assembles 15 consecutive indices of received SSC sequences to be a CFRS codeword with uncertain cyclic shift volume. This CFRS codeword stands for code group to which the cell-specific downlink scrambling code belongs, and its cyclic shift volume helps detect frame boundary through its comma-free property. Accordingly, it has to identify the received CFRS codeword is which one among 64 alternatives and its cyclic shift volume. Fig. 4 shows functional block diagram of the second stage procedure. Since the P-SCH is always transmitted in alignment with the S-SCH, the P-SCH correlating result can be a phase reference to correct the possible phase error during the S-SCH matched correlation. That is, a coherent detection was recommended in this stage [3].

3) **Scrambling code determination**: After achieving frame synchronization and code group identification, the cell-specific downlink scrambling code could be determined by de-scrambling the CPICH with limited possible scrambling codes in the identified code group. Fig. 5 illustrates the determination processing of the third stage. The de-scrambling process is performed over a certain number of coherent chips. These de-scrambling results are mutually compared to find out the maximum. The scrambling code candidate which results in the maximal de-scrambling result could obtain one vote. After de-scrambling over 38400 chips of a frame, the scrambling code candidate, which wins the maximum of votes whose number exceeds a well-determined threshold, could be recognized as a valid scrambling code used by the best cell.

Pipeline cell search algorithm ideally pipelines the execution of three-stage functions. Fig. 6 shows the processing flow of pipelined cell search. Since the cell-specific scrambling code is detected and recognized, the frequency acquisition and the broadcasting information reception could be commenced.

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C. Algorithm Parameters

In this paper, the cell search chip is assumed to work together with a crystal oscillator whose inaccurate range is 3 ppm. The 3 ppm inaccuracy range gives rise to 6 kHz frequency offset in a 2 GHz communication system. As a result, 256-chip time is still coherent duration, and a code correlator matching over 256 chips does not result in disarrangement correlation error. The algorithm parameters of pipelined cell search are defined and summarized in Table I.

III. ARCHITECTURE DESIGN

A. Stage 1 Architecture

Corresponding to Fig. 3, Fig. 7(a) illustrates the data path architecture of stage 1 procedure. In this stage, slot boundary detection has to draw support from vigorous correlation property of PSC sequence under low SIR operating condition in W-CDMA. The PSC sequence is a GHG (Generalized Hierarchical Golay) sequence [4][6]. There exists an EGC (Efficient Golay Correlator) which could be used to perform correlation procedure with very low computation power. As mentioned above, the correlation length of PSC is $CL_{	ext{PSC}} = 256$. A typical matched correlator with 256 taps requires 255 add/subtract operations. The EGC requires only 13 add/subtract operations. Accordingly, an EGC is adopted to reduce computation loading, i.e., it results in lower power consumption. Fig. 7(b) shows the detailed EGC architecture for W-CDMA cell search.

According to non-coherent detection in this stage, consecutive outputs of EGC will be accumulated non-coherently over $AK_{t}$ slots to procure reliable statistics for slot boundary decision. It employs an accumulator that has 2560 chip fields and each field is necessary to accumulate for 15 slots. The accumulator is comprised of an adder and a register file with 2560 fields shown in Fig. 7(a). A general on-chip shift register, which is necessary to shift 2560 data per chip time, draws tremendous power consumption and core area. The shift register is realized by an off-chip SRAM with 5.12 KB. The Max function consists of a comparator and register, which serially compares accumulation results.

B. Stage 2 Architecture

The Fig. 8(a) illustrates the data path architecture of stage 2 procedure. By taking advantage of EGC and low-power shift register concepts [7][8], a hierarchical SSC matched correlator is proposed to mitigate the computation loading of correlations by means of hierarchical decoding and reduce power consumption. The hierarchical SSC decoder consists of a partial EGC (Efficient Golay Correlator) with four iterations for inner decoding and an active correlator with a 16-field register file for outer decoding. The inner decoder is designed according SSC constructing method [4]. Taking advantage of hierarchical decoding concept, only one active correlator with a 16-field register file is capable of accomplishing 16 active correlations between each interval of two consecutive inner decoding results. The 16-field shift register architecture is shown in Fig. 8(c), and it consumes about half power of the general counterpart.

Before CFRS decoding for frame boundary and code group identification, a hard-decision among 16 SSC correlation results is performed to reduce subsequent CFRS decoding complexity. Besides, the SSC hard-decision result is treated as the weight of this code symbol for the subsequent CFRS decoding. The hard-decision block is design with a serial comparator and a list table as shown in Fig. 8(a).

After receiving over $DL_{	ext{CFRS}}$ slots, a full-length CFRS codeword with certain cyclic shifts is ready for decoding. The CFRS decoding is to perform a hypothesis-decision process among 960 hypotheses. These 960 hypotheses come from total 64 possible codeword and 15 cyclic shift possibilities per codeword. A weighted decoding method is adopted for preferable performance. That is, only when the code symbols are equal to hypothetical ones, their weights are added into

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<table>
<thead>
<tr>
<th>Parameters</th>
<th>Length</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$CL_{	ext{PSC}}$</td>
<td>256 chips</td>
<td>The matched correlation length of primary synchronization code. A full-length PSC matched correlation over 256 chips is still a coherent duration.</td>
</tr>
<tr>
<td>$AK_{t}$</td>
<td>15 slots</td>
<td>The non-coherent accumulation length in stage 1. A suitable length for reliable statistics is over 15 slots.</td>
</tr>
<tr>
<td>$CL_{	ext{EGC}}$</td>
<td>256 chips</td>
<td>The coherent matched correlation length of secondary synchronization code. It is the full-length 256 chips of PSC sequences.</td>
</tr>
<tr>
<td>$DL_{	ext{CFRS}}$</td>
<td>15 symbols</td>
<td>The CFRS decoding length in stage 2. A full-length codeword has 15 code symbols. The robust Hamming distance 13 between different codewords is only reserved under full-length case.</td>
</tr>
<tr>
<td>$DS_{	ext{Lack}}$</td>
<td>256 chips</td>
<td>The de-scrambling length of one vote in stage 3.</td>
</tr>
<tr>
<td>$Th_{	ext{vote}}$</td>
<td>38 votes</td>
<td>The threshold number of votes for recognizing a cell-specific downlink scrambling code election is valid. According to [3], it is assumed as 38.</td>
</tr>
</tbody>
</table>

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Fig. 7 Stage 1 hardware architecture
the hypothesis correlation results. In its circuit design, the weighted correlation processes of 15 symbols between the received codeword and 960 hypotheses are fully pipelined. Fig. 8(d) shows the weighted correlations that are accomplished by simple systolic array architecture. Afterward correlation results are compared to find out the maximum as the CFRS decoding result.

C. Stage 3 Architecture

In the third stage, eight parallel de-scrambling with respective scrambling codes and a decision mechanism by majority vote are used to identify cell-specific downlink scrambling code. Fig. 9(a) illustrates the data path architecture of stage 3 procedure. Each de-scrambling over $DL_{c3}$ chips results in one vote. After de-scrambling over 38400 chips, total 150 votes are distributed among 8 candidates. The scrambling cod candidate that has the maximal votes and exceeds $Th_{OTE}$ is recognized as a valid scrambling code of the best cell.

D. Whole Chip Architecture

In order to determine a suitable quantification bit number, a serial of simulations of dynamic rang and quantification has been run iteratively [9]. As a result, a 4-bit quantification is well suited to cell search algorithm with low hardware complexity and slight performance loss. The whole chip architecture is illustrated with exact bit widths in Fig. 10. For more cost-effective hardware design, there are two truncations used in stage 1 and 2, respectively. Both truncations will not induce serious performance loss.

IV. IMPLEMENTATION RESULTS AND PERFORMANCE

The design of the chip was carried out through a "top-down" design approach based on Verilog hardware description language (HDL). Design with HDL provides a technology-independent and highly flexible description at the
behavior level (or RTL). The behavior-level description of cell search was synthesized into gate-level design by the logic synthesis tool Synopsys involving a cell library in 3.3-V 0.35-um CMOS technology. Afterward the back-end design was accomplished by using Cadence tools. The whole chip layout is shown in Fig. 11, containing 41,817 gates and three ROMs for SSC outer codes (16x16 bits), CFRS codes (64x60 bits), and initial phases of 512 scrambling codes (512x18 bits). The core area of cell search chip measures only 4x4 mm^2. The critical path of the whole chip exists in square-sum operation. The maximum clock frequency is 200 MHz according to post-layout simulations. This high clock rate is derived from the well-pipelined hardware architecture.

To evaluate the real cell search time of this chip, an ASIC bit-true model was developed for performance simulation in the presence of Rayleigh fading, intra-cell interference and inter-cell interference [9]. The quantization and truncations of the ASIC prolong the cell search time slightly. The real cell search time of the chip is shown in Fig. 12. In stage 1 and 2 procedure, the signal power is the SCH power that includes both P-SCH and S-SCH powers. The proportions of both P-SCH and S-SCH channels are equal to each other. In stage 3 procedure, the signal power is the CPICH power. Besides, the SCH power equals to the CPICH power. The interference power includes inter- and intra-cell interferences’ power.

V. CONCLUSIONS

A cell search ASIC complying with the 3GPP W-CDMA standard has been designed and presented in this paper. Pipelined cell search is adopted to improve cell-searching time. In the ASIC design, both synchronization matched correlators for PSC and SSC sequences were well elaborated with low-computing power and cost-effective area. A weighted CFRS decoder with preferable performance was also designed in simple systolic array architecture. Moreover, 4-bit quantization for input signals and two truncations within stage 1 and 2 were presented to effectively reduce chip area with slight performance loss. Finally, the cell search chip was implemented in a 3.3-V 0.35-um CMOS technology with 4x4-mm^2 core area and 1.38-W power dissipation.

![Fig. 11 Whole chip layout](image)

![Average Cell Search Time](image)

![Fig. 12 ASIC cell search time](image)

REFERENCES


