Abstract—This paper presents a new hardware implementation of gate drive circuits applied to low-power neutral-point-clamped (NPC) multilevel three-phase inverters. The proposed circuit is based on commercially available MOS-gate driver ICs (MGDs) for large-scale applications, which may reduce the total cost of implementation of NPC inverters. Only one dc power supply is required to feed all the gate drivers for the three-phase system. Detailed design procedures are presented, which include the protection circuits for avoiding hazardous switching states of the power switches. Experimental results of a laboratory prototype demonstrate the validity of the proposed circuit. These results also suggest that for achieving safe operation of snubberless power switches during transients, a hybrid implementation of each NPC phase leg, consisting of MOSFETs with voltage ratings at half the dc bus voltage and of insulated gate bipolar transistors rated at the total dc bus voltage, is recommended.

Index Terms—Charge pump technique, gate drive circuit, switch-voltage balancing, three-level neutral-point-clamped (NPC) inverter.

I. INTRODUCTION

MULTILEVEL inverters have been considered a high-potential technology for high-power high-voltage applications, since they can offer some advantages over their two-level pulsedwidth modulated counterparts, such as reduced switch-voltage ratings, reduced switch \( \frac{dv}{dt} \) stresses, and output voltage waveforms with improved spectra at lower switching frequencies [1]–[3]. In particular, neutral-point-clamped (NPC) inverters have been receiving increased attention recently for the integration of renewable energy sources to the utility grid [4]–[6] and for low-voltage drives, traction, and utility applications [7], [8]. Thus far, special concerns on the controls of these inverters have been extensively reported [9]–[14]. Nevertheless, low-voltage applications of three-level NPC inverters are still very restricted, and few works on this topic have been done [7], [8], [15]. Although the use of integrated gate drive circuits [MOS-gate driver ICs (MGDs)] for controlling two-level inverters are very common, this has not yet been the case for multilevel inverters. The development of low-cost and reliable gate drive circuits may considerably reduce the total cost of implementation of multilevel inverters, and then make them a competitive solution in industries. In [7] and [16], gate drive circuit was proposed based on the bootstrap charge pump scheme, which was applied to a three-level NPC three-phase inverter and to one phase leg of an eight-level floating source multilevel inverter, respectively. In those works, power MOSFETs were used, and the gate drivers were composed of discrete components.

This paper is focused on the implementation of the charge pump technique with commercially available MGDs, generally applied to two-level inverters, for the power switches of three-level NPC inverters. The proposed gate drive circuit is intended for applications up to a 500-dc-link voltage, making it suitable for a great number of low-voltage industrial applications where power MOSFETs could be applied. The implemented circuit requires only one dc power supply to feed the whole gate driver for the three-phase system. Moreover, it allows for independent triggering and long conduction time of the power switches. These attributes are usually more restricted in conventional gate drive circuits, based on the charge pump technique, and it may impose some limitations to the inverter performance [17], [18]. In [17], some design considerations and preliminary experimental tests for one phase leg of the NPC, connected to a dc-link voltage rated at 64 V and with a resistive load, were presented. In the work developed in this paper, experimental tests were carried out on a three-phase NPC inverter at a dc bus voltage equal to 320 V, while feeding a three-phase resistive load and also when it was driving an unloaded 1-hp/3450-r/min induction motor. During these tests, the voltage balancing on the power switches was of a special concern. Special care was taken on implementing protection circuits in order to avoid switching states which could cause damage to the power switches. Moreover, the total harmonic distortion (THD%) in the output voltages is shown for verifying the proper operation of the inverter. For
completion, the results of the previous work [17] are also presented here.

This paper is organized as follows. In Section II, important design issues on gate drive circuits are described, with emphasis on the use of integrated circuit devices of type MGD. In Section III, the use of MGDs, applied to NPC inverters, and the proposed gate drive circuits are explained. In Section IV, the experimental results are shown, and the conclusion is presented in Section V.

II. CHARGE PUMP TECHNIQUE

A block diagram of an inverter switch, with control and power stages, is shown in Fig. 1. Control circuits, protection scheme, the gate drive circuit, and its associated auxiliary power supply are in the control stage, together with the main power supply. The dc bus (VDC+) and power switch are in the power stage. In this work, the auxiliary power supply consists of the bootstrap capacitor voltages, as it will be shown later in this paper.

The ground connection of power switches depends on the converter topology and can generally be arranged in two different ways. One is by connecting the emitter (or source) terminal to the control ground reference. It is of simple triggering, and no special procedure is needed. In the other way, when S1 (Fig. 1) is floating, as referenced to the control ground point, an isolated (auxiliary) power supply is required to turn it on. This makes the design of the control stage more complex, particularly when the power stage has several power switches floating from the ground reference. Hence, in this paper, only the second case is considered.

The basic function of the gate drive circuit is to properly trigger the power switches with the use of isolated power supplies that provide safe operation of the inverters [18]. The charge pump is a simple technique of implementing low-cost gate drivers and is very popular in industries [19]. In the next section, this technique is explained.

A. Typical Charge Pump Circuit

The charge pump technique is based on a charged capacitor that works as an auxiliary voltage source for switching voltage-controlled power switches, such as MOSFETs and insulated-gate bipolar transistors (IGBTs). The charge pump circuit has a voltage supply V1, a diode D1, and a capacitor C1, as shown in Fig. 2. In this case, the auxiliary voltage supply, which corresponds to the isolated supply, is made up by the capacitor C1. Its working cycle is described as follows [19].

1) The capacitor C1 is charged up to the voltage V1 by the current flowing in the loop containing D1 and the load, while the power switch S1 is opened.
2) A signal is sent to activate the optocoupler OP that connects C1 to the switch control terminals, and then, the capacitor voltage turns S1 on. In this situation, the diode D1 prevents C1 from discharging through the main power supply and protects the circuitry that is connected to V1.

The circuit shown in Fig. 2 is very simple but it does not allow long conduction times of the switch, considering that C1 will discharge due to leakage currents and S1 bias current. If longer turn-on times are desirable, some capacitor recharging procedures should be provided [19], [20]. The proposed circuit provides a way to recharge this capacitor.

A gate drive circuit based on the charge pump operation is integrated in a simple and low-cost device named MGD, and it has been used as a good choice to implement power inverters for industrial applications.

B. MGD Characteristics and Practical Considerations

A typical application using the commercial IR21xx family is shown in Fig. 3. It shows an easy way to implement a high-speed one-phase inverter leg using high- and low-side
The high-side output (HO) is the only one that uses the charge pump technique. The low-side output (LO) is a high-current ground-connected buffer.

The point connections HO, LO, VB, and VS in Fig. 3 correspond to those shown in Fig. 2.

The inverter and gate drive circuit (MGD), as well as the charge pump components, are usually specified based on the dc bus voltage, maximum output switch current, and switching frequency.

Therefore, the following items must be taken into account during the components’ selection [19]–[21].

1) MGD: The MGD output sink current greatly influences the choice of switching frequency. This characteristic and the dc bus voltage are critical for selecting this component. Commercial devices can be found with output current ranging from 100 to 2000 mA and voltages from 100 to 1200 V.

2) Diode D1: As mentioned before, when the high-side switch is turned on (S1 in Fig. 2 and Q1 in Fig. 3), the diode will be reverse-biased with a voltage close to the dc bus value. Aside from this, it should have a fast response time to allow for quick charge changes on C1. Therefore, the diode D1 must be carefully chosen. It must be pointed out that in the proposed circuit, there is no need to use any bootstrap diode.

3) Capacitor C1: A minimum capacitive value must be specified for the sake of a proper and safe switching procedure. On the other hand, large capacitance values may cause problems to the recharging process. Capacitors of tantalum or polyester types are commonly preferred.

The minimum capacitance value is given as [19]

\[
C_1 = 2 \left( \frac{2Q_g + \frac{1}{f_{sw}} \max{I_{qbs}} + Q_{ls}}{V_1 - V_{D1}} \right)
\]

where \( f_{sw} \) is the switching frequency, \( Q_g \) is the total gate charge of the high-side switch (typically \( 20 \text{nC} < Q_g < 150 \text{nC} \)), \( Q_{ls} \) is the shift charge level required per cycle (typically equal to \( 5 \text{ nC} \) for 500 V/600 V ICs or \( 20 \text{ nC} \) for 1200 V ICs), \( V_{D1} \) is the forward voltage drop across the bootstrap diode, and \( I_{qbs} \) is the quiescent current for the high-side driver circuitry (approximately equal to 0.8 mA).

In practical situations, the actual value of \( C_1 \) must be much higher than the one obtained from (1).

III. MGD-BASED GATE DRIVE CIRCUIT FOR NPC INVERTERS

Fig. 4 shows one phase leg of an NPC, where the neutral point \( N \) and the MGDs associated with the switches (Q1–Q4) are shown. The NPC operation, as described next, is based on a sequence of switching pairs of power switches (Fig. 4). Dead-time intervals are inserted between each changing of switch state, in order to avoid short circuit in the dc links (CUP, CLOW).

1) Initially, all switches are off.

2) Q3–Q4 are then turned on, while the others remain off.

3) Q3–Q4 are turned off, dead-time interval is inserted, Q2–Q3 are turned on, and Q1 remains off.

4) Q2–Q3 are turned off, dead-time interval is inserted, Q1–Q2 are turned on, and Q4 remains off.

5) Q1–Q2 are turned off, dead-time interval is inserted, and Q3–Q4 are turned on.

6) Repeat sequence from step 3).

This sequence repeats continuously throughout the operation of the inverter.

The charging process of the bootstrap capacitors (C1–C3) is accomplished by means of this switching sequence. The capacitors C2 and C3 are continuously recharged through V1, and diodes D2 and D3, respectively, when the switches Q3–Q4 are on.

In step 3), C1 is being charged by C2 through D1, and in step 4), C1 remains connected to C2.

This circuit has some usage restrictions, namely, the limitation of the switches’ conduction time, as mentioned in Section II-A, and unbalanced capacitor (C1–C3) voltages which are mostly caused by the voltage drops in the switches and diodes. These drops may set the switches in their linear operation region and damage them. Aside from it, it is important to define a switching sequence, as described in steps 1), 2), 3), 4), 5), and 6).

The proposed gate drive circuit eliminates the switching sequence, as previously described, and the bootstrap diodes D1–D3.
A. Verification of the Switch-Voltage Balance

In this section, some preliminary tests are presented with the use of FLUKE 99 scopemeter series II—50 MHz. Fig. 5 shows the switch Q3 voltage waveform when the circuit of Fig. 4 was initially tested with one phase and a resistive load connected between the dc bus (±64 V) and the output of the inverter. This condition is bound to occur in three-phase applications if the control signals of the other phases are not synchronized.

As it is shown in Fig. 5, an overvoltage occurs on the switch Q3, which, in this case, is equal to the total dc bus voltage. This should not happen in an NPC inverter.

This problem can be caused by two main factors.

1) When a pair of switches (in this case, Q3 and Q4) is not switched on at the same time. In this case, an overvoltage problem can occur, depending on the load configuration. A proper design of the control logic can prevent this occurrence.

2) When a bootstrap capacitor is recharged through an inadequate current path.

Fig. 6 shows case 2), where C3 is recharged through current \( i_{cp} \).

When the switches Q3 and Q4 are turned on, the bootstrap capacitor C3 is charged by the voltage source V1. When these switches are turned off, the voltage drop of the diode D3 remains low (as if it is conducting) for a long time, due to the fact that Q3 and Q4 are in the high-impedance state and, consequently, there is no reverse current in D3. In this situation, according to the voltage Kirchoff law, the voltage across Q4 is zero, and then, the voltage across the switch Q3 will be equal to the dc-link voltage (VDC+).

The proposed circuit (Fig. 9) will be described in the next sections. It does not use bootstrap diodes, eliminating the previously mentioned second factor of failure, as shown in Fig. 7. It shows that there is no overvoltage in the switches and their voltages are equal to half of the VDC+.

B. Protection Circuits

In order to avoid hazardous switching states, some protection procedures were included in the proposed circuit. Special switching states are required for preventing the total (VDC+) or partial dc-link voltage from short-circuiting. Moreover, the switching sequences of switch pairs must be synchronized, and dead-time condition must be inserted as well. In Table I, the permissible switching conditions are shown, where it can be seen that three states cause short circuit.

Fig. 8 shows the schematic diagram of the protection circuits. There is a logic circuit that prevents invalid switching states at Q1–Q4, based on Table I. In case that it happens in the control inputs g1–g4, the inverter is disabled. Adjustable dead-time circuit, start-up reset, and shut down by external command are also included.

C. Proposed Gate Drive Circuit for Three-Level NPC Inverters

The purpose of this section is to present a way of keeping the bootstrap capacitors charged in the NPC topology and of eliminating the limitations of the circuit in Fig. 4. Fig. 9 shows the schematic diagram of the proposed gate drive circuit for one phase leg.
A single dc power supply set to 15 V (main power supply in Fig. 1) is used to feed the MGDs and the protection circuits. The bootstrap capacitors C1–C3 (auxiliary power supply in Fig. 1) are charged by the dc bus VDC+, via an external refresh circuit named charge control, associated with three current sources I1, I2, and I3. With this method, it is possible to keep each switch turned on for long time intervals and to keep the bootstrap capacitor voltages controlled and stable.

Moreover, each pair of power switches can be enabled independently, which avoids the need of predefined switching steps 1), 2), 3), 4), 5), and 6) [7].

The charge control circuit is shown in more detail in Fig. 10. It can be implemented basically with an oscillator and a low-power voltage doubler rectifier. The current source and the Zener diode help to produce a low ripple in the power-supply circuit. The current sources can be implemented with the use of simple components, such as resistors, Zener diodes, and/or transistors.

Fig. 11 shows a scheme presenting the energy balance of a gate drive circuit using MGDs with a charge pump technique. The total power loss that occurs during the switch turn-on is directly affected by the switching frequency, and it is named $G_p$ in Fig. 11.

The power lost in the MGD, caused by internal bias current, was named $B_p$. The external refresh circuit that keeps the bootstrap capacitor charged, as shown in Fig. 10, must be able to transfer the total power ($P_{aux}$), as follows:

$$P_{aux} \geq (B_p + G_p)$$ (2)
where (2) can be written as

\[ P_{aux} \geq (V_{C1} \ast I_{qbs} + f_{sw} \ast V_{C1} \ast Q_{g}) \]  

where \( V_{C1} \) is the voltage in capacitor C1 and \( I_{qbs} \) and \( Q_{g} \) are as described in (1).

By using (2) and (3), the minimum value of the current sources \( I_{1}, I_{2}, \) and \( I_{3} \) can be calculated so that the automatic recharge process works properly, and that means keeping all the bootstrap capacitors charged continuously. The current sources can be calculated with

\[ I \geq \left( \frac{V_{C1} \ast I_{qbs} + f_{sw} \ast V_{C1} \ast Q_{g}}{V_{Z} - V_{D4} - V_{D5}} \right) + I_{qos} \]  

where

- \( I_{qos} \) quiescent current for the oscillator;
- \( V_{Z} \) Zener voltage used to supply the oscillator;
- \( V_{D4} \) and \( V_{D5} \) forward voltage drops in the diodes D4 and D5, respectively.

The specification of the oscillator capacitance \( C_{P1} \) (Fig. 11) is defined as

\[ (V_{CP1} \ast f_{osc} \ast Q_{CP1}) \geq P_{aux} \]  

where \( f_{osc} \) is the oscillator switching frequency and \( Q_{CP1} \) is the charge level in \( C_{P1} \). The left-hand side in (5) means the maximum (theoretical) power transfer of the charge control circuit (Fig. 11).

By considering the approximations

\[ V_{CP1} \approx V_{C1} \]  
\[ (V_{Z} - V_{D4} - V_{D5}) \approx V_{C1} \]

a final result can be written as

\[ C_{P1} \geq \left( \frac{I_{qbs} + f_{sw} \ast Q_{g}}{V_{C1} \ast f_{osc}} \right) \]  

Since there is no refresh circuit associated with the current source \( I_{1} \), this current source can be set to a value lower than the one defined by (4).

The current sources play an important role for balancing the switch voltages.

**D. Switch-Voltage Balancing**

It is desirable that each power switch handles as low voltage as possible during OFF-state. In the proposed circuit, the specification of the current sources \( I_{1}, I_{2}, \) and \( I_{3} \) (Fig. 9) influences the switch blocking voltage and their balancing. These current sources force the diodes DA and DB to conduct in the proper time, which helps the balancing process of the switch voltages. In addition to this, the voltages of capacitors CUP and CLOW must be controlled so that the neutral point is maintained around half of the dc bus voltage.

If the switches Q3 and Q4 are turned on (Fig. 9), the current source \( I_{3} \) will prompt the diode DA to conduct, and then, the total dc bus will be equally divided among Q1 and Q2. A similar situation happens when the switches Q1 and Q2 are turned on. In this case, the current source \( I_{1} \) will force the diode DB to conduct, and the other switches will have their share of the total dc bus.
Fig. 13. Switching sequence of square-wave control applied to the NPC inverter.

The diodes DA and DB will assure that when Q2 and Q3 are turned on, the output voltage of the inverter will be equal to half of the dc-link voltage, which implies that the switches Q1 and Q4 will also be at half of the dc voltage value.

When all switches are turned off, as it is the case during dead-time intervals, both current sources I1 and I3 will work as described before.

It must be pointed out that at any switch state, the current sources operate independently, which implies that the refresh
circuits also operate continuously. Then, all the bootstrap capacitors are always kept charged.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup

With the purpose of verifying the performance of the proposed circuit, a prototype was implemented based on Fig. 9 and tested under several conditions. The NPC inverter was implemented, with IGBTs of type IRG4BC20KD, and connected to a dc-link voltage rated initially at $\pm 160\text{ V}$ with a split power supply ($V_{DC+} = 320\text{ V}$).

In the gate drive circuit, MGDs of type IC IR2110 were used to trigger switches Q3 and Q4 and two IR2117 to trigger Q1 and Q2. The capacitors’ calculation was based on (1) and (8), resulting in $C_1 = C_2 = C_3 = 1\mu\text{F}$ and $C_{P1} = 220\text{ nF}$. The Zener diode (VZ1) ratings are 18 V/1 W; the diodes DA and DB are of type BYT79-500, while D4, D5, and D6 are of type BA159 and the voltage supply $V_1$ is set to 15 Vdc.

The oscillator frequency of the charge control circuit was set to 4.3 kHz, and its Zener diode rates are 18 V/1 W. The current source values are obtained from (4) and are equal to 3 mA.

Fig. 12 shows the complete prototype of the NPC inverter feeding a three-phase resistive load.

All of the experimental results presented here were obtained with a switching control of a square-wave type. It consists of a 12-pulse sequence based on the switching sequence as presented in Table I. Fig. 13 shows one switching sequence applied to each phase leg that produces output voltages at 60 Hz.

These switching sequences must follow this pattern, no matter what the choice of the modulation technique is [14]. Fig. 13 also shows the dead-time interval between each switching change.

Experimental results of the three-phase system are presented in the next figures, with the inverter connected to a three-phase resistive load, with the use of Tektronix TDS 3034B.

The line voltage is a 12-step waveform with a maximum amplitude equal to $(2/3)V_{DC+}$, while the line-to-line voltage is a six-step waveform, with its maximum at $V_{DC+}$ (total dc bus voltage), as shown in Fig. 14.

The THD% of the line-to-line voltages are similar to the line voltages. Fig. 14(b) shows the experimental Fourier spectrum of the line-to-line voltage of Fig. 14(a).

B. Operation While Driving an Induction Motor

In this section, the experimental results are shown, when the dc bus voltage $V_{DC+}$ is set to 320 V and the inverter is driving an unloaded induction motor rated at 1 hp/3450 r/min.

Fig. 15 shows the line voltages and the switch-voltage waveforms of one phase leg. In Fig. 15(a) and (b), voltage spikes occur, which did not appear during the tests with the resistive load [Figs. 7 and 14(a)].

Fig. 15(b) shows that very short duration overvoltages happen only on the intermediate switches (Q2 and Q3). This result suggests that these switches must be rated at $V_{DC+}$ and top and bottom switches (Q1 and Q4) can be rated at half of $V_{DC+}$. Consequently, Q1 and Q4 can be built of power MOSFETs, while IGBTs are recommended for Q2 and Q3. The use of power MOSFETs can significantly reduce power loss and costs for low-power applications.

V. CONCLUSION

This paper presented a new hardware implementation of a bootstrap charge-pump-technique-based gate drive circuit applied to a three-level NPC inverter for low-power applications. The design equations and the considerations on the choice of components were experimentally verified. The main advantages are as follows: the use of commercially available MGDs, with the benefit of low power consumption; the use of a single low power supply for the whole three-phase system gate driver and the protection circuits; and safe operation of power switches with long turn-on time intervals. However, the results suggest that a hybrid implementation of each phase leg, consisting of MOSFETs with voltage ratings at half of the dc bus voltage and of IGBTs rated at the total dc bus voltage, is recommended for achieving safe operation during transients and for reduced power losses and costs.
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