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Edge current induced failure of semiconductor PN junction during operation in the breakdown region of electrical characteristic

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Typical blocking I–V characteristics are shown and analyzed for PN junctions exhibiting a breakdown region above 1000 V from commercial diodes and power MOSFETs. The leakage reverse current of PN junctions from commercial silicon devices available at this time has a flowing component at the semiconductor–passivant material interface around the junction edge. For high voltage commercial power MOSFETs operation in the avalanche breakdown region is limited to 150 V. Above 150–175 °C even for controlled-avalanche diodes deviation from linear variation results in a breakdown region with round knee and still with visible voltage dependence at current increase. Such soft breakdown region caused by the phenomena in the interfacial layer is exhibited at lower applied reverse voltage than the expected one for breakdown caused by charge carrier avalanche multiplication at the junction. Operation even for short in the soft breakdown region can lead to PN junction failure and for this reason, a maximum working permissible reverse voltage is specified in device data sheet with a value under the breakdown region. Junction failure consists in significantly lower reverse voltage than the initial one or even electrical short-circuit caused by a spot of material degradation in the interfacial layer from the junction periphery. Operation of the controlled-avalanche diode in the breakdown region is possible only for single pulse of short duration and at junction temperature not higher than 175 °C. Above 150–175 °C even for controlled-avalanche diodes deviation from linear variation of the reverse current has been observed and soft breakdown region can appear before the expected avalanche breakdown. Device failure after operation in the breakdown region, caused by spot of material degradation at the junction periphery has occurred in such conditions. For high voltage commercial power MOSFETs operation in the avalanche breakdown region is limited to 150 °C.

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1. Introduction

Semiconductor PN junctions from available commercial silicon high voltage devices may exhibit failure when operation in the breakdown region is allowed. For this reason, a maximum permissible working reverse or blocking voltage is specified in the data sheets to prevent operation at higher voltage reaching the breakdown region. Most of commercial power silicon diodes and thyristors are in this situation, although operation in the breakdown region for auto-protection against transient over-voltages is desirable. Only for controlled-avalanche PN junctions, operation in the breakdown region is allowed in specified conditions. For this reason, silicon controlled-avalanche PN junction devices are used in practice to protect devices with a specified maximum permissible working voltage [1]. Weakness for operation in the avalanche breakdown region of high voltage diodes was reported long time ago [2,3]. At this time, commercial controlled-avalanche diodes with breakdown voltage lower than 300–400 V withstand without failure, significantly higher power in the avalanche breakdown region than similar controlled-avalanche diodes of the same junction area but of breakdown voltage higher than 1000 V. To our knowledge, explanation and understanding of such behavior is
not available in the literature. The presence and influence of the leakage reverse current existing from low applied reverse voltage is not taken into consideration in the breakdown region.

Excessive reverse leakage current flow at the junction edge [4], was considered a major limitation for reaching higher working reverse voltage towards the theoretical expected value of breakdown voltage. Instability of reverse I–V characteristic due to the junction edge leakage current at high temperature operation and applied voltage below the breakdown voltage was reported [5–7].

In spite of presence of the leakage reverse current at the PN junction edge in modern devices [8], little importance is given to it and for operation of silicon PN junction devices at high temperature only the junction bulk current is considered [9].

The purpose of this paper is to provide further experimental results and analysis, revealing the influence of the leakage current from the semiconductor–passivant dielectric interface from the PN junction periphery, on the device reliability at operation in the breakdown region.

2. Analysis of experimental reverse electrical characteristics and the junction edge leakage current component

Reverse I–V characteristics for PN junctions from commercial silicon diodes available at this time on the market, revealing typical behavior before and in the breakdown region are shown in Fig. 1 for an ordinary rectifier diode, and in Fig. 2 for a controlled–avalanche rectifier diode [10]. Both the investigated diode samples are of standard recovery type, that is, high charge carrier lifetime is exhibited in the junction base. It is seen from Figs. 1a and 2a that at low applied reverse voltage, $V_R$ voltage dependence of the reverse current, $I_R$, as $V_R^{-1/n}$ is exhibited [11], where $n$ is an integer equal or greater than 4. Such behavior, hardly could be attributed to the junction bulk generation or diffusion components of $I_R$. At room temperature, voltage dependence as $V_R^{-3/2}$ or $V_R^{-1/3}$ (abrupt or linear graded PN junction) is expected from the bulk generation current. Nonetheless for silicon PN junctions exhibiting variation of $I_R$ as $V_R^{-3/2}$ or $V_R^{-1/3}$ at room temperature, experimental evidence there exists for a dominant edge current component of $I_R$ [12–14]. Deviation of $I_R$ at room temperature above 50–100 V from the initial linear dependence ($V_R^{-1}$) to another linear dependence as $V_R^{-1/(2n)}$ or $V_R^{-1/3}$ (Figs. 1a and 2a) is rather caused by its junction peripheral component and not by its bulk component. At high temperature, saturation tendency of $I_R$ at low voltage in Figs. 1a and 2a could be attributed to the constant bulk diffusion current. Nonetheless, deviation from the constant current at higher voltage cannot be explained by the bulk component of $I_R$. Similar behavior related to constant current and deviation from it takes place for the drain current of a power MOS transistor [15]. When bias voltage comparable with the threshold voltage is applied on the gate, the multiple cell drain junction exhibits constant current at low drain positive voltage and deviation at higher applied voltage. In such a situation most of the drain current flows at the cells’ junction edge. Further results for MOSFETs will be shown below.

Significant contribution to the level of $I_R$ in Figs. 1 and 2 below the breakdown region comes from the junction periphery. In Fig. 3, PN junction silicon dice with junction terminations (glass passivated plane junction and planar junction with diffused rings), widely used at this time for commercial diodes are shown. Besides the junction bulk current component, $I_{R,B}$, significant junction edge current component, $I_{R,E}$, can flow through a very thin interfacial layer, located between the silicon and the junction passivating material layers. This $I_{R,E}$ edge current is present from low applied voltage up to the breakdown region. The properties of the interfacial layer incorporating fixed electric charge and atomic layers from the semiconductor and passivating materials are different from these two materials. The total current $I_R$ is given by the sum of the $I_{R,B}$ and $I_{R,E}$ components. Experimental evidence for excessive junction edge current ($I_{R,E}$) was also given in [16], in spite of suitable used junction termination and passivation material. The $I_{R,E}$ edge current component can be the primary component of $I_R$ for PN junctions from commercial devices available on the market at this time [17,18]. This edge current can cause junction pre-breakdown at voltage value significantly lower than the expected theoretical one.

To reach higher breakdown voltage value towards the theoretical expected value, different junction terminations [19,20], have been proposed. Nevertheless premature breakdown in practical devices based on such terminations at lower voltage value than the expected one [21], cannot be explained if the junction edge leakage current is not taken into consideration. Junction breakdown
results from experiments revealed disagreement not well explained. In the works [22–27] typical electrical characteristics similar to those given in Figs. 1 and 2, including the breakdown region up to high current level are not given. Such characteristics can reveal the nature of $I_R$ before the breakdown region is reached.

In Figs. 1b and 2b, plots of the same electrical characteristics given in Figs. 1a and 2a, but this time in log-linear scales are shown. The low leakage current region exhibits linear voltage dependence of the $I_R$ current above 100–300 V, given by the relation:

$$\log I_R/I_R^0 = mV_R$$

where $I_R^0$ is a current value at the intersection of the straight line fitting the electrical characteristic with the reverse current ordinate, and $m$ is a slope coefficient given by:

$$m = \Delta \log I_R/I_R^0$$

At some value of $V_R$ around 1000 V in Fig. 1b, deviation from linear variation takes place, manifested as accentuated current increase. This change in $I_R$ variation still with noticeable voltage dependence of $I_R$ is attributed to the $I_R$ edge current (Fig. 3). Significant edge current increase above 1000 V is caused by accentuated non-uniform flow in the interfacial layer around the junction periphery. In comparison with Fig. 2b where almost sharp knee (no deviation from linear variation) to the breakdown region is caused by charge carrier avalanche multiplication at the PN junction level, a soft breakdown region is exhibited above 1000 V in Fig. 1b. The current in this soft breakdown region is not the result of carrier avalanche multiplication process from the junction. For a diode sample similar to that used in Fig. 1b, practically vertical region given by carrier avalanche multiplication has been observed at 1700–1800 V, by applying short duration pulse voltage at room temperature. Such vertical avalanche region has been observed at pulsed current level higher than 50 mA, but failure has occurred during such a test.

The interfacial layer, the location of the edge current, (Fig. 3), may have different properties from a device type (manufacturer) to another as a consequence of the junction passivation process. In the case of Fig. 2b, the interfacial layer provides better stability of the electrical phenomena than in the case of Fig. 1b and therefore different voltage dependence is exhibited at higher applied voltage. Pre-breakdown started at about 1000 V is visible in Fig. 1b, instead of an expected avalanche breakdown at 1700–1800 V. The electrical characteristics from Figs. 1 and 2 in linear-linear scales indicate resistive behavior attributed to the interfacial layer. The plots in Fig. 4a and b are shown at room temperature but similar behavior is manifested at high temperature. Non-linearity of the resistance of the interfacial layer (Fig. 3) is manifested at low and high voltage for the ordinary rectifier diode (Fig. 4a). Similar behavior is exhibited at high temperature. For the controlled-avalanche diode, linearity of the interfacial layer resistance is manifested practical on the entire voltage range (Fig. 4 b). Similar behavior takes place up to 150 °C. Non-linearity at higher applied reverse voltage causes pre-breakdown or soft breakdown region before the expected junction avalanche breakdown region is reached. In spite of suitable junction termination providing lower electric field at the junction edge than in its bulk [28–30], pre-breakdown in the interfacial layer may cause PN junction failure.

3. Device reliability at operation in the breakdown region

The diode sample used in Figs. 1a and b and 4a corresponds to commercial glass passivated (Fig. 3a) rectifier diodes available on the market at this time, 6 A maximum rectified current and 600 V maximum permissible repetitive working voltage, $V_{FWMR}$ are the main specifications in the data sheet for the diode type.

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**Fig. 2.** Typical reverse I–V characteristics at room and high junction temperature for commercial controlled-avalanche rectifier diode: (a) log-log scales I–V characteristics and (b) log-linear scales I–V characteristics.

**Fig. 3.** Silicon die of glass passivated diode (a) and of planar oxide passivated diode (b) 1 – PN junction; 2 – interfacial layer between the semiconductor and passivating material; 3 – junction bulk depletion layer; 4 – passivating layer and 5 – diffused rings (junction termination).
sample used in Figs. 1a and b and 4a. Nonetheless, diode types of VRWM = 800 V or 1000 V can be seen in the same data sheet. From Fig. 4a for a 600 V diode type sample, it is seen that above 800–1000 V, deviation from linear variation takes place and non-specification of VRWM at 800 or 1000 V in such a case is understandable. Specifications of VRWM at 50, 100, 200 and 400 V in the same data sheet is due to the fact that an edge current related breakdown region (pre-breakdown) is closer to such voltage values. Although in the manufacturing process, initial silicon material targeting working voltage above 1000 V may be used, different voltage device types will result (manufacturing yield) because the level of the junction edge current in the interfacial layer has large fluctuations.

Short time operation of the diode sample used in Fig. 1a and b or in Fig. 4a at breakdown current higher than 10 mA and at room temperature resulted in device failure. The device definitive failure is preceded by thermal second breakdown as illustrated in Fig. 5. In this figure only initial and final phases are shown. It is not easy to describe the transition phases. After device failure, a different electric characteristic at room temperature is exhibited (Figs. 1a and b and 4a). Now the soft breakdown region related to the edge current is manifested starting with 500 V at room and high temperature and consequently, a value of VRWM lower than 600 V (limited to 300–400 V) has to be specified for reliable operation. The failed characteristic in Figs. 1a and b and 4a is the result of some local change in the interfacial layer from the junction periphery due to local overheating. Electrical characteristics like for the failed characteristic are possible in fabrication due to junction passivation process insufficiency, so that, local “defects” in the resulted interfacial layer leading to manufactured devices of lower reverse voltage. Repetition of short time operation in the breakdown region at high current level above 10 mA, for the new obtained electrical characteristic after failure (Figs. 1a and b or 4a) results in further degradation. Device failure analysis indicated that a small spot of material degradation in one corner of the silicon die, as shown in Fig. 6 causes lower reverse voltage handling capability after failure. By using suitable etching procedure to remove the degraded material spot from the corner, a new I–V characteristic of higher reverse voltage closer to the initial characteristic (Fig. 4a) was obtained. This confirms the role of the edge current from the junction interfacial peripheral layer in premature breakdown.

For the controlled-avalanche diode (Figs. 2a and b and 4b), operation was performed in the breakdown region, at avalanche breakdown current higher than 10 mA, in the same conditions when failure occurred for the above ordinary rectifier diode. No failure took place even at higher current than used for the ordinary rectifier diode. The main specifications in the data sheet for the controlled–avalanche diode are the following: 2A maximum rectified current, maximum reverse repetitive voltage, VRM = 1000 V and allowed operation in the breakdown region with a specification of 20 mJ single surge absorbed energy in the avalanche region at junction temperature, $T_j = 175 \, ^\circ C$. Although at room temperature there is no specification for the single surge absorbed energy in the data sheet, this is significantly higher than 20 mJ. Another manufacturer for the same device type specifies in the data sheet for operation in the avalanche breakdown region a maximum power of 1000 W for sine wave pulse of 20 $\mu$ s duration at 175 $\, ^\circ C$. The silicon die of the controlled–avalanche diode type has an area of at least two times lower than the corresponding one of the ordinary rectifier diode.

Applied peak pulsed power of 1000 W in the avalanche region (Fig. 2a and b) and instantaneous avalanche voltage around of 2000 V will give a peak avalanche current of about 0.5 A. An absorbed energy of 20 mJ at 175 $\, ^\circ C$ does not have much contribution to additional junction temperature increase. Taking into account
the diode thermal capacitance, more than $5 \, ^\circ C$ rise above $175 \, ^\circ C$ is not possible. Nevertheless applied avalanche pulse at $175 \, ^\circ C$ junction temperature higher than $40–50 \, mJ$ can cause diode failure, although instantaneous junction temperature higher than $200 \, ^\circ C$ is not reached.

Possible failure mechanism for the controlled-avalanche diode in the breakdown region is also related to the junction edge current at high temperature. In Fig. 7 the current–voltage characteristics from Fig. 2a and b are plotted in linear–linear scales. While at $150 \, ^\circ C$, linear voltage dependence of $I_R$ is still exhibited up to the breakdown region, at $200 \, ^\circ C$, deviation is visible above $1400 \, V$, due to non-uniform edge current flow around the junction periphery. In the avalanche region at peak avalanche current around $1 \, A$ and about $200 \, ^\circ C$, the instantaneous voltage can overcome $2000 \, V$. The reverse leakage current already deviated from linear dependence can vary so that a soft breakdown region before the avalanche breakdown region is reached and failure can occur. Thus the failure may occur due to the breakdown in the interfacial layer from the junction edge and not to the breakdown caused by carrier avalanche multiplication at the PN junction itself.

For controlled-avalanche diodes of higher voltage and larger area, deviation from linear variation of $I_R$ has been found at temperature of $100–150 \, ^\circ C$ as shown in Fig. 8. Nonetheless in comparison with an ordinary rectifier diode, the deviation remains under control, and a breakdown region controlled by the junction carrier avalanche multiplication is still reached. Main specifications given in the data sheet for the sample used in Fig. 8 are the following: $40 \, A$ rectified current, $V_{RWM} = 1200 \, V$ and $11 \, kW$ peak power in the avalanche region for $10 \, \mu s$ square pulse duration at $175 \, ^\circ C$. This corresponds to $110 \, mJ$ absorption energy. For a $10 \, \mu s$ pulse, about $3 \, A$ peak avalanche current is allowed. The energy of $110 \, mJ$ increases the junction temperature with a few degrees but failure occurs above $200–250 \, mJ$, although the instantaneous junction temperature remains lower than $200 \, ^\circ C$. It is worth to mention that for a $25 \, A$ and $1200 \, V$ avalanche diode from the same manufacturer, a $10 \, kW$ peak avalanche power is indicated in the data sheet in the same conditions, although the area of the silicon die is about two times lower. This may be related to the difficulties in controlling the edge leakage current for higher junction area devices. For such controlled-avalanche diodes, after failure in the avalanche breakdown region, spots of material damage have been found at the junction periphery and not on its internal area.

As a consequence of the above, the junction edge current can be a limitation even for the performance of controlled-avalanche PN junction diodes in the breakdown region. Higher absorption energy
and therefore higher junction temperature without failure is possible in the vertical avalanche breakdown region if a linear voltage dependence region of the reverse leakage current is exhibited up to the avalanche region at 200 °C and higher temperature.

As it is known power MOSFETs have also capability to operate in the avalanche breakdown region in specified conditions. Electrical characteristics for a commercial device are shown in Fig. 9a–c. Main specifications in the data sheet are the following: 3A maximum drain current, 125 W maximum power at 25 °C, 280 mJ single pulse avalanche energy at 25 °C and 3 A maximum peak avalanche current. The maximum operation temperature is 150 °C. At 150 °C the single pulse avalanche energy is practically zero.

For the drain electrical characteristics shown in Fig. 9a in log–log scale, the same linear voltage dependence of the drain current, \( I_D \), as \( V_{gs} \) at high temperature of 150–200 °C as in the diode case (Figs. 1a and 2a) is exhibited. At 225 °C and higher temperature, practically constant drain current is manifested at low voltage and then deviation from constant current as in the diode case. In Fig. 9a drain blocking characteristics are also shown for bias voltage on the gate, \( V_{gs} \) at 1.93 V at 150 °C and 175 °C. In comparison with \( V_{gs} = 0 \) V, an order of magnitude increase for the drain current level is exhibited. The drain current now is constant at low voltage and deviation from constant level takes place above 100 V. At such bias voltage applied on the gate, comparable with the threshold voltage, the drain current deviation is practically given by the current flow at the periphery of many paralleled PN junction cells. Therefore constant current at low voltage and deviation from this current is possible when the junction edge leakage current is dominant. In Fig. 9b, the characteristics from Fig. 9a are plotted in log-linear scales. Comparison with the characteristics of the controlled-avalanche diode (Fig. 2b) reveals that some deviation from linear variation takes place for the MOS transistor before the avalanche breakdown region is reached. When bias voltage is applied on the gate (higher leakage current at the cell junction edge) deviation from linear voltage dependence is again exhibited. From Fig. 9b it is seen that above 150 °C the breakdown voltage value does not increase as in the case of the controlled-avalanche diode (Fig. 2b). The maximum operation temperature for the MOS transistor is 150 °C. At this temperature according to the data sheet, the single pulse energy allowed in the avalanche breakdown region is practically zero, although at room temperature the specified value is 280 mJ. For the controlled-avalanche diode from Fig. 2a and b of lower area of the silicon die in comparison with the MOS transistor, at 175 °C, single pulse energy of 20 mJ is still allowed in the avalanche breakdown region. As a consequence, the available power MOS transistors do not have better surge energy handling capability in the avalanche region than controlled-avalanche diodes of comparable area of the silicon die and practically the same breakdown voltage. Such limitation may be related to the thickness of the silicon epitaxial layer used in MOS transistors.

In Fig. 9c, characteristics from Fig. 9a, b in linear–linear scale are shown. Comparison with characteristics of the controlled-avalanche diode (Fig. 7) indicates deviation from linear voltage dependence of the drain current at 150 °C without bias on the gate, starting from 1200 V, whereas the breakdown voltage value is about 1420 V. With applied bias on the gate \( (1.93 \) V) at 150 °C the drain current deviation takes place at 1000 V and continues until the breakdown voltage of 1420 V is reached. At 175 °C and no bias on the gate, deviation begins at 1200 V with higher slope of change than at 150 °C and a voltage value of 1420 V is reached at high breakdown current level of about 1 mA. Higher voltage in the breakdown region than 1420 V is not reached at 200 °C or 225 °C. This is due to the fact that the breakdown may be controlled now by the edge current of the cells drain junctions and not by junction carrier avalanche multiplication. Related to the temperature increase of the breakdown voltage value at a given breakdown current, the MOS transistor (Fig. 9b) manifests practically the same behavior as the ordinary rectifier diode (Fig. 1b). A difference consists in the fact that for the MOS transistor, in the

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**Fig. 9.** Drain blocking electrical characteristics for commercial power MOS transistor of 3 A and 1200 V: (a) log–log scales; (b) log–linear scales and (c) linear–linear scales.
vertical breakdown region the voltage dependence of the breakdown current is very reduced in comparison with the ordinary rectifier diode. Such behavior could be due to the fact that many cell breakdown regions are paralleled and contribution to the breakdown region may come from the punch-through effect of the drain junction (limited thickness of the N epilayer region).

4. Conclusions

I–V reverse characteristics at room and high temperature, with a breakdown region above 1000 V have been presented, for silicon PN junctions from available commercial silicon diodes and power MOS transistors. Voltage dependence of the reverse leakage current as \( V_{nl}^n \) (\( V_n \), is the reverse voltage) at room or higher temperature is possible where \( n = 2, 3, 4 \) and higher value, given by significant contribution from current flow at the junction edge. Deviation from such voltage dependence at higher voltage than 50–100 V in log–log scales cannot be explained by a dominant bulk component. The junction edge current flows in a very thin layer as interface between semiconductor and the junction passivation material. The electrical characteristics in log–linear scales or linear–linear scales above 100–300 V fit to linear variation. At higher applied voltage, deviation of leakage reverse current from linear variation region is possible and further variation results in a soft breakdown region, with noticeable voltage dependence. Due to flow of reverse current in the interfacial layer, a soft breakdown region appears at lower voltage than the expected vertical breakdown region, caused by junction carrier avalanche multiplication. Because operation in the soft breakdown region can lead to device failure, a maximum permissible working voltage is specified in the data sheet to avoid its reaching. The electrical characteristic of failed PN junctions can manifest soft breakdown region at lower reverse voltage than before failure or even electrical–short-circuit caused by spot of material damage at the junction edge. For high voltage controlled-avalanche diodes, current deviation from linear variation is not observed or is exhibited at lower degree up to 150 °C, so that the breakdown region caused by carrier avalanche multiplication is reached. Nonetheless, even for such junctions at 200 °C, noticeable deviation from linear variation takes place. A soft breakdown region related to the leakage current from the interfacial layer may appear before the true avalanche region is manifested and device failure can occur. Similar defects given by spot of material degradation at the junction periphery as in the case of an ordinary rectifier diode, were found for controlled-avalanche diodes. The power handling capability of commercial power MOSFETs in the avalanche breakdown region is not superior to that of controlled-avalanche diodes of the same area of silicon die and breakdown voltage value.

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References